D9050PCIC PCI Express® Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

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PCI Express Automated Testing—At A Glance

The Keysight D9050PCIC PCI Express® Automated Test Application helps you verify PCI Express device under test (DUT) compliance to specifications using Keysight Z-Series or UXR Series Infiniium oscilloscope.
The PCI Express® Automated Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the PCI Express® Automated Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

NOTE D9050PCIC PCI Express Compliance Test Application supports two channel scope. In case of two channel scope, only channel 1 and 2 will be available.

NOTE D9050PCIC PCI Express Compliance Test Application supports D9010AGGC Compliance Test Software Measurement Server for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com.

NOTE This document covers the methods of implementation for PCIe 5.0 and PCIe 6.0 devices. For PCIe 4.0 devices, please see the Keysight D9040PCIC PCI Express Compliance Test Application Methods of Implementation document.

Required Equipment and Software

In order to run the PCI Express automated tests, you need the following equipment and software:

- D9050PCIC PCI Express® Automated Test Application software and license
- MATLAB Run Time - R2021a (9.10)
- Intel Clock Jitter Tool 5.0.2 (https://www.intel.com/content/www/us/en/content-details/652180/clock-jitter-tool-5-0-2.html)
- Use one of the following oscilloscope models:
  - Keysight Z-Series Infiniium Oscilloscope
  - Keysight UXR Series Infiniium Oscilloscope
- E2688A Serial Data Analysis and Clock Recovery software
- Keyboard, qty = 1, (provided with the Keysight Infiniium Series Oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium Series Oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, qty = 2 (provided with the Keysight Infiniium Series Oscilloscope)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length

In This Book

This manual describes the tests that are performed by the PCI Express® Automated Test Application in more detail; it contains information from (and refers to) the base specification, and it describes how the tests are performed.

This manual is divided into following sections:

- “Introduction” covers the software and license installation and test preparation guide.
- “PCI-Express Gen5 2.5 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 2.5 GT/s.
- “PCI Express Gen5 5.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 5.0 GT/s.
- “PCI-Express Gen5 8.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 8.0 GT/s.
- “PCI Express Gen5 16.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 16.0 GT/s.
- “PCI Express Gen5 32.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 32.0 GT/s.
- “PCI-Express Gen6 2.5 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 2.5 GT/s.
- “PCI Express Gen6 5.0 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 5.0 GT/s.
- “PCI-Express Gen6 8.0 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 8.0 GT/s.
- “PCI Express Gen6 16.0 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 16.0 GT/s.
- “PCI Express Gen6 32.0 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 32.0 GT/s.
- “PCI Express Gen6 64.0 GT/s Tests” covers the PCI Express Gen 6 tests and methods of implementation at 64.0 GT/s.
- “Appendices” covers oscilloscope calibration, channel de-skew calibration, and index information.

The chapters in this book are:

- Chapter 1, “Installing the PCI Express Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the PCI Express® Automated Test Application and gives a brief overview of how it is used.
- Chapter 3, “Reference Clock Tests, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests for all data rates.
- Chapter 4, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 2.5 GT/s data rate.
- Chapter 5, “CEM-EndPoint Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-endpoint tests at 2.5 GT/s data rate.

- Chapter 6, “CEM-RootComplex Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-rootcomplex tests at 2.5 GT/s data rate.
- Chapter 7, “Reference Clock Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 2.5 GT/s data rate.
- Chapter 8, “Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 5.0 GT/s data rate.
- Chapter 9, “CEM-EndPoint Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-endpoint tests at 5.0 GT/s data rate.
- Chapter 10, “CEM-RootComplex Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM rootcomplex tests at 5.0 GT/s data rate.
- Chapter 11, “Reference Clock Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 5.0 GT/s data rate.
- Chapter 12, “Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 8.0 GT/s data rate.
- Chapter 13, “CEM-EndPoint Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-endpoint tests at 8.0 GT/s data rate.
- Chapter 14, “CEM-RootComplex Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-rootcomplex tests at 8.0 GT/s data rate.
- Chapter 15, “Reference Clock Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 8.0 GT/s data rate.
- Chapter 16, “Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 16.0 GT/s data rate.
- Chapter 17, “CEM-EndPoint Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-endpoint tests at 16.0 GT/s data rate.
- Chapter 18, “CEM-RootComplex Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-rootcomplex tests at 16.0 GT/s data rate.
- Chapter 19, “Reference Clock Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 16.0 GT/s data rate.
- Chapter 20, “Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 32.0 GT/s data rate.
- Chapter 21, “CEM-EndPoint Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-endpoint tests at 32.0 GT/s data rate.
- Chapter 22, “CEM-RootComplex Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 CEM-rootcomplex tests at 32.0 GT/s data rate.
- Chapter 23, “Reference Clock Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 32.0 GT/s data rate.
- Chapter 24, “Reference Clock Tests, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at all data rates.
- Chapter 25, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 2.5 GT/s data rate.
- Chapter 26, “Reference Clock Tests, 2.5 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 2.5 GT/s data rate.
- Chapter 27, “Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 5.0 GT/s data rate.
- Chapter 28, “Reference Clock Tests, 5.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 5.0 GT/s data rate.
- Chapter 29, “Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 8.0 GT/s data rate.
- Chapter 30, “Reference Clock Tests, 8.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 8.0 GT/s data rate.

- Chapter 31, “Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 16.0 GT/s data rate.
- Chapter 32, “Reference Clock Tests, 16.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 16.0 GT/s data rate.
- Chapter 33, “Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 32.0 GT/s data rate.
- Chapter 34, “Reference Clock Tests, 32.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 32.0 GT/s data rate.
- Chapter 35, “Transmitter (Tx) Tests, 64.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 transmitter tests at 64.0 GT/s data rate.
- Chapter 36, “Reference Clock Tests, 64.0 GT/s, PCI-E 6.0” contains more information on the PCI Express version 6.0 reference clock tests at 64.0 GT/s data rate.
- Appendix A, “Calibrating the Digital Storage Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the PCI Express automated tests.
- Appendix B, “INF_SMA_Deskew.set Setup File Details” describes a setup used when performing channel de-skew calibration.

See Also,

The PCI Express® Automated Test Application's online help, which describes:

- PCI Express Automated Testing—At a Glance
- Creating or Opening a Test Project
- Setting Up the Test Environment
  - Test Mode
  - Device Definition
  - Connection Setup
  - Test Report - User Comments
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
  - Options to Start Test Runs
  - Settings to Optimize Test Runs
- Configuring Automation in the Test Application
  - Using Script for Automation
  - Using Files for Automation
  - Running Automation Script or Files
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App
  - Customizing the Test Application
  - File Menu Options
  - View Menu Options
  - Tools Menu Options
  - Help Menu Options
  - Controlling the Application via a Remote PC
  - Using a Second Monitor

Contents

Part I
Introduction

KEYSIGHT TECHNOLOGIES

1 Installing the PCI Express Compliance Test Application

If you purchased the D9050PCIC PCI Express Compliance Test Application separately, you need to install the software and license key.

NOTE

D9050PCIC PCI Express Compliance Test Application supports **D9010AGGC Compliance Test Software Measurement Server** for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com.

Installing the Software

1. Please install the MATLAB Run Time - R2021a (9.10). To download please browse the URL: https://in.mathworks.com/products/compiler/matlab-runtime.html
2. To obtain the PCI Express Compliance Test Application, please go to Keysight website: http://www.keysight.com/find/D9050PCIC
3. The link for PCI Express Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

   Be sure to accept the installation of the .NET Framework software; it is required in order to run the PCI Express Compliance Test Application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1. Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

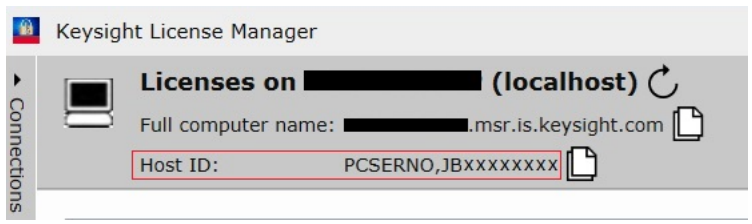


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1. Save the license files on the machine, where you wish to run the Test Application and its features.
2. Launch Keysight License Manager.
3. From the configuration menu, use one of the options to install each license file.

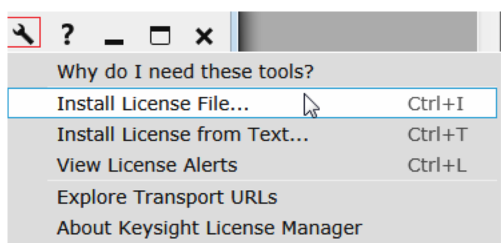


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

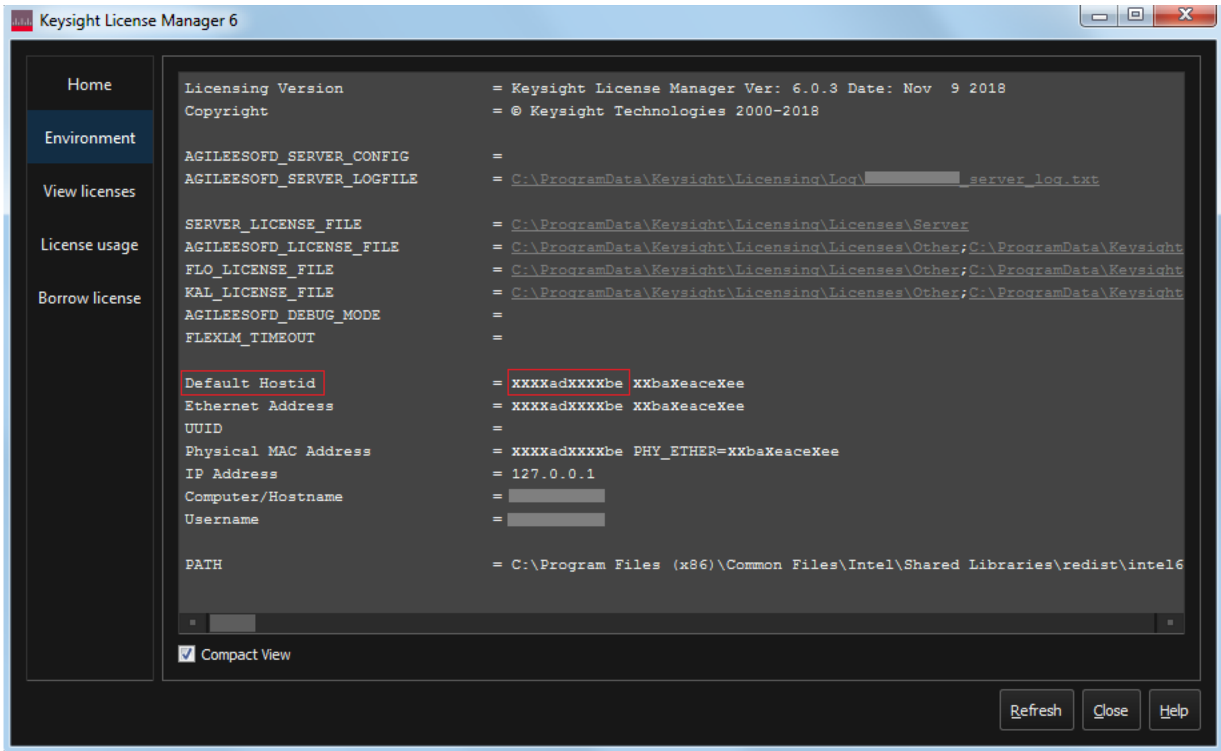


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

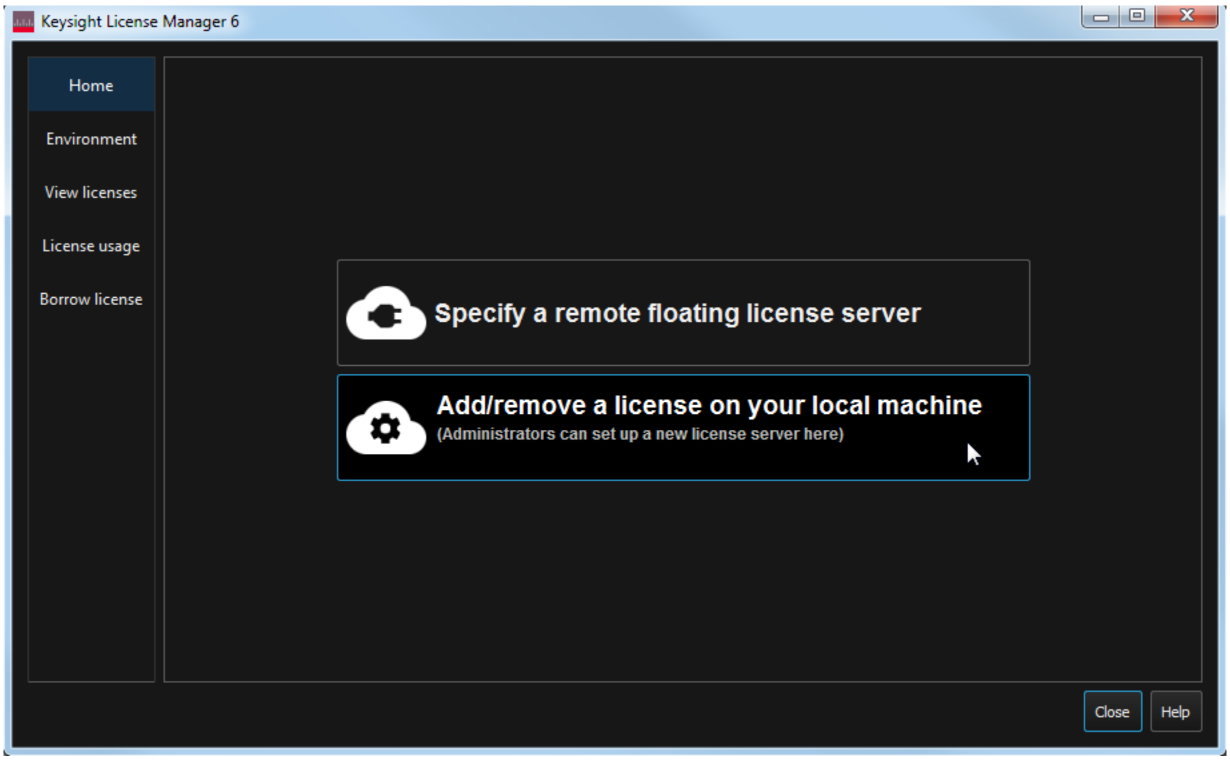


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

Before running the PCI Express automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the PCI Express Compliance Test Application and perform measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope, see Appendix A, "Calibrating the Digital Storage Oscilloscope.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration and channel de-skew calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel they were calibrated for.

Starting the PCI Express Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze** > **Automated Test Apps** > **D9050PCIC PCIE Test App**.

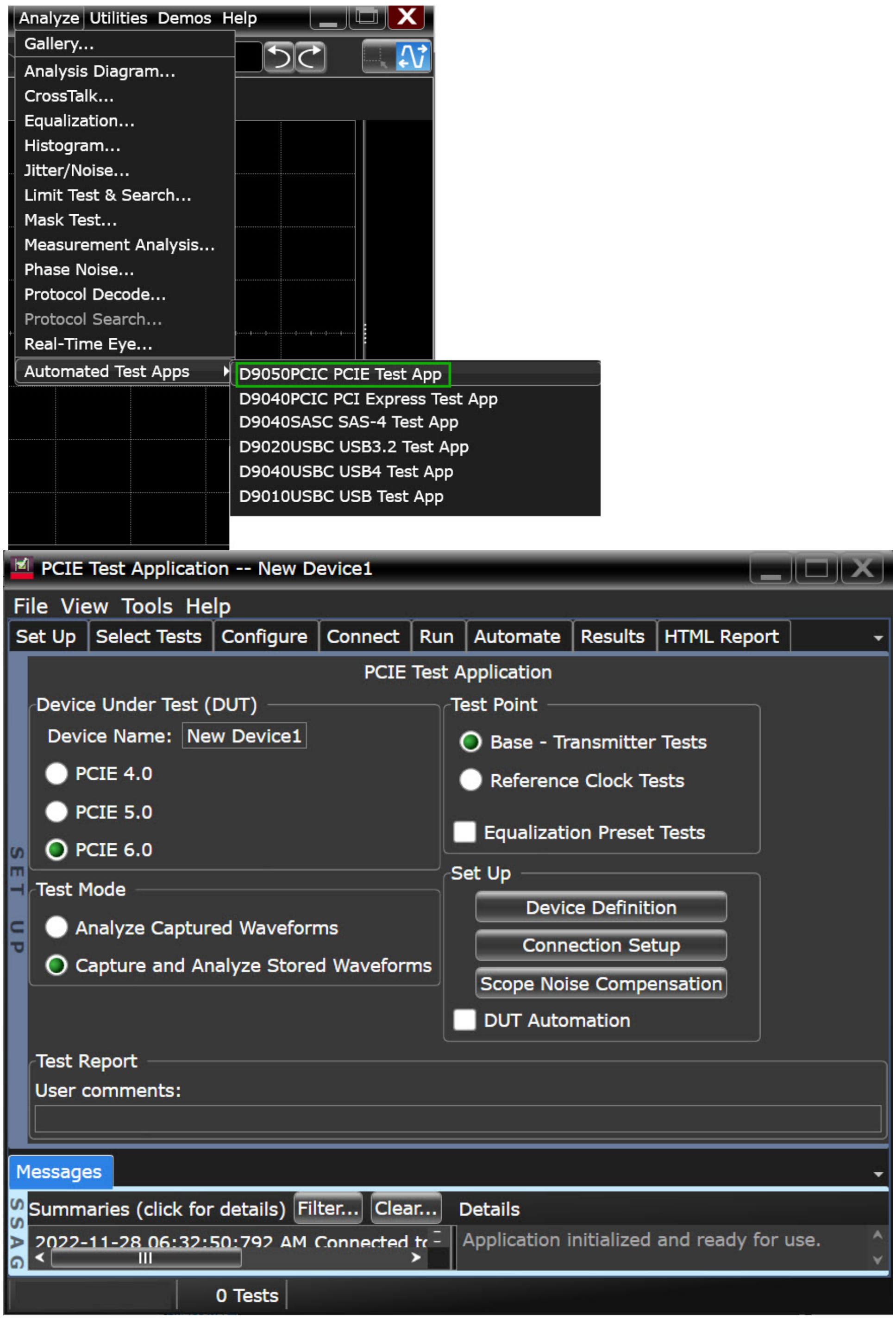


Figure 5 The PCI Express Compliance Test Application

NOTE

If PCI Express does not appear in the Automated Test Apps menu, the PCI Express Compliance Test Application has not been installed (see Chapter 1, “Installing the PCI Express Compliance Test Application).

Figure 5 shows the PCI Express Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure the test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Allows to automate tests through automation commands
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the PCI Express Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The PCI Express Compliance Test Application's online help describes:

- Starting the PCI Express Compliance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up the test environment.
  - To set up InfiniiSim.
  - To load saved waveforms.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
  - To select the "store mode".
  - To run multiple times.
  - To send email on pauses or stops.
  - To specify the event.
  - To set the display preferences.
  - To set the run preferences.
- Viewing test results.
  - To delete trials from the results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
  - To change the test display order.
  - To set trial display preferences.
- Viewing/exporting/printing the HTML test report.
  - To export the report.
  - To print the report.
- Saving test projects.
  - To set AutoRecovery preferences.
- Controlling the application via a remote PC.
  - To check for the App Remote license.
  - To identify the remote interface version.
  - To enable the remote interface.
  - To enable remote interface hints.
- Using a second monitor.

Part II
PCI-Express Gen5 All GT/s Tests

KEYSIGHT TECHNOLOGIES

3 Reference Clock Tests, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests, common to all data rates, using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE In case of Z-series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the PCIe Base Specification.

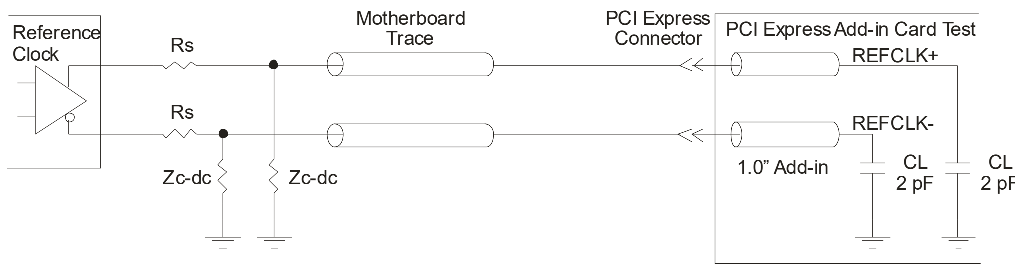


Figure 1 Driver Compliance Test Load.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > All Data Rate Tests > Reference Clock Tests**.

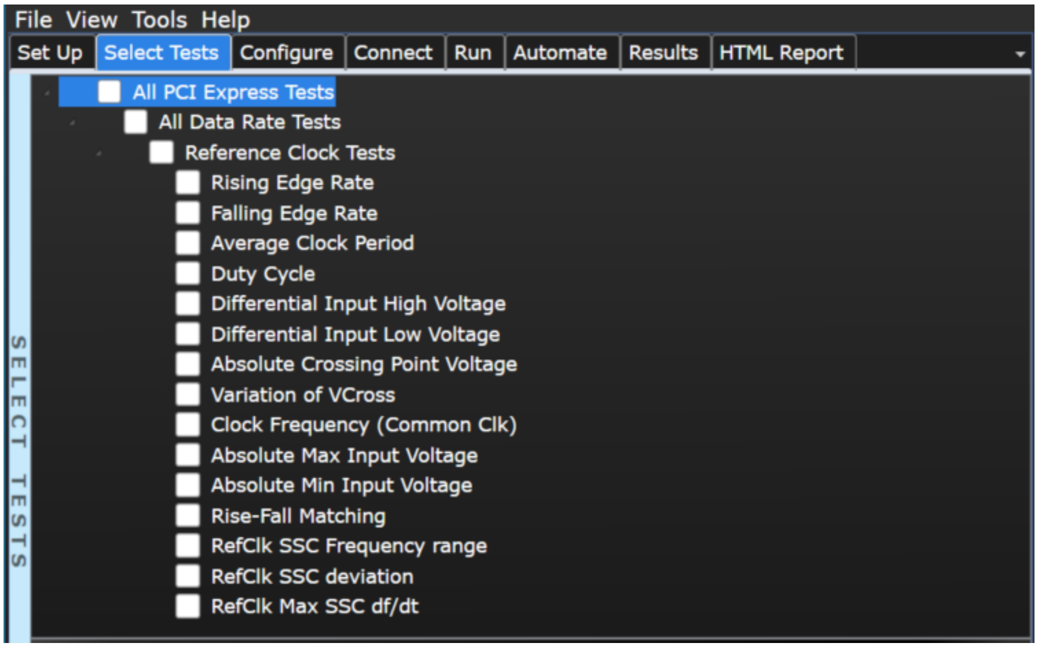


Figure 2 Selecting Reference Clock Tests

Rising Edge Rate Test

The rising edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for rise time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Rise Edge Rate	Rising Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 8-69.

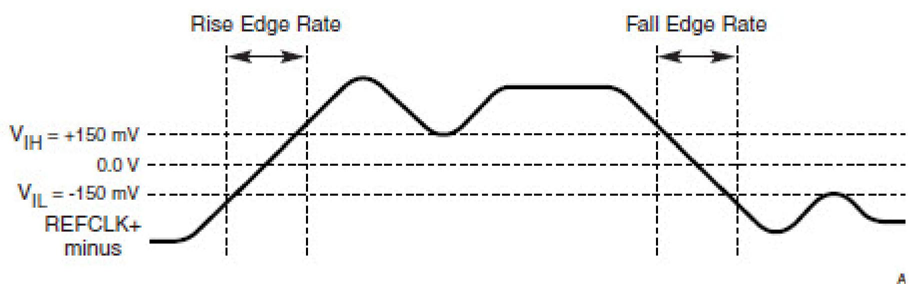


Figure 3 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the maximum rise time using **Rise time** measurement.
6 Zoom to maximum value of rise time.
7 Converts the maximum rise time to units of V/ns as given in the PCIE spec. [0.0000000003 / Maximum Rise Time value].
8 Reports the rising edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as `0.6 V/ns` ≥ Rising Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

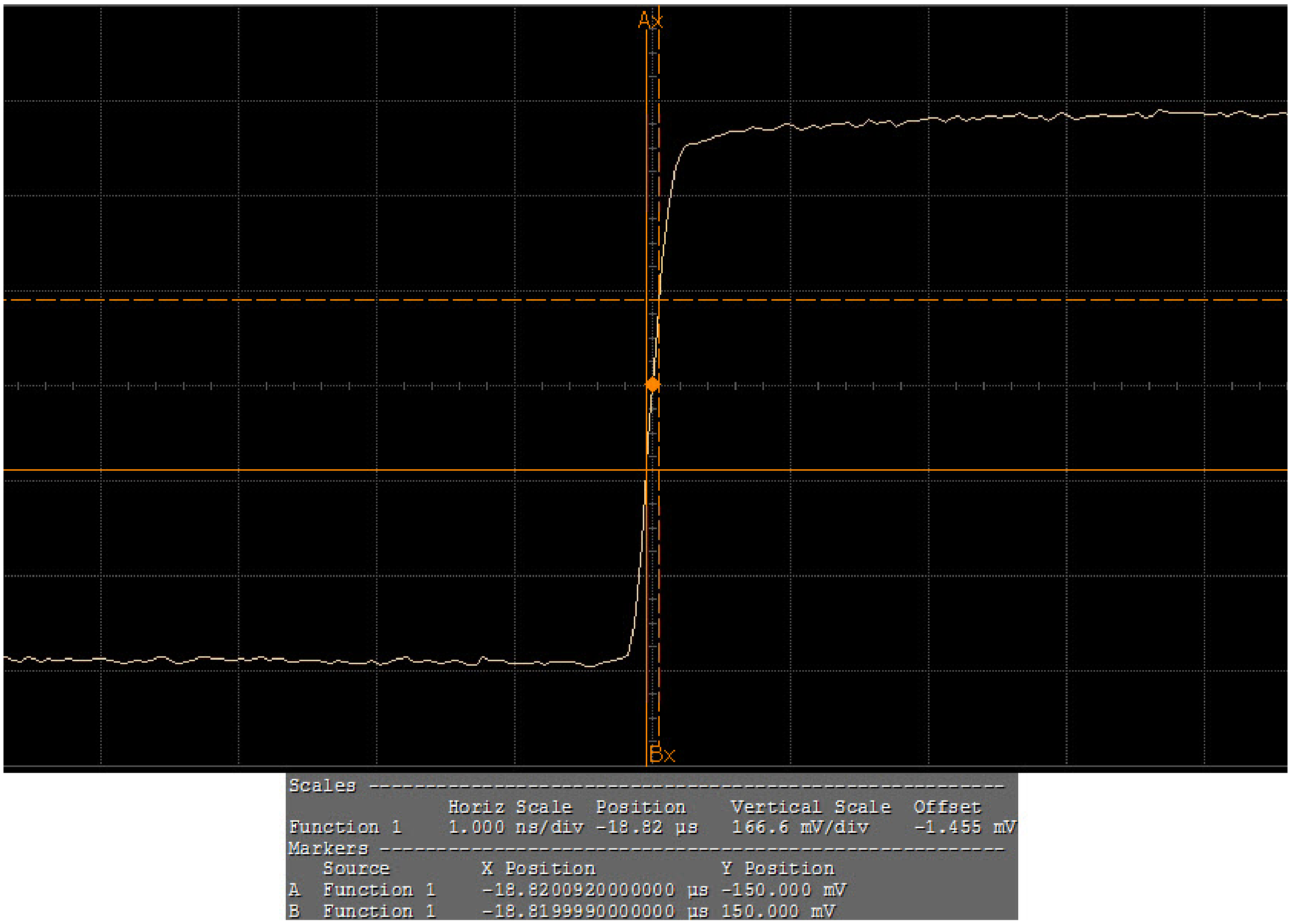


Figure 4 Reference Image for Rising Edge Rate

Falling Edge Rate Test

The falling edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for fall time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Fall Edge Rate	Falling Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See, Figure 8-69.

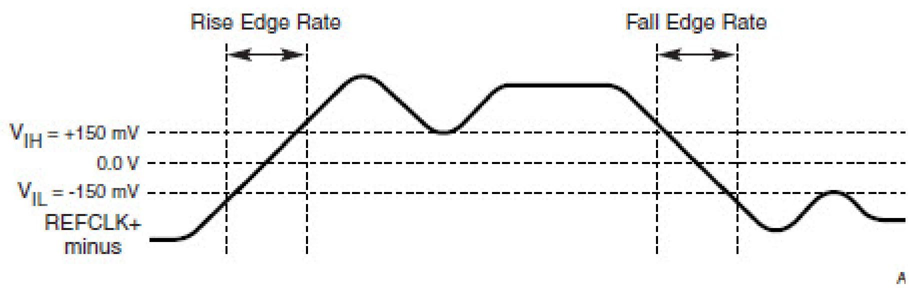


Figure 5 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the maximum fall time using **Fall time** measurement.
6 Zoom the resultant waveform to maximum value of fall time.
7 Converts the maximum fall time to units of V/ns as given in the PCIE specification [0.0000000003 / Maximum Fall Time value].
8 Reports the falling edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as 0.6 V/ns ≤ Falling Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

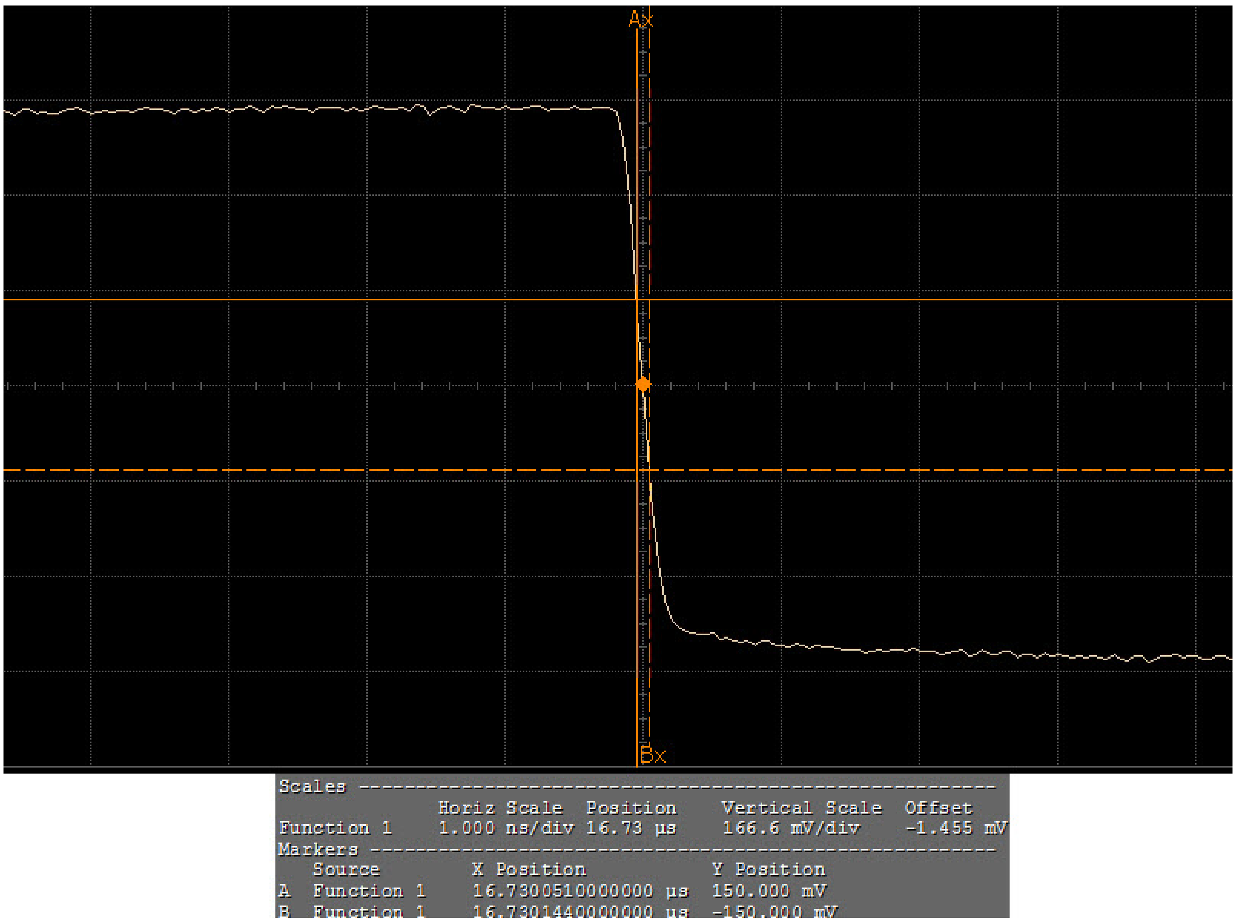


Figure 6 Reference Image for Falling Edge Rate

Average Clock Period Test

This test verifies that the Refclk Average Clock Period is within the conformance limits as specified in PCIE Express Base Specification, Revision 5.0, Section 8.6.2, Table 8-16.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2800 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Configures memory depth and sampling rate as per the data rate.
4 Fits and displays all sample data on screen.
5 Measures the average voltage using **V average** measurement.
6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7 Measures the average frequency using **Frequency** measurement of **Clock**.
8 Measures the average period using **Period** measurement of **Clock**.
9 Computes the difference between ideal and actual frequency in terms of parts per million of 100MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

NOTE
Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

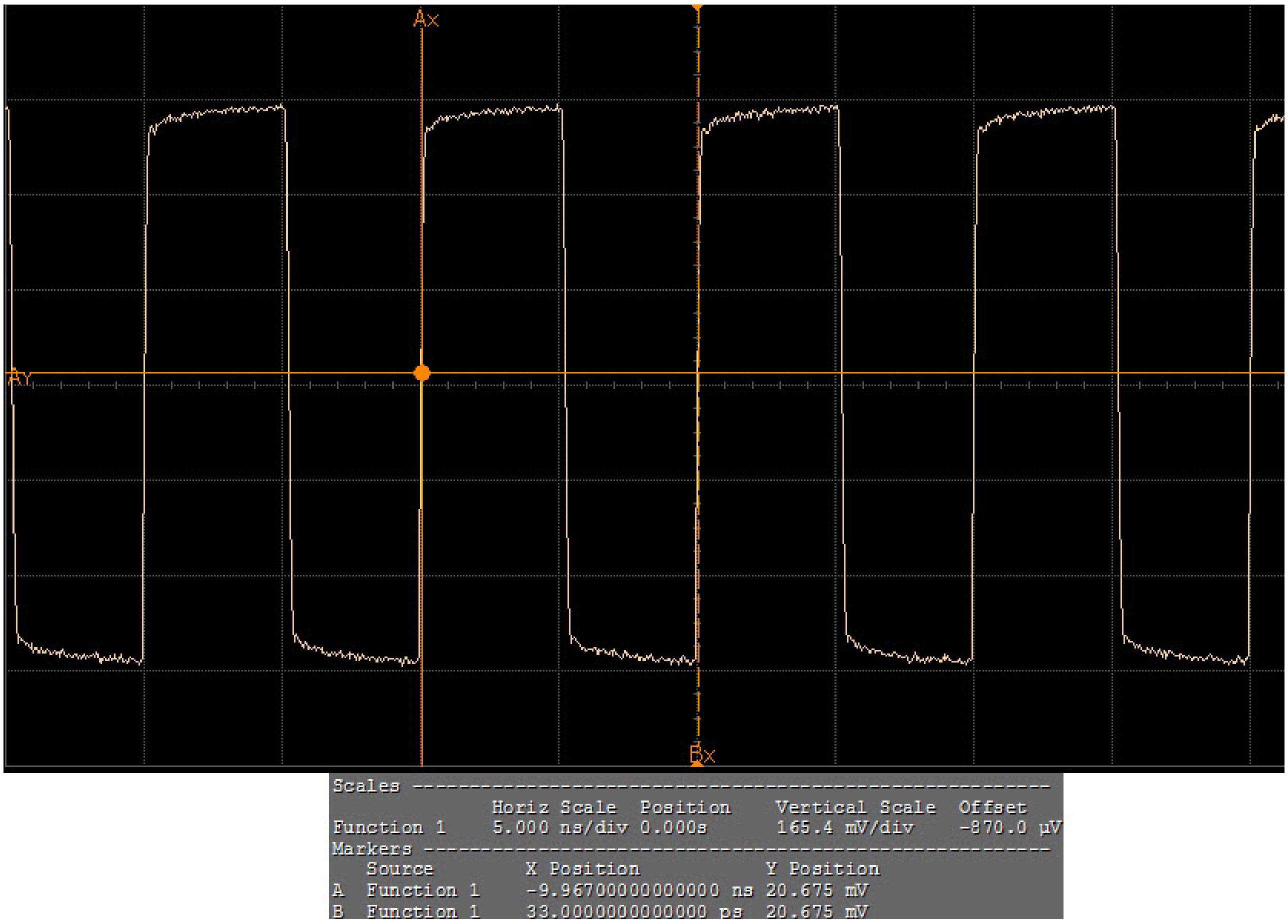


Figure 7 Reference Image for Average Clock Period

Duty Cycle Test

The duty cycle test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Duty Cycle	Duty Cycle	40%	60%

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Configures memory depth and sampling rate as per the data rate.
4. Fits and displays all sample data on screen.
5. Measures the average voltage using **V average** measurement.
6. Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7. Measures the duty cycle using the **Duty cycle** measurement.
8. Finds the margin for maximum duty cycle and minimum duty cycle.
9. Compares the margin and choose the largest margin to report the value (worst value) as duty cycle.
10. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as `40% ≤ Duty Cycle ≤ 60%`.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

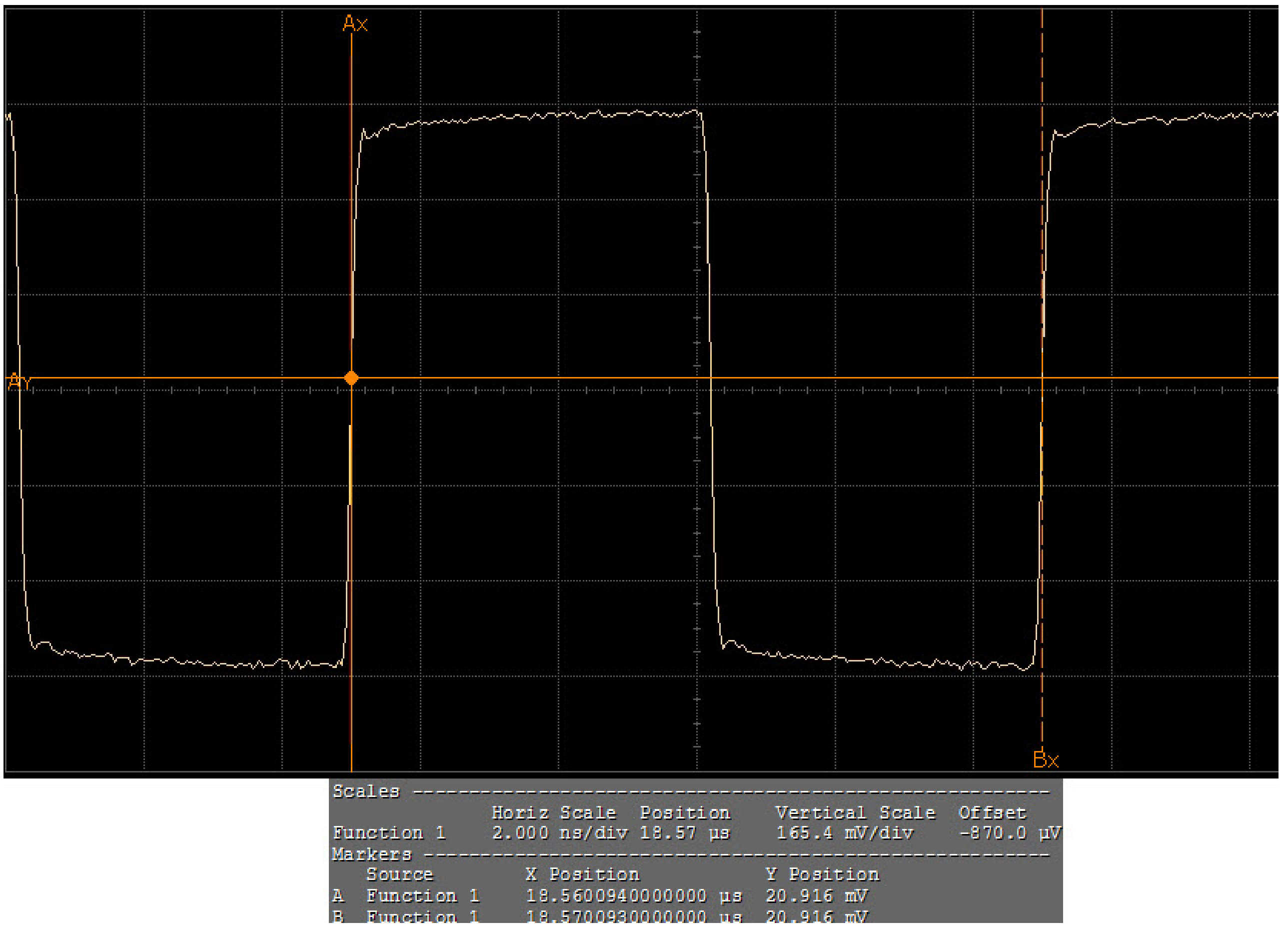


Figure 8 Reference Image for Duty Cycle

Differential Input High Voltage Test

The differential input high voltage test verifies that the reference clock differential input high voltage is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)
V_{IH}	Differential Input High Voltage	150 mV

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the maximum voltage using **V max** measurement.
6 Reports the maximum voltage value as differential input high voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as $V_{IH} > 150$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

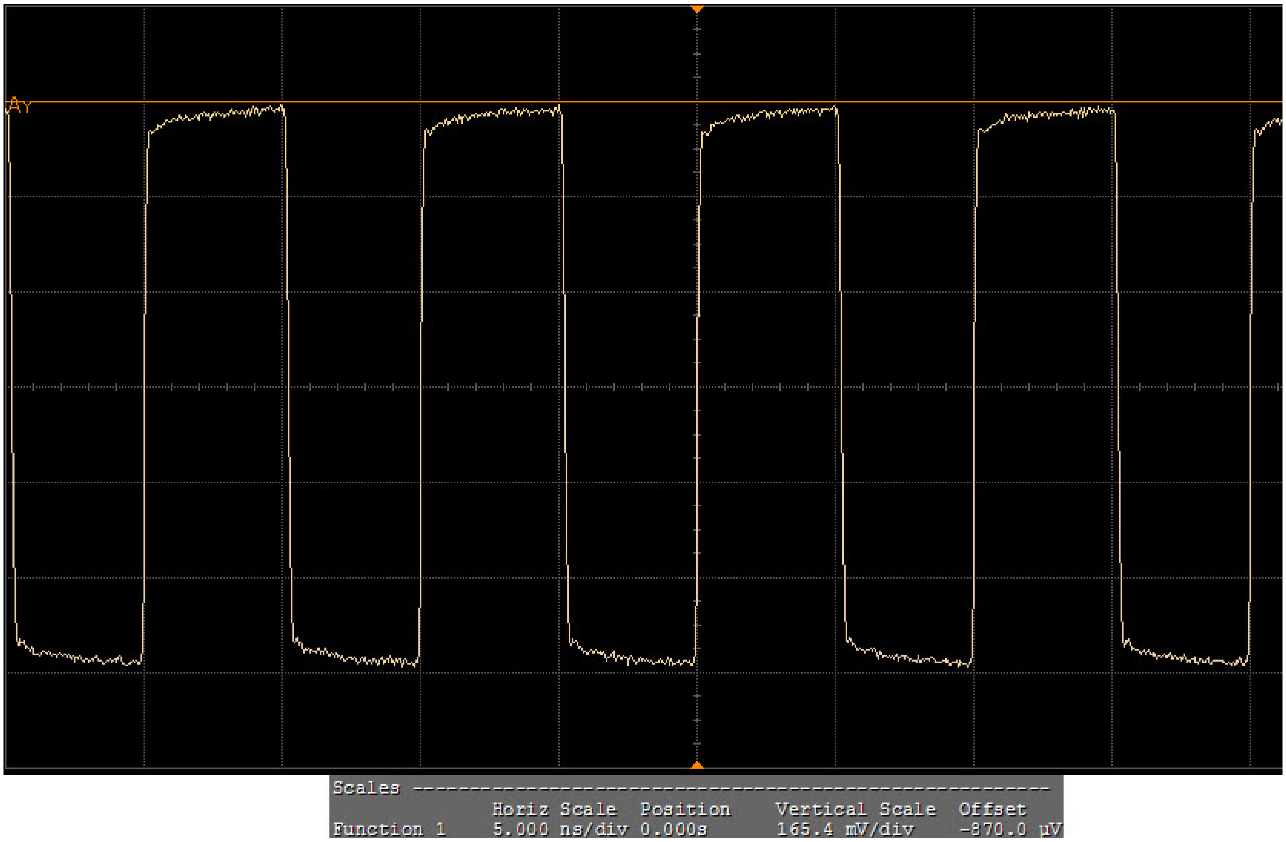


Figure 9 Reference Image for Differential Input High Voltage Test

Differential Input Low Voltage Test

The differential input low voltage test verifies that the reference clock differential input low voltage is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{IL}	Differential Input High Voltage	-150 mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the minimum voltage using **V min** measurement.
6 Reports the minimum voltage value as differential input low voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as V_{IL} < 150 mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

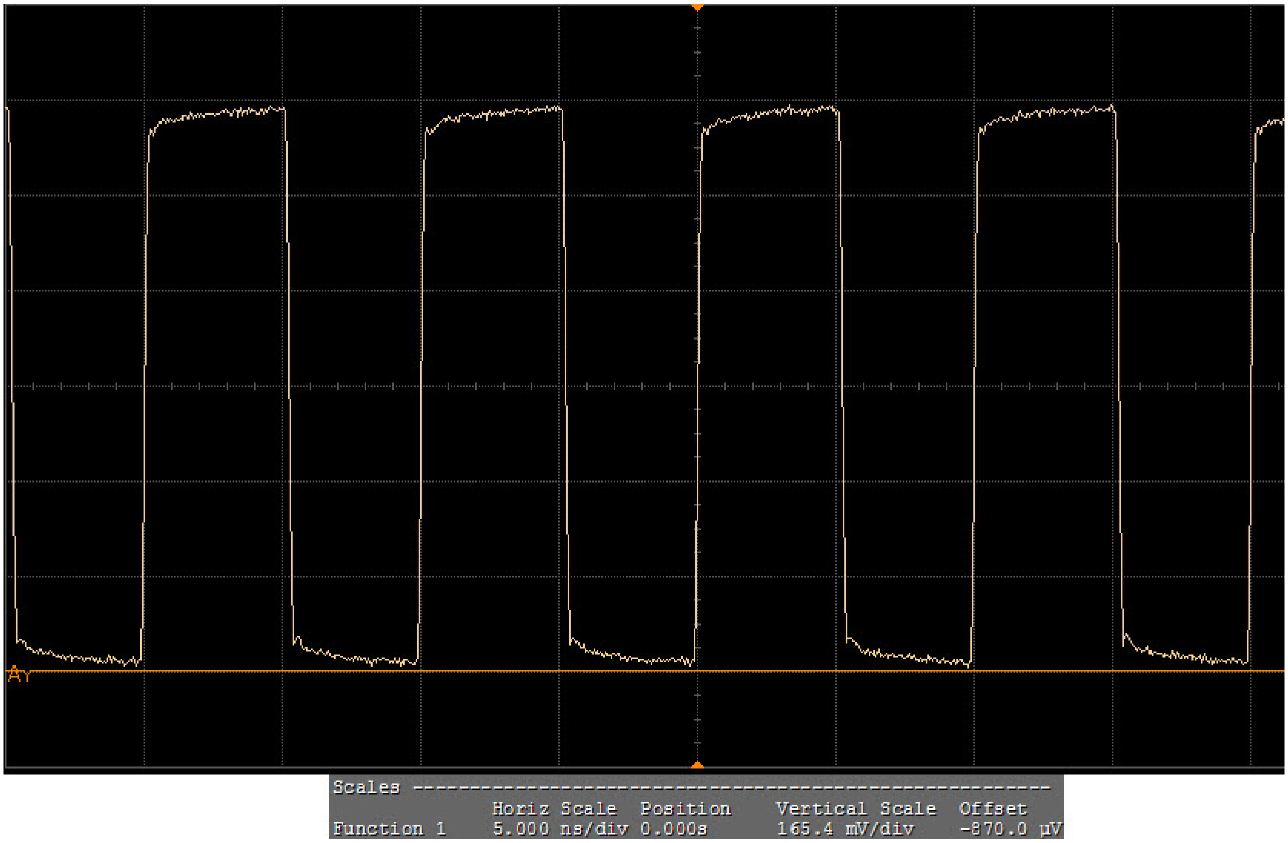


Figure 10 Reference Image for Differential Input Low Voltage Test

Absolute Crossing Point Voltage Test

The absolute crossing point voltage test is measured at crossing point where the instantaneous voltage value of the rising edge of RefClk+ equals the falling edge of RefClk-. It refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

Table 1 Absolute Crossing Point Voltage Test Details

Symbol	Parameter	Min(at 100 MHz Input)	Max (at 100 MHz Input)
V_{CROSS}	Absolute Crossing Point Voltage	+250 mV	+550 mV

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 8-65.

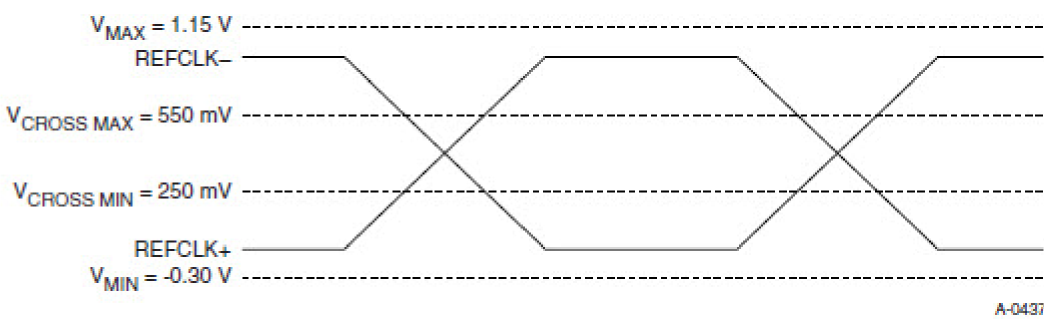


Figure 11 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.10 of the PCI Express Base Specification.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Uses MATLAB function to find the absolute crossing point voltage. The MATLAB function does the following:
   - *a* Finds crossing edges for rising and falling edges.
   - *b* Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.
4 Computes the margin for minimum crossing point voltage and margin of maximum crossing point voltage.
5 Compares the margin and choose the smallest margin to report the value (worst value) as absolute crossing point voltage.
6 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as `250mV ≤ Absolute Crossing Point Voltage ≤ 550mV`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Variation of V_{Cross} Test

The variation of V_{Cross} test is measured at crossing point where the instantaneous voltage value of the rising edge of Refclk+ equals the falling edge of Refclk-. It is defined as the total variation of all voltages of rising Refclk+ and falling Refclk-.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{CROSS} Delta	Variation of V_{CROSS} over all rising clock edges	+140 mV

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 8-66.

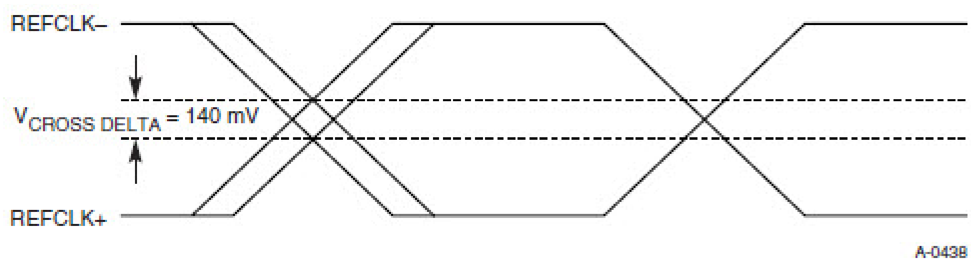


Figure 12 Single-Ended Measurement Points for Delta Cross Point

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Fits and displays all sample data on screen.
2. Uses MATLAB function to find the variation of V_{CROSS}. The MATLAB function does the following:
   - *a* Finds crossing edges for rising and falling edges.
   - *b* Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.
3. Finds the differential value between maximum crossing rising edge and minimum crossing rising edge as variation of V_{Cross}.
4. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{Cross} < 140\ mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Clock Frequency (Common Clk)

This test verifies that the measured reference clock frequency, F_{REFCLK}, is within than the allowed frequency range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 2 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{REFCLK}	Refclk Frequency	99.97 MHz	100.03 MHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100 MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel** Setup.
4. Sets the time scale to 5 ns.
5. Fits and displays all sample data on the screen.
6. Enables jitter analysis so that measurements are made on all edges.
7. Measures the clock frequency.
8. Reports the mean frequency.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Max Input Voltage Test

The absolute max input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{MAX}	Absolute Max Input Voltage	+1.15 V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the maximum instantaneous voltage including overshoot. See Figure 8-65.

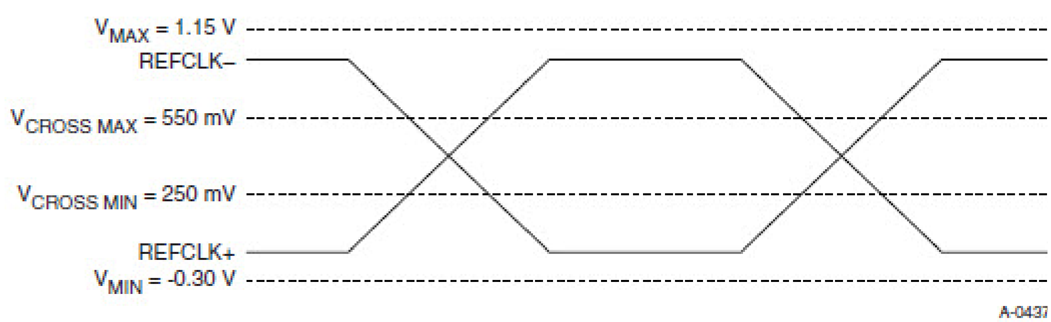


Figure 13 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5. Measures the RefClk+ maximum voltage using **V max** measurement.
6. Measures the RefClk- maximum voltage using **V max** measurement.
7. Compares the RefClk+ maximum voltage and the RefClk- maximum voltage.
8. Reports the largest value (worst value) as the Absolute Max Input Voltage.
9. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{MAX} < +1.15V$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

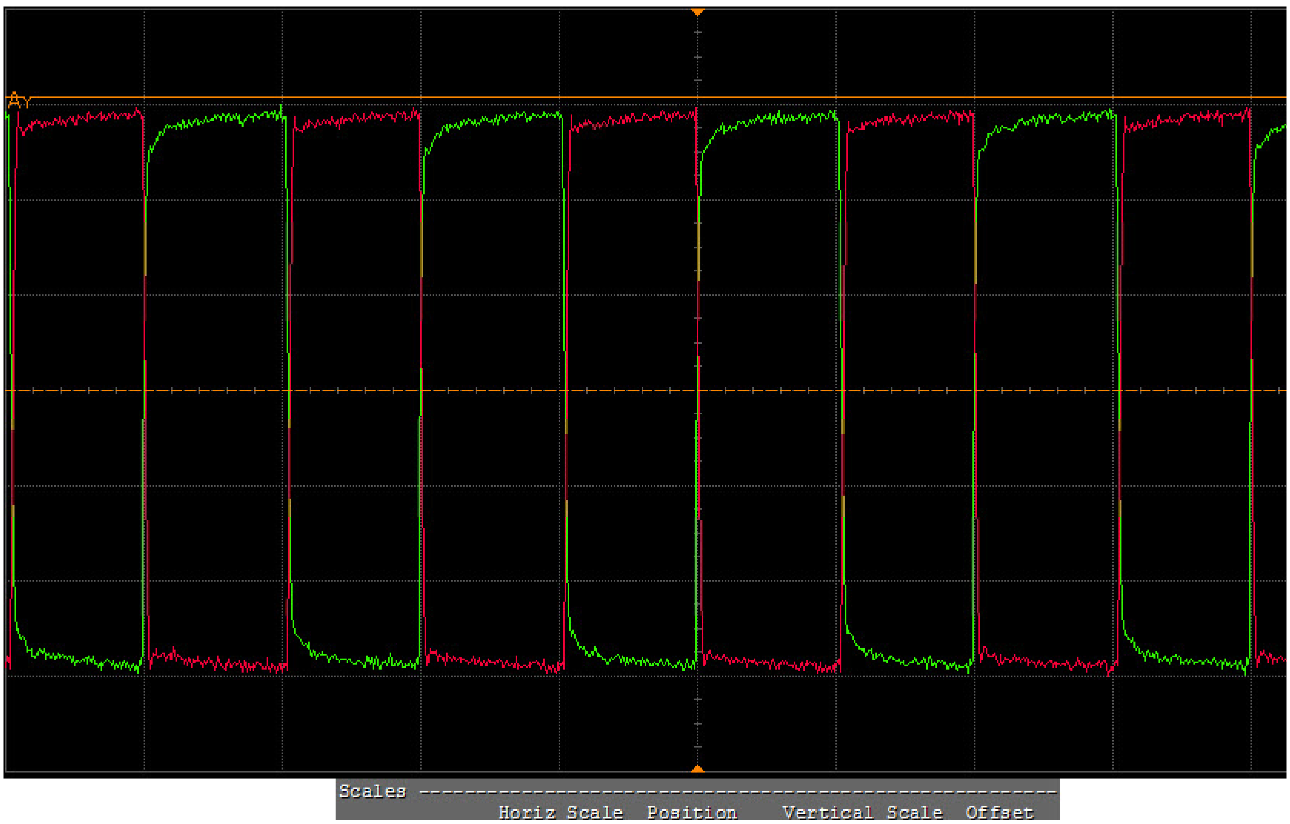


Figure 14 Reference Image for Absolute Max Input Voltage Test

Absolute Min Input Voltage Test

The absolute min input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{MIN}	Absolute Min Input Voltage	-0.3 V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the minimum instantaneous voltage including undershoot. See Figure 8-65.

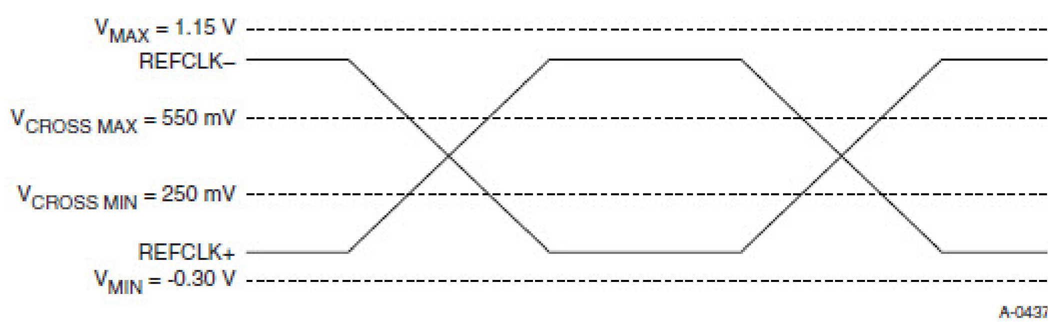


Figure 15 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures memory depth and sampling rate as per the data rate.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ minimum voltage using **V min** measurement.
6 Measures the RefClk- minimum voltage using **V min** measurement.
7 Compares the RefClk+ minimum voltage and the RefClk- minimum voltage.
8 Reports the smallest value (worst value) as the Absolute Min Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{MIN} < -0.3V$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

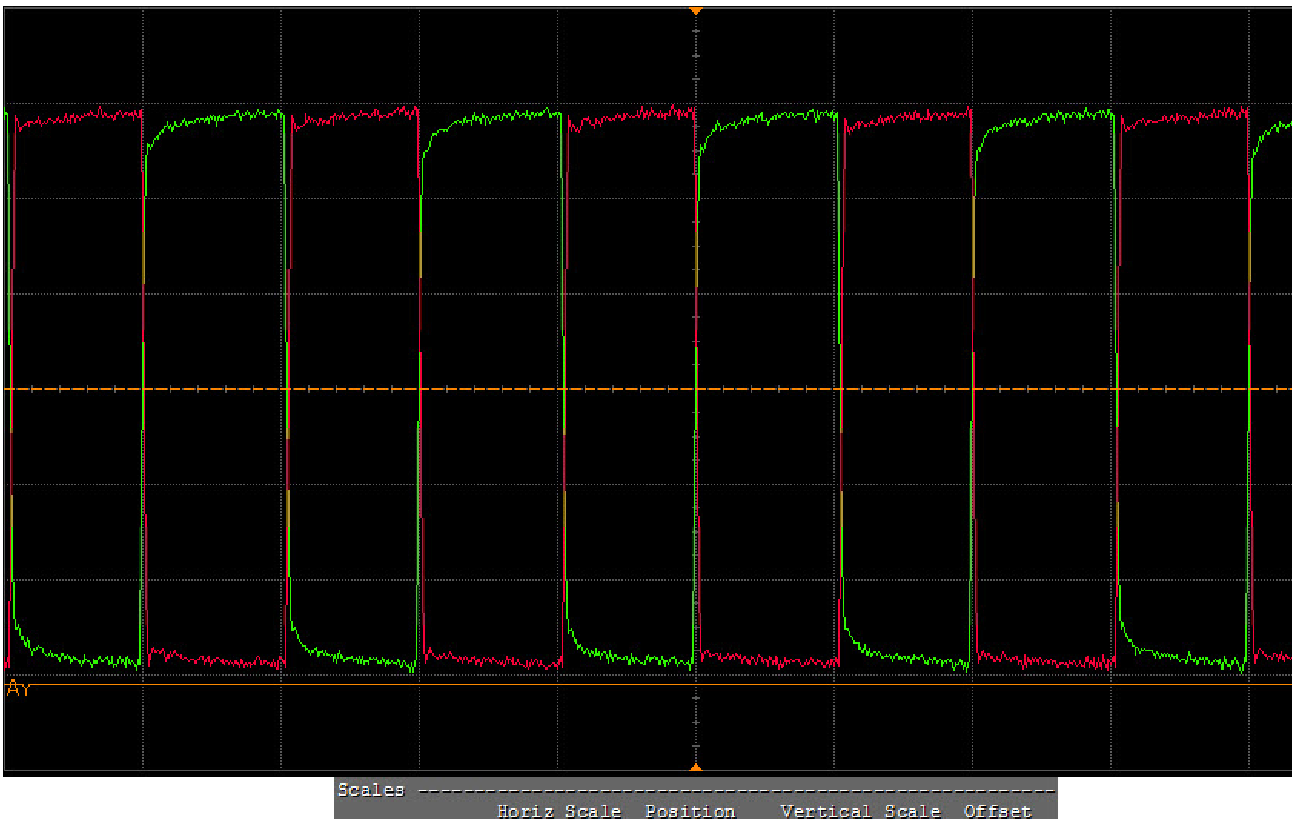


Figure 16 Reference Image for Absolute Min Input Voltage Test

Rise-Fall Matching Test

The rise-fall matching test matching applies to rising edge rate for RefClk+ and falling edge rate for RefClk-. It is measured using +/-75 mV window centered on the median cross point where RefClk+ rising meets RefClk- falling. The median cross point is used to calculate the voltage thresholds and oscilloscope is used to calculate the edge rate calculations. The rise edge rate of RefClk+ should be compared to the fall edge rate of RefClk-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	20%

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8-67.

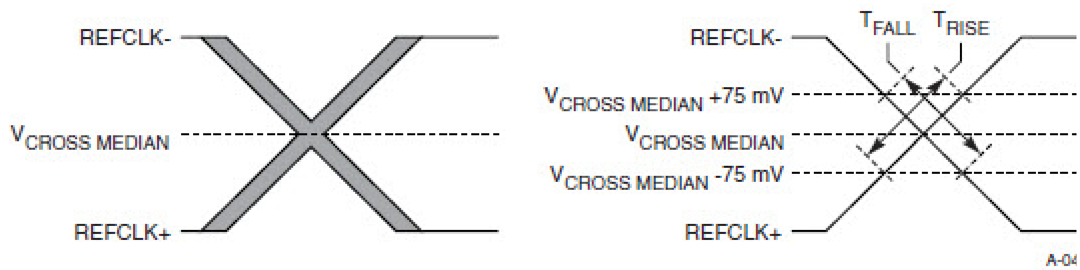


Figure 17 Single-Ended Measurement Points for Rise and Fall Time Matching

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures memory depth and sampling rate as per the data rate.
2. Fits and displays all sample data on screen.
3. Sets the Middle Threshold by ([maximum crossing rising edge value +minimum crossing rising edge value] / 2).
4. Sets the **Upper Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** + 75mV].
5. Sets the **Lower Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** - 75mV].
6. Measures RefClk+ rise time using **Rise time** measurement.
7. Measures the RefClk- fall time using **Fall time** measurement.
8. Finds the slowest edge between RefClk+ rise time and RefClk- fall time.
9. Computes the Rise-Fall matching value as follows:

$$.\text{Rise-Fall Matching} = \frac{Abs|\text{RefClk+ rise time} - \text{RefClk- fall time}|}{\text{Slowest Edge Value} \times 100}$$

10. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of `Rise-Fall Matching < 20%.`

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

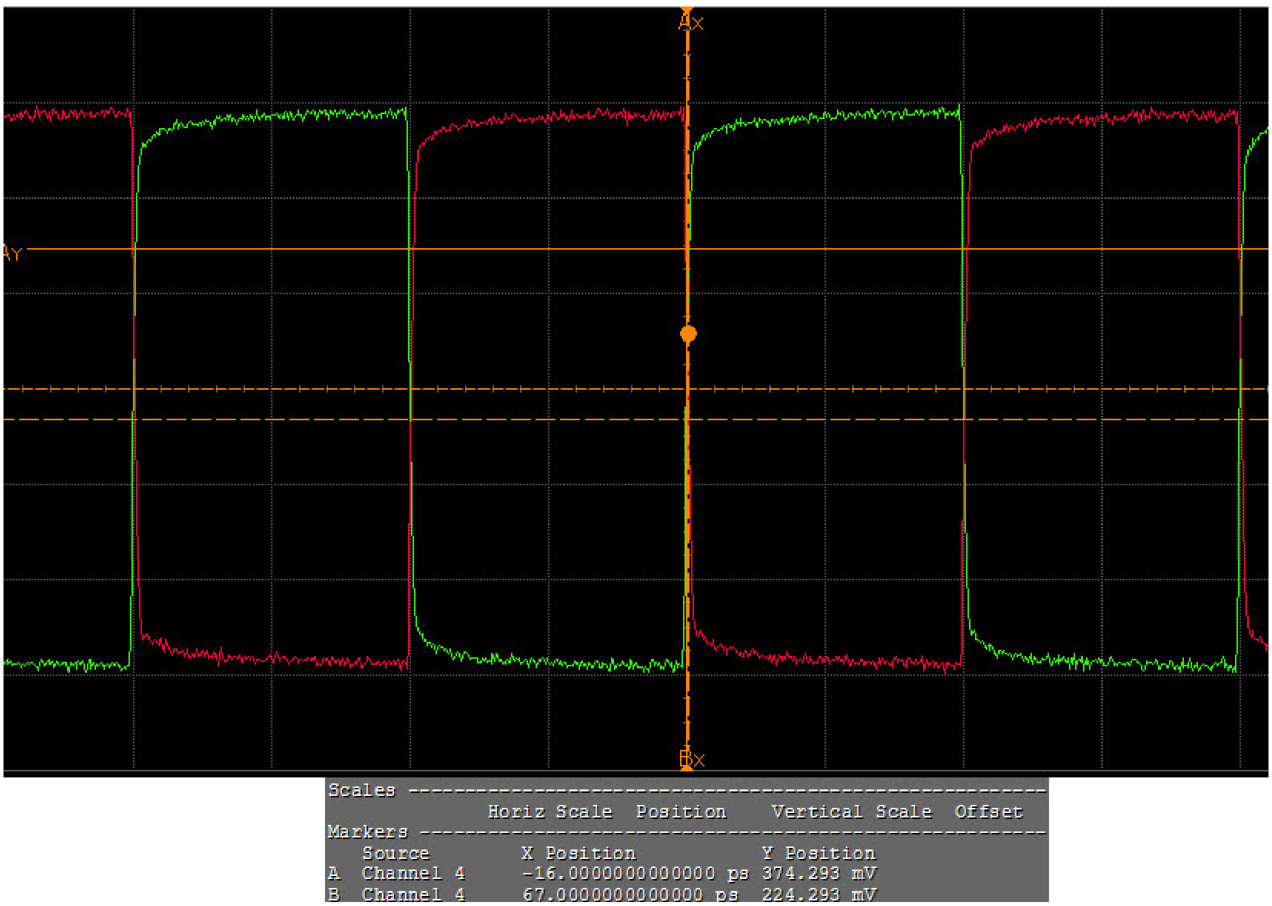


Figure 18 Reference Image for Rise-Fall Matching

RefClk SSC Frequency Range (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters).

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 3 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal frequency is ~ 100 MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Sets the scale and offset of the input channels to their optimum values.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk SSC Deviation (Common Clk) Test

This test verifies that the measured reference clock SSC deviation is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters).

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 4 SSC Deviation Test Details

Symbol	Description	Min/Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.03% /-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal frequency is ~ 100 MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min, and Period_average.
9. Computes SSC deviation Max(%) = ((1 / 100MHz) - SSC's Minimum UI) / (1 / 100MHz) * 100
10. Computes SSC deviation Min(%) = ((1 / 100MHz) - SSC's Maximum UI) / (1 / 100MHz) * 100
11. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk Max SSC df/dt (Slew Rate) (Common Clk) Test

This test verifies that the reference clock maximum SSC df/dt is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 5 RefClk Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a Generates a differential plot (x_n - x_{n-1}).
   b The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

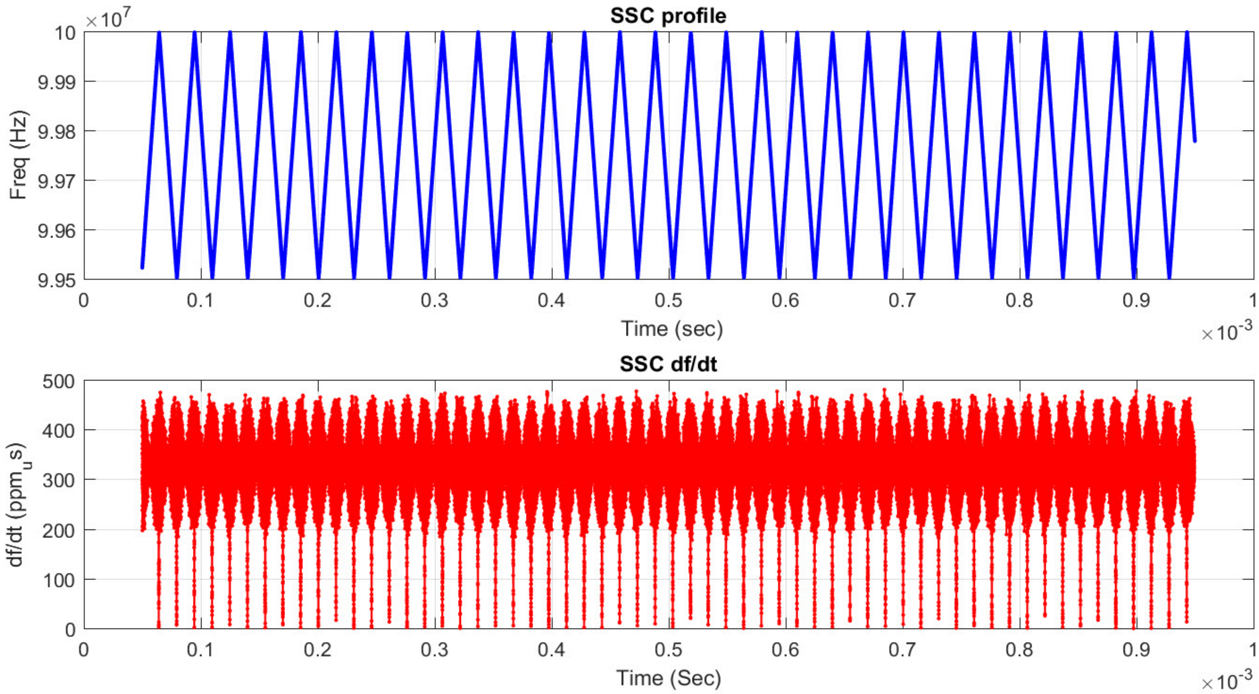


Figure 19 Maximum SSC Slew Rate

Part III
PCI-Express Gen5 2.5 GT/s Tests

KEYSIGHT TECHNOLOGIES

4 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 2.5 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE **It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.**

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

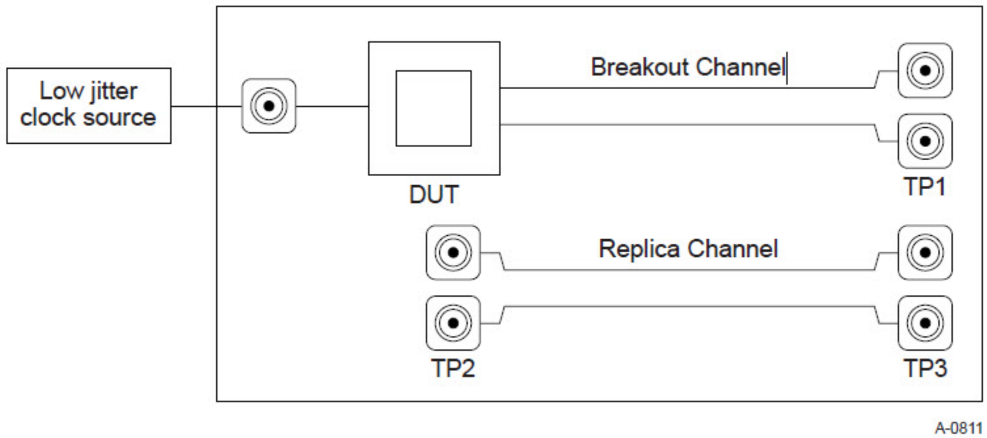


Figure 20 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 2.5 GT/s Tests > Transmitter (Tx) Tests**.

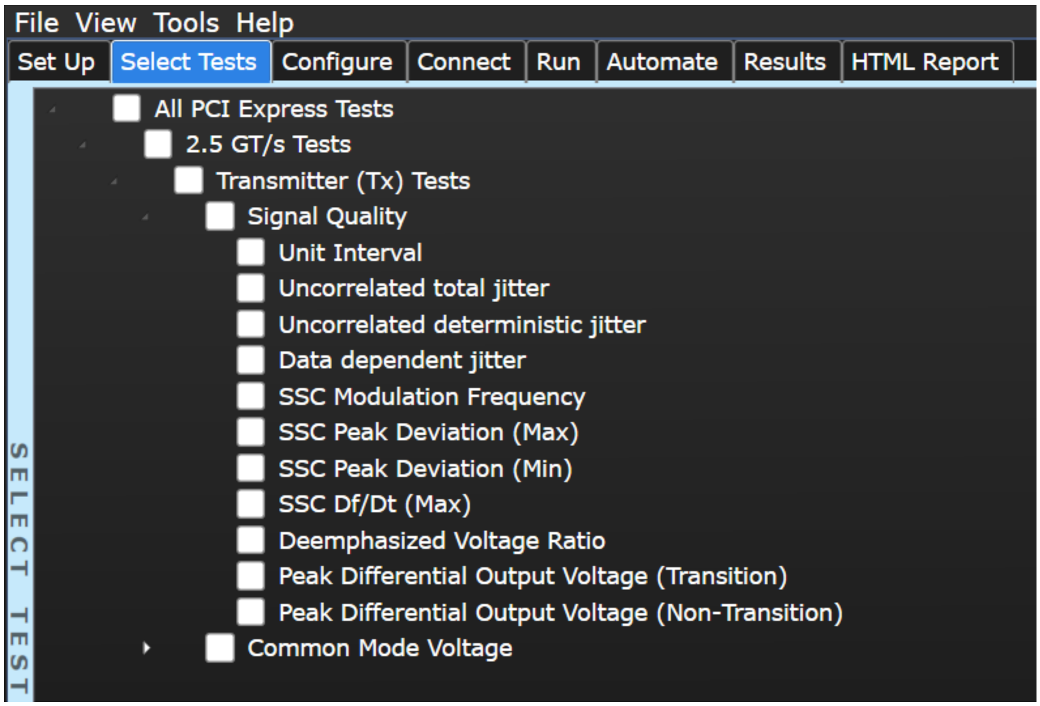


Figure 21 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 6 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
  a Selects **Unit Interval** as data measurement analysis unit.
  b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

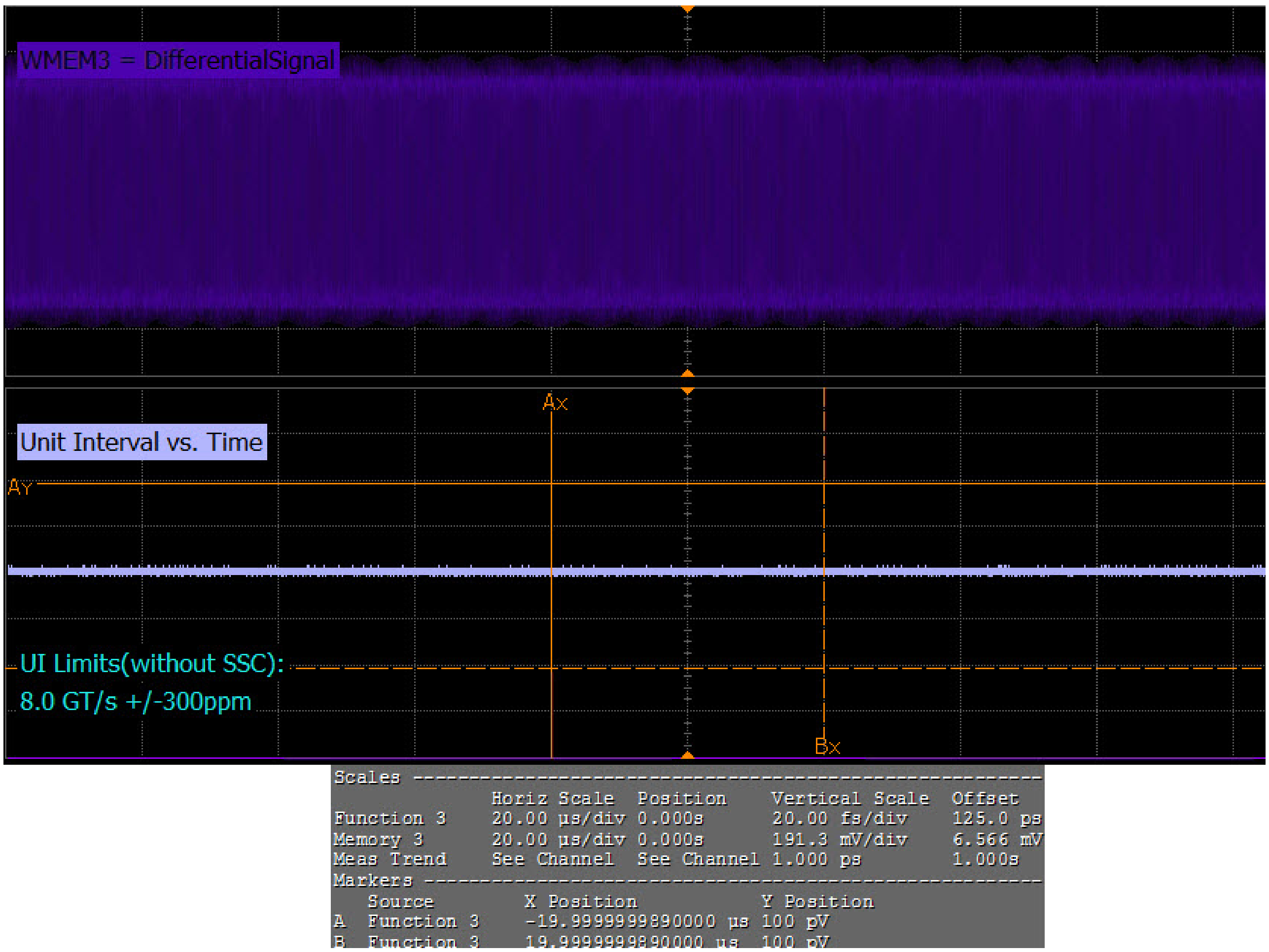


Figure 22 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 7 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	100.00 ps PP at 10^{-12}

Test Definition Notes from the Specification

- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.
- See Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$)) of the PCI Express Base Specification, Revision 5.0 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 8 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	100 ps PP

Test Definition Notes from the Specification

- See Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$)) of the PCI Express Base Specification, Rev 5.0 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, T_{TX-DDJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 (Data Dependent Jitter) is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-DC-}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 9 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground. See also the $I_{TX-SHORT}$.
- $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

a Enables and displays common mode measurements.

b Loads common mode signal to waveform memory.

c Loads and enhance dynamic range D+ signal and D- signal.

d Enables the average common mode measurement.

e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0 as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

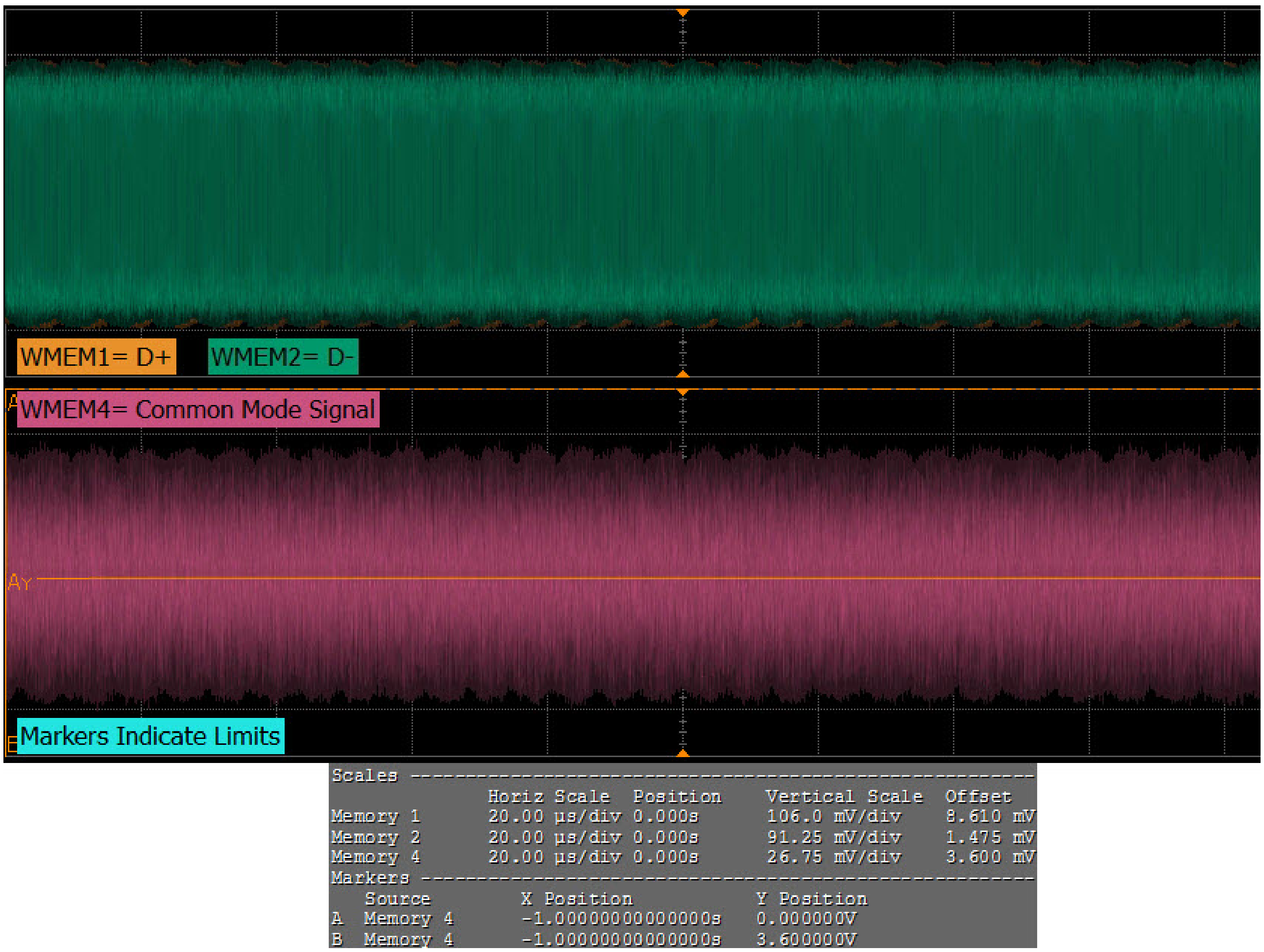


Figure 23 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 1.25 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 10 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $VT_{X-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 1.25 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

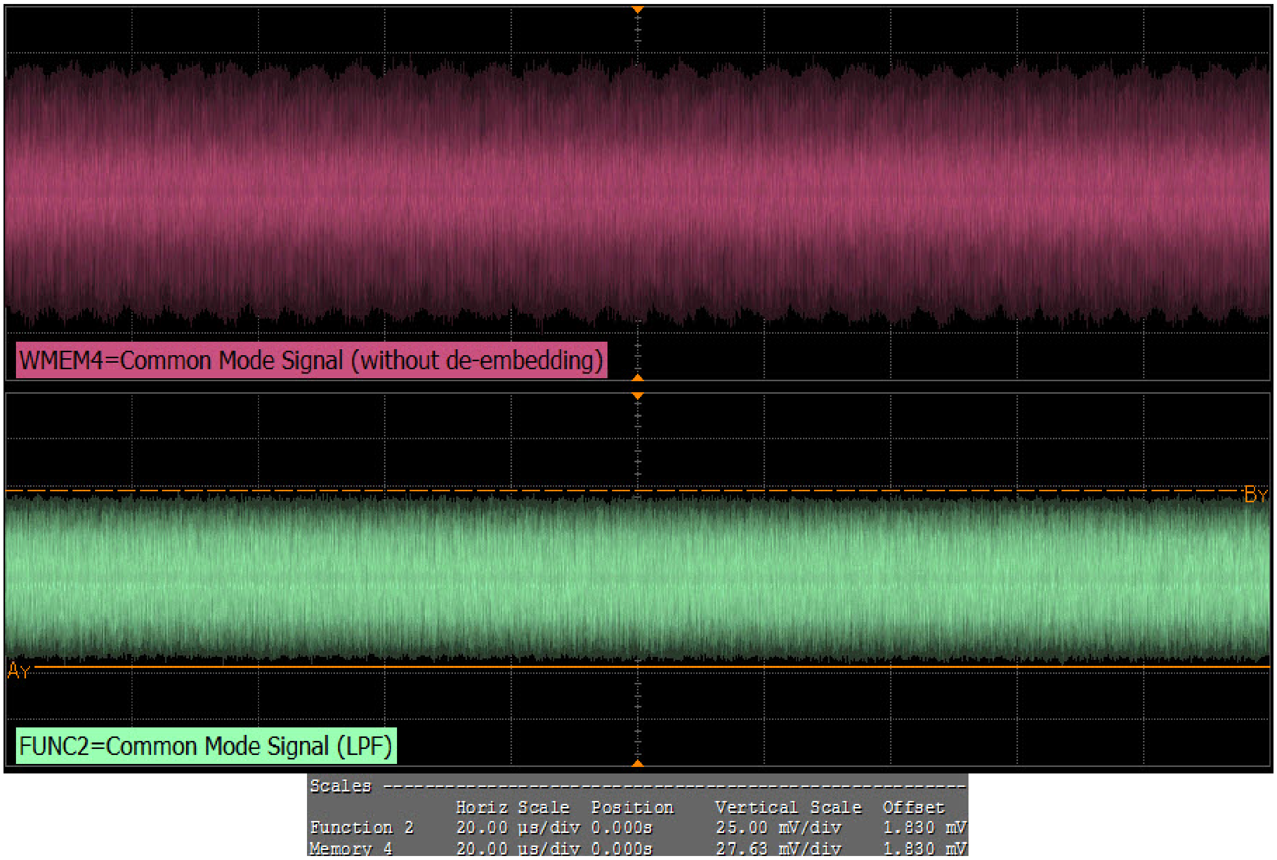


Figure 24 Reference Image for AC-CM voltage (4GHz LPF) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25$ mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 11 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
- DC Common Mode Line Delta
- Average DC value of D+
- Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100$ mV

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT..

Table 12 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

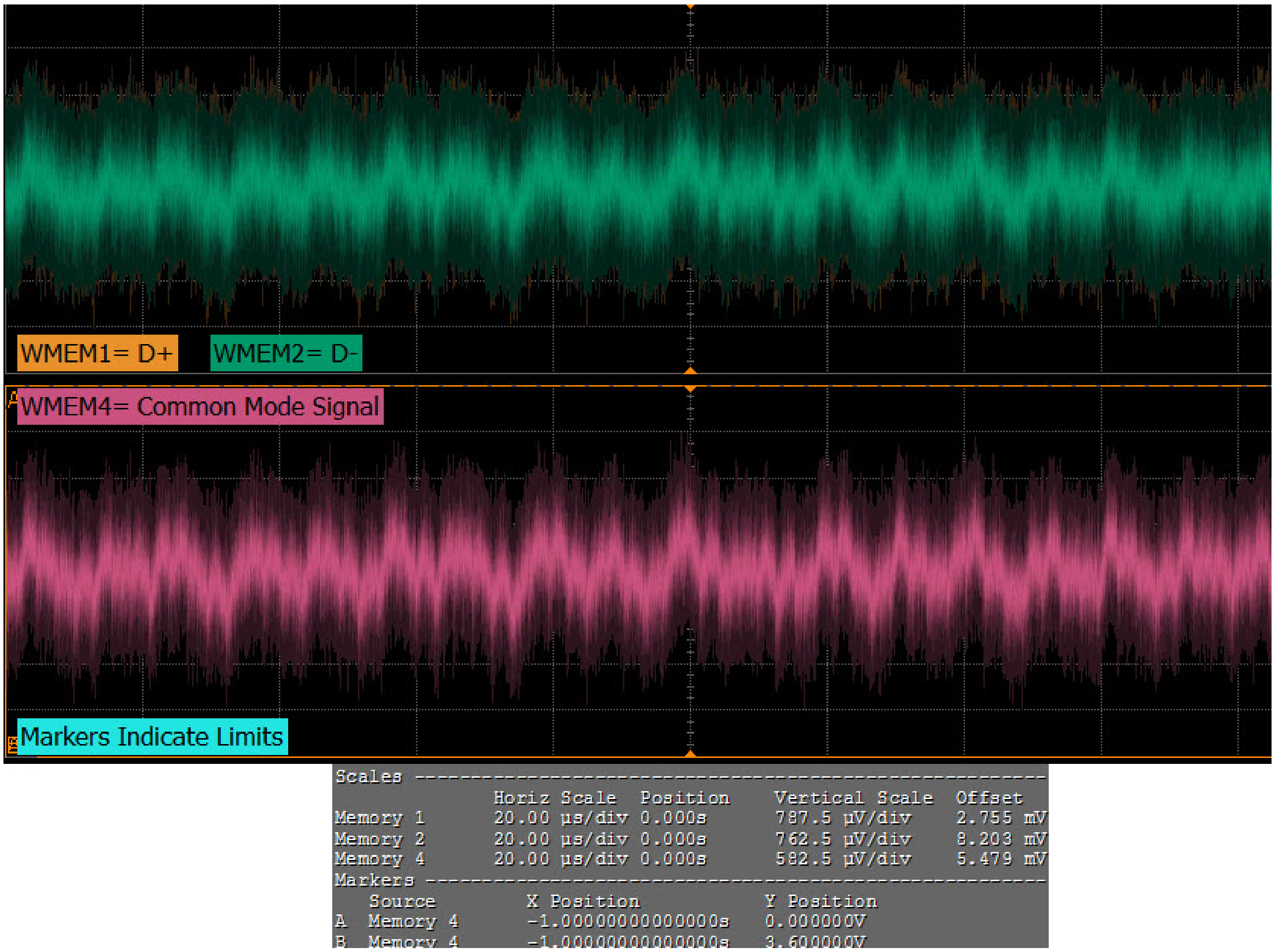


Figure 25 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 13 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 14 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 2.5 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option..
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 15 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 2.5 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 16 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a. Generates a differential plot (x_n - x_{n-1}).
   b. The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

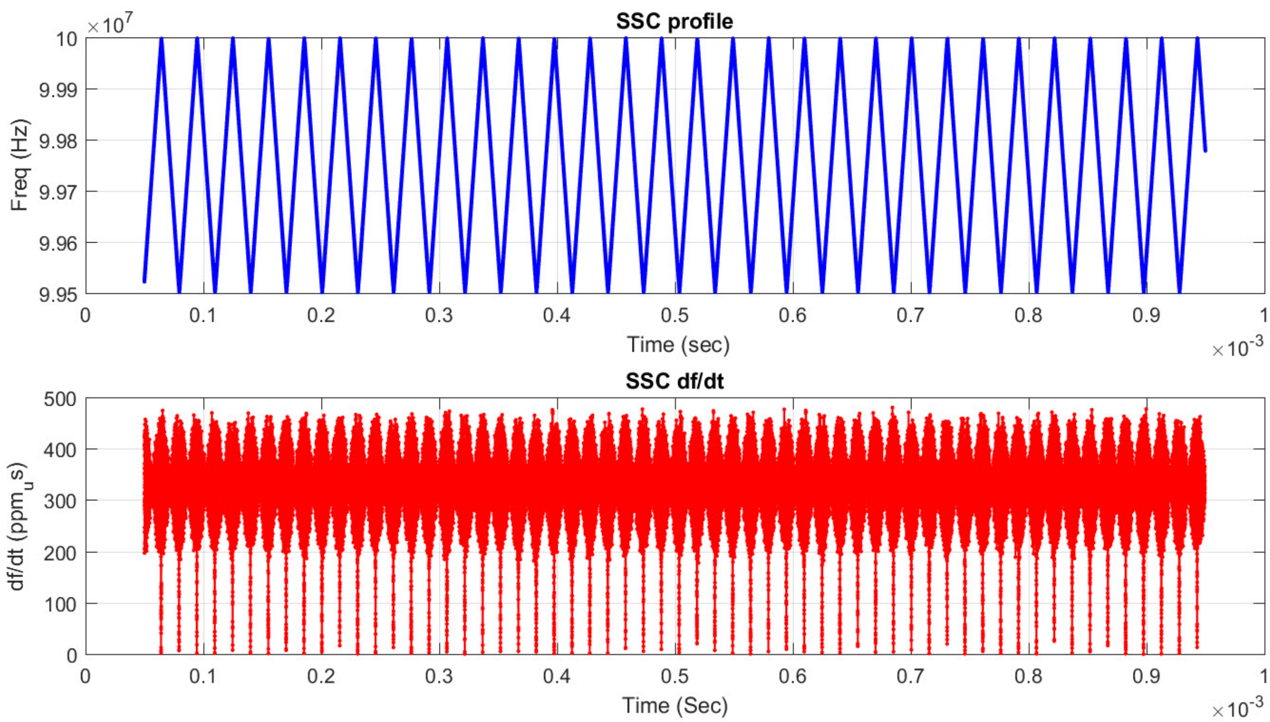


Figure 26 Maximum SSC Slew Rate

Deemphasized Voltage Ratio Test

The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, $V_{TX\text{-}DE\text{-}RATIO} = -20\log10\ (V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 17 Deemphasized Voltage Ratio (-3.5 dB) Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DE\text{-}RATIO}$	Deemphasized Voltage Ratio	-4.500 dB	-2.500 dB

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   - *a* Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with Damping Factor of 0.707.
   - *b* Sets the value of **Nominal Data Rate** as **2.5 GT/s.**
   - *c* Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s.**
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and bases.
7. Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.
8. Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.
9. Calculates de-emphasis ratio using the following formula:

   De-emphasis ratio $= -20*\log10(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$

10. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the transition eye diagram data from the SigTest tools as $V_{TX-DIFF-PP}$.

2 Extracts the non-transition eye diagram data from the SigTest tools as $V_{TX-DE-EMPH-PP}$.

3 Calculates de-emphasis ratio using the following formula:

De-emphasis ratio: $-20*\log_{10}(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$

4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$

Where,

‘i’ is the index of all waveform values.

‘V_{DIFF}’ is the differential voltage signal.

The **Peak Differential Input Voltage** test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the standard specifications.

$V_{RX\text{-}DIFFp\text{-}p} = 2*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 18 Peak Differential Output Voltage (Transition) Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.800 V	1.20 V

Understanding the Test Flow - Using Infiniium Measurement Method

> **NOTE** This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   - *a* Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
   - *b* Sets the value of **Nominal Data Rate** as **2.5 GT/s.**
   - *c* Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the transition bits eye top and bases.
5. Finds the differential value between the transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the transition eye diagram data from the SigTest tools.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTest tools.
3. Compares the measured peak differential output/input voltage (transition) value to the compliance test limits.
4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}, Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 19 Peak Differential Output Voltage (Non-Transition) Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.4765 V	1.20 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

  a Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.

  b Sets the value of **Nominal Data Rate** as **2.5 GT/s**.

  c Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s**.

3 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and bases.

5 Finds the differential value between the non-transition bits eye top and base using **Histogram**.

6 Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the non-transition eye diagram data from the SigTest tools.
2. Gets largest non-transition amplitude (outer eye), smallest non-transition amplitude (inner eye) test results from SigTest tools.
3. Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.
4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

5 CEM-EndPoint Tests, 2.5 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-EndPoint tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB, and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test)

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running CEM-EndPoint Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to the **All PCI Express Tests > 2.5 GT/s Tests > CEM EndPoint Tests**.

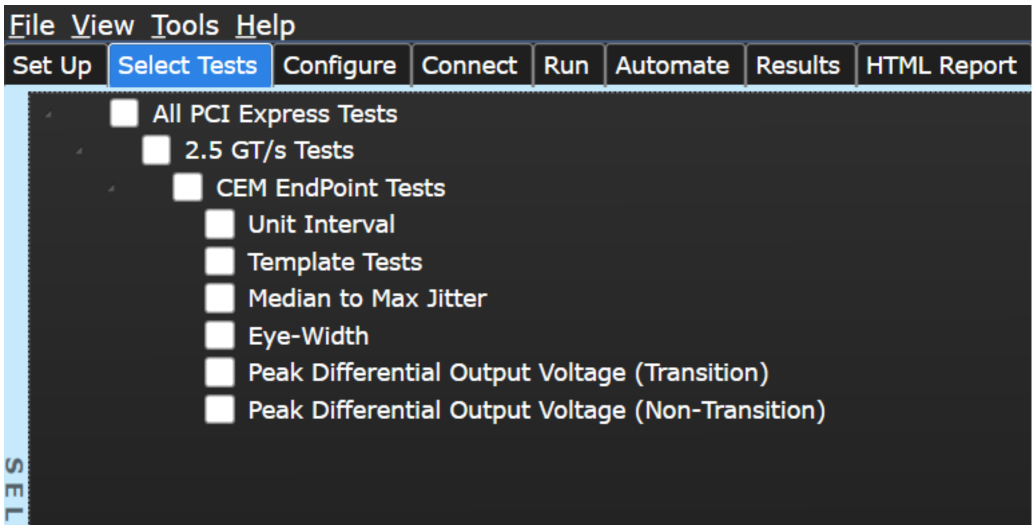


Figure 27 Selecting CEM EndPoint Tests

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This is an informative test only.

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 20 **Unit Interval Test Details**

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations.
- No test load is necessarily associated with this value.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 4.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
  a Selects **Unit Interval** as data measurement analysis unit.
  b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 1.0a as `399.88 ps < UI < 400.12 ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

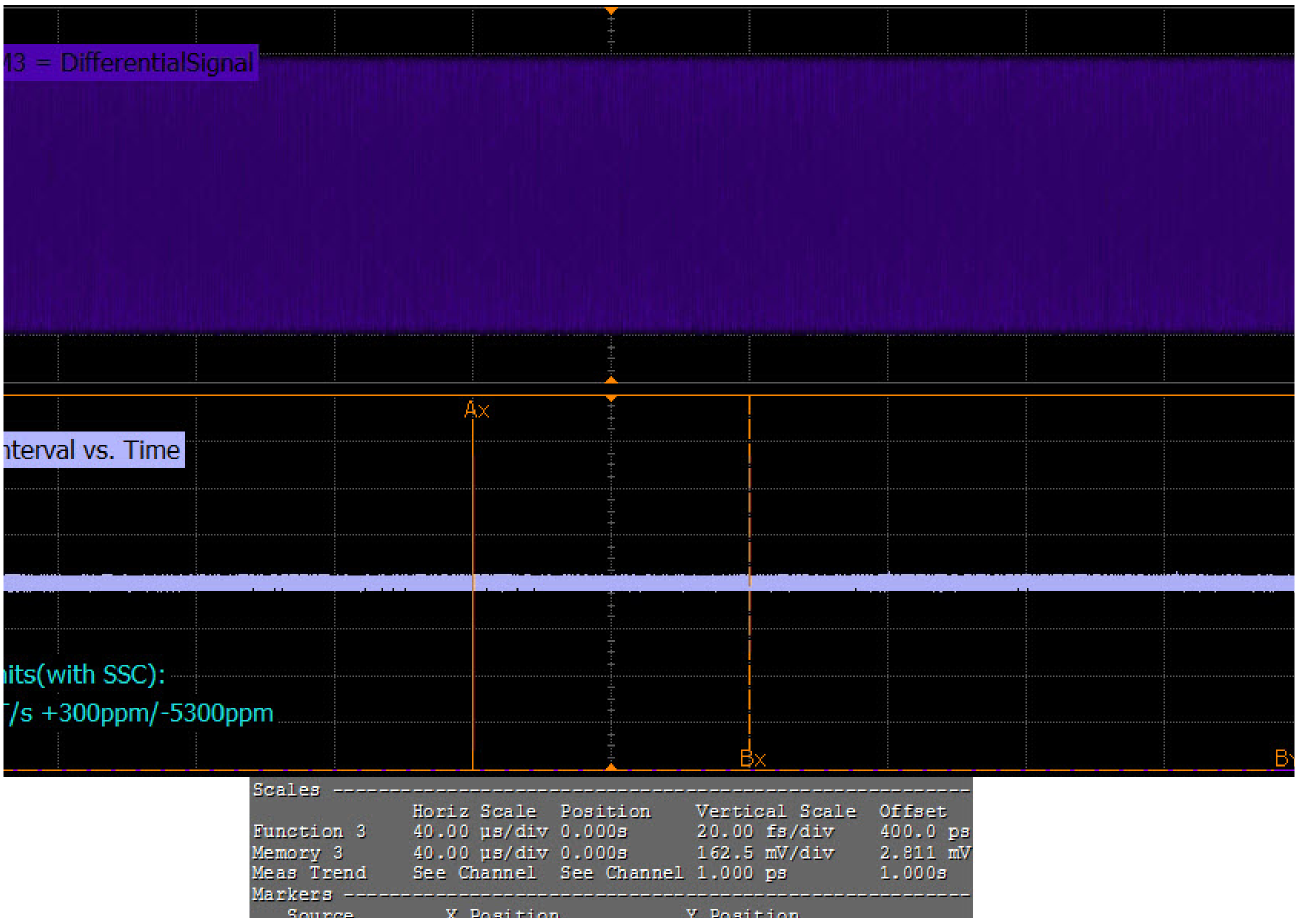


Figure 28 Reference Image for Unit Interval Test

Template Test

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.1, Table 4-9 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-6.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.1, Figure 4-7, Table 4-9 is used as reference to check the compliance of the DUT.

Table 21 Template Test Details

Parameter	Min	Max	Comment
Vtx_A	514 mV	1200	Notes 1, 2, 5
Vtx_{A_d}	360 mV	1200	Notes 1, 2, 5
Ttx_A	287 ps	N/A	Notes 1, 3, 5

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.

4 $T_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12}.

5 The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture, PHY Test Specification..

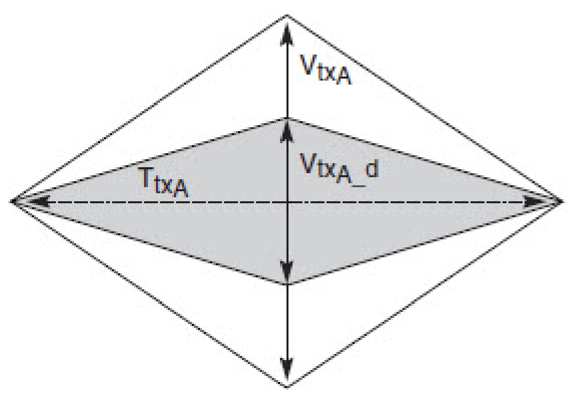


Figure 29 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 4.0. To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 115 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

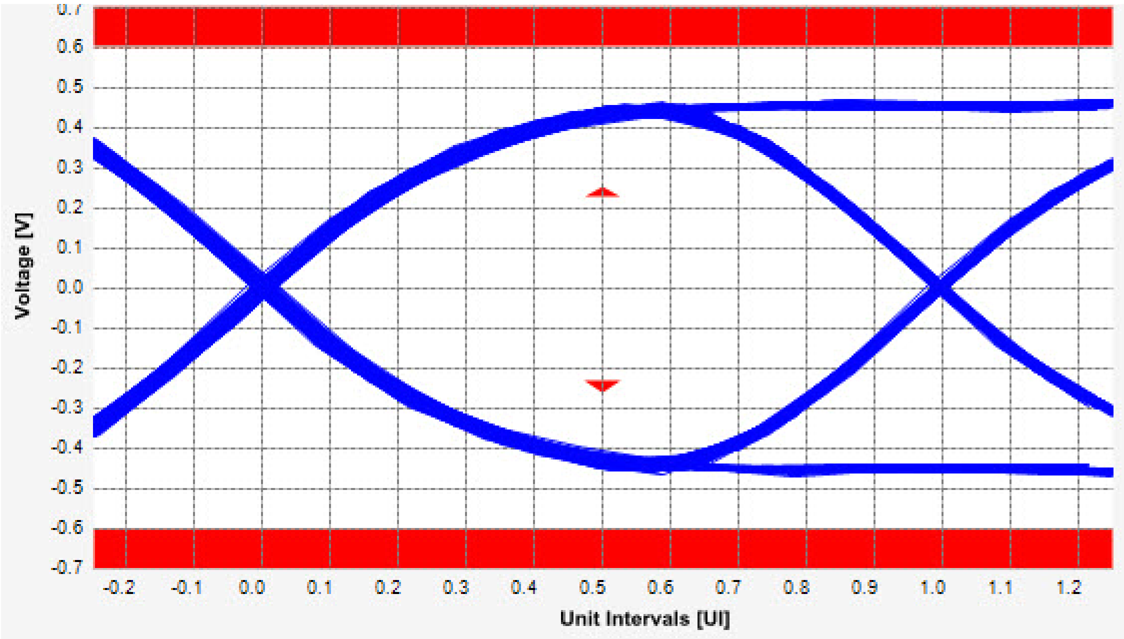


Figure 30 Reference Image for Template (Transition) Test

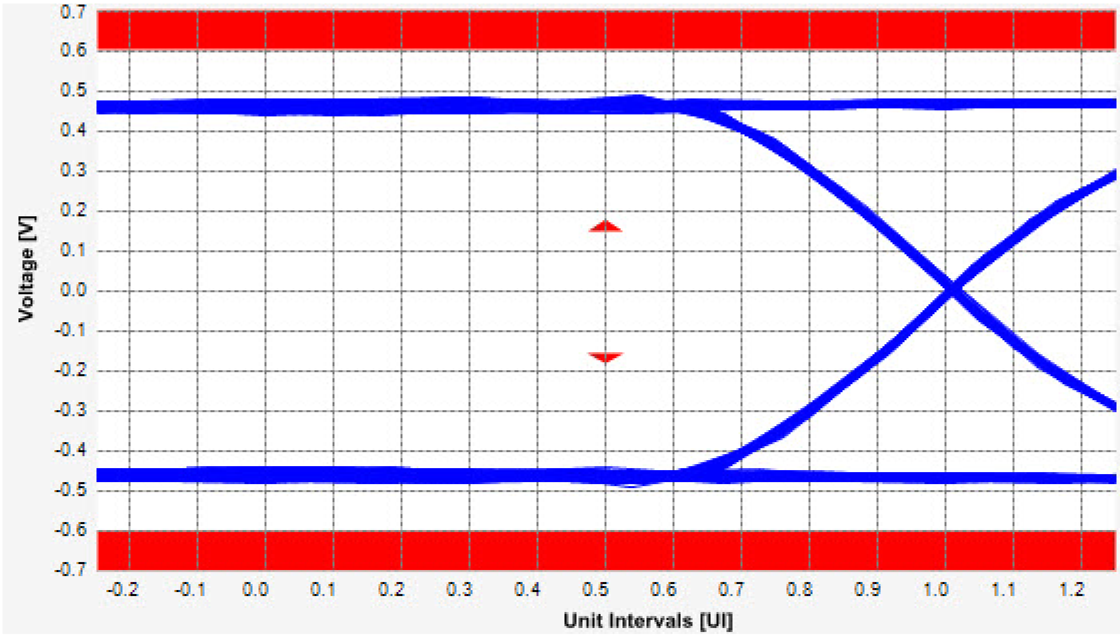


Figure 31 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median. The limit for the median to max jitter is calculated by the following equation:

$$\text{Median to max jitter} = (1\ UI - \text{Eye Width})/2$$

Where,

1 UI = 400ps

Eye Width = 237ps

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.1, Figure 4-7, Table 4-9 is used as reference to check the compliance of the DUT.

Table 22 Median to Max Jitter Test Details

Symbol	Max
$T_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	56.5 ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.
- $T_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12}.
- The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture, PHY Test Specification.

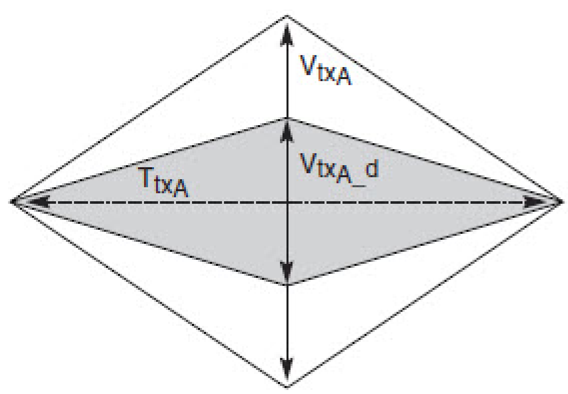


Figure 32 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 115 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 2.5 GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.
2 Computes the median to max jitter using the following formula:

$$\text{Median to max jitter} = \text{Maximum peak to peak jitter after filter} / 2$$

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a as 56.50 ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

Eye-Width = [Mean Unit Interval] - [Peak to Peak Jitter]

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.1, Table 4-9 is used as reference to check the compliance of the DUT.

Table 23 Median to Max Jitter Test Details

Symbol	Min
T_{TXA}	287 ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.
- T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.
- The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture, PHY Test Specification.

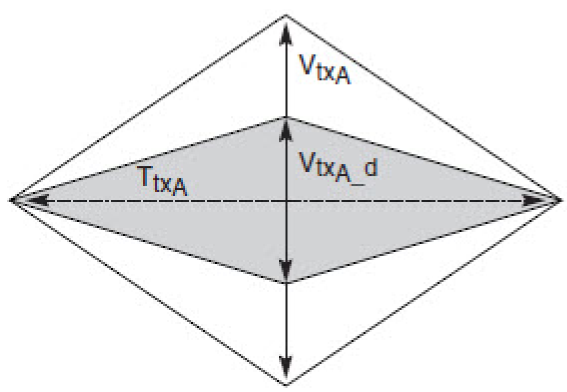


Figure 33 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 115 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:
Device: PCIE 5.0
Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 1.0a.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits as T_{txA} >287 ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage Test (Transition)

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.1, Figure 4-7, Table 4-9 is used as reference to check the compliance of the DUT.

Table 24 Template Test Details

Parameter	Min	Max
Vtx_{A_d}	360 mV	1200 mV

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture, PHY Test Specification.

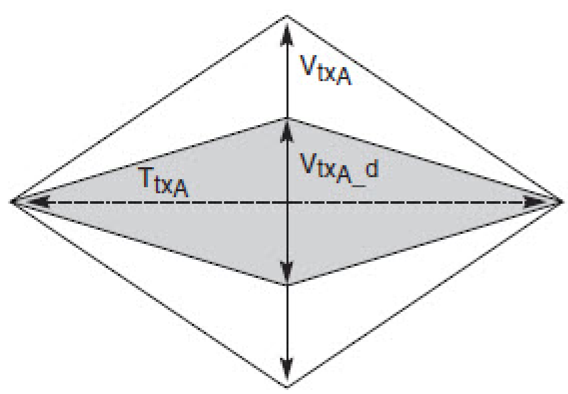


Figure 34 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 115 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 2.5 GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

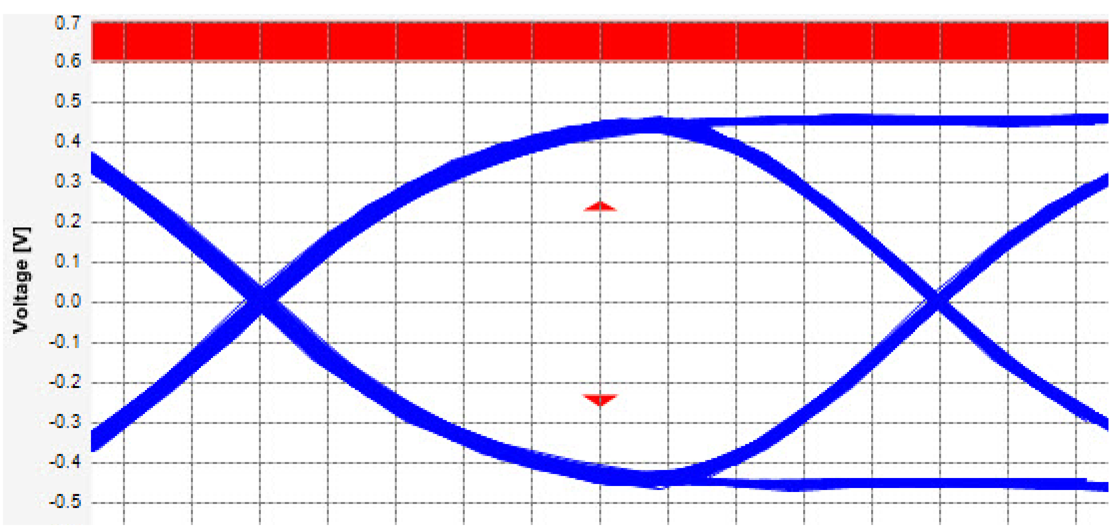


Figure 35 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage Test (Non-Transition)

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.1, Figure 4-7, Table 4-9 is used as reference to check the compliance of the DUT.

Table 25 Template Test Details

Parameter	Min	Max
$Vtx_{A\_}d$	360 mV	1200 mV

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture, PHY Test Specification.

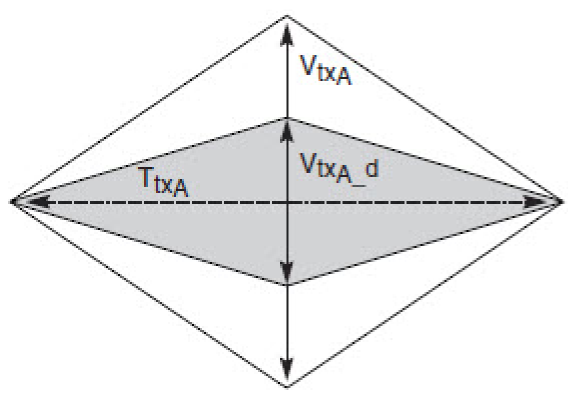


Figure 36 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 115 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 2.5 GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

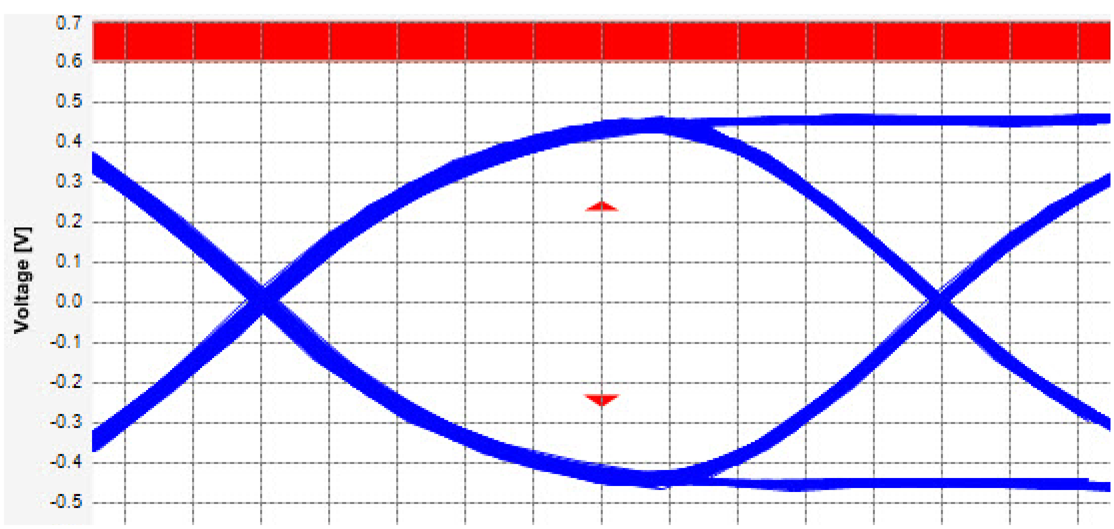


Figure 37 Reference Image for Peak Differential Output Voltage Test

6 CEM-RootComplex Tests, 2.5 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-RootComplex tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Automated Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1. With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.
   The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.
2. Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.
3. Connect cables up as follows:
   a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR
   b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running CEM-RootComplex Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 2.5 GT/s Tests > CEM RootComplex Tests**.

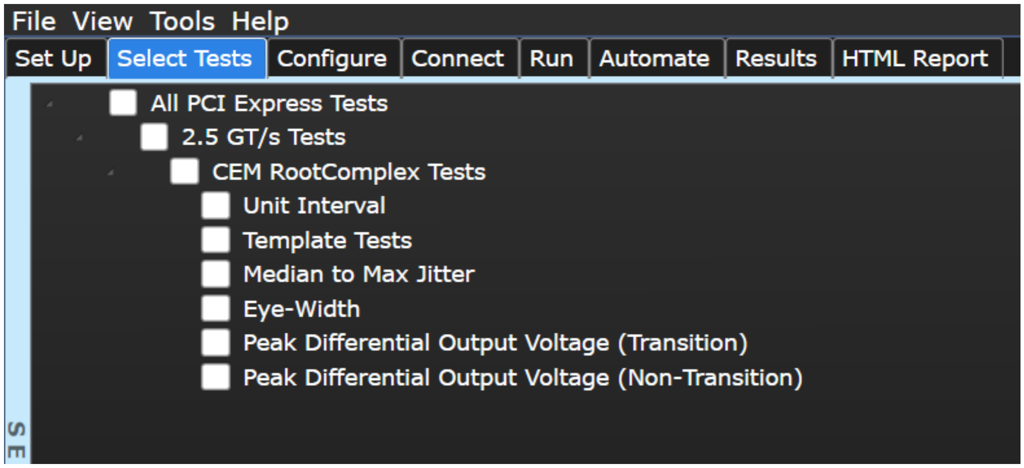


Figure 38 Selecting System Board (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window is as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 26 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	TBD

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 4.0. To execute the test, follow the procedure in** "Running CEM-RootComplex Tests" on page 133 **and select Unit Interval.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

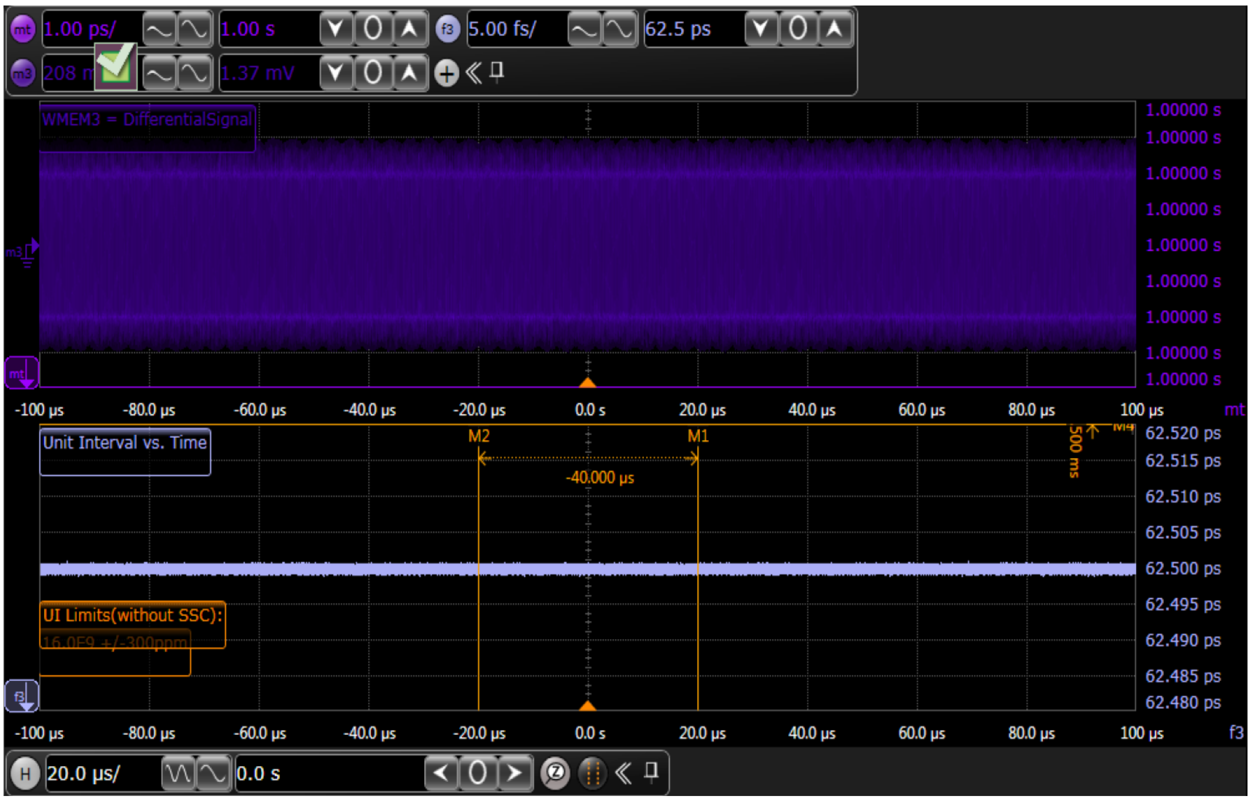


Figure 39 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in the PCI Express Card Electromechanical Specification (CEM).

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Figure 4-9, Table 4-25 is used as reference to check the compliance of the DUT.

Table 27 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	274 mV	1200 mV	Notes 1, 2, 4
V_{TXS_d}	253 mV	1200 mV	Notes 1, 2, 4
T_{TXS}	246 ps	N/A	Notes 1, 3, 4

Test Definition Notes from the Specification

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 233 ps for simulation purposes at BER 10^{-12}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

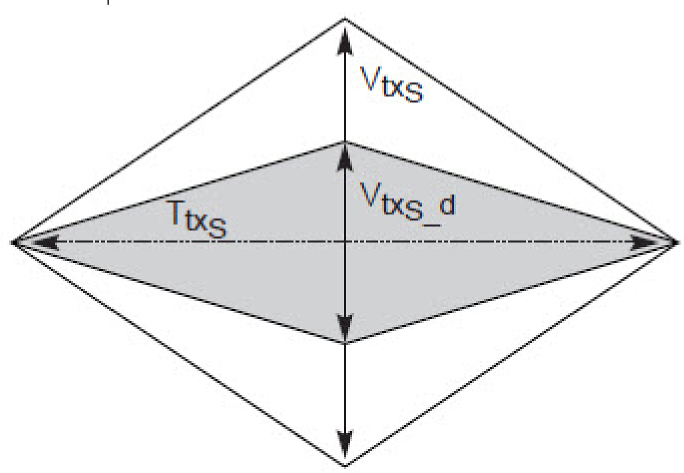


Figure 40 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 4.0. To execute the test, follow the procedure in** "Running CEM-RootComplex Tests" **on page 133 and select Template Tests.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 4.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

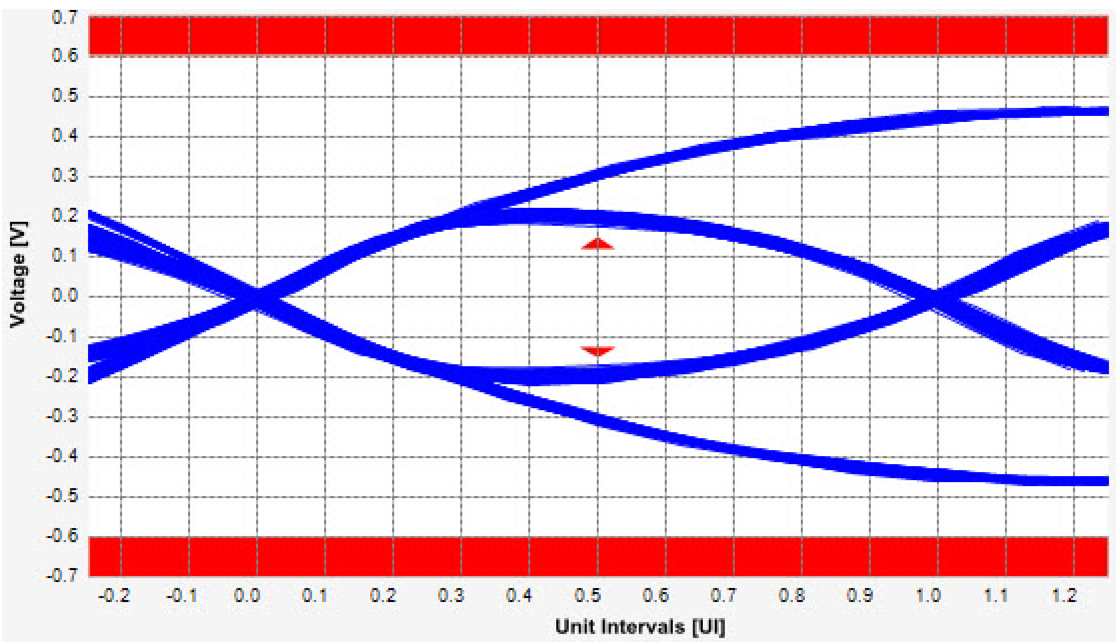


Figure 41 Reference Image for Template (Transition) Test

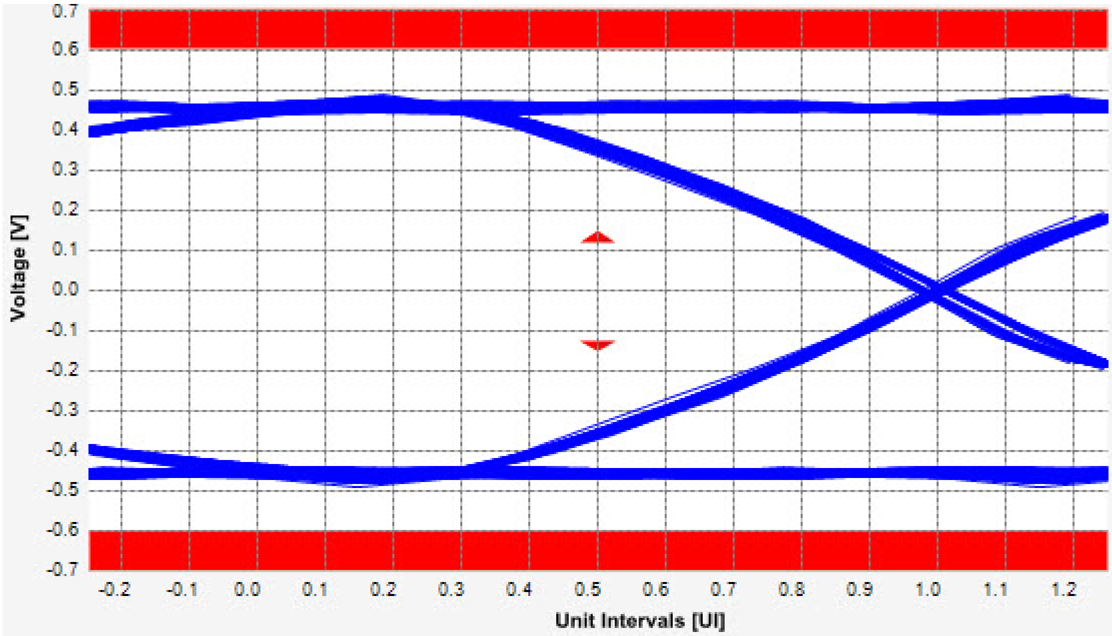


Figure 42 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median. The limit for the median to max jitter is calculated by the following equation:

$$\text{Median to max jitter} = (1\ UI - \text{Eye Width})/2$$

Where,

1 UI = 400ps

Eye Width = 183ps

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Table 4-25 is used as reference to check the compliance of the DUT.

Table 28 Template Test Details

Symbol	Min	Max	Comments
$T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	N/A	77 ps	Notes 1, 2, 3

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 $T_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum time delta between the jitter median and the maximum deviation from the median. The sample size for this measurement

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification

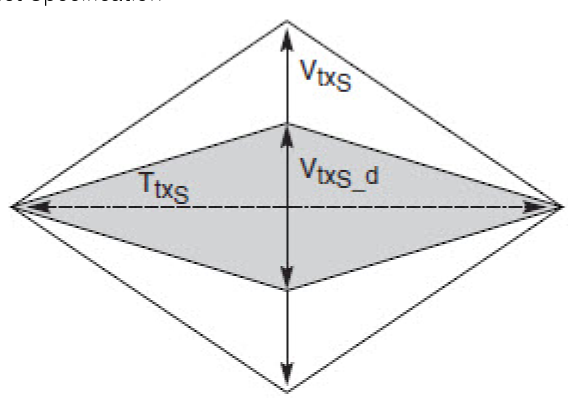


Figure 43 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 133 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 2.5 GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.
2 Computes the median to max jitter using the following formula:

$$\text{Median to max jitter} = \text{Maximum peak to peak jitter after filter} / 2$$

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a as 77 ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye - width = [\boldsymbol{M}eanUnitInterval] - [TotalJitteratBER - 12]$$

System Board must meet the **System Board Transmitter Path Compliance Eye** Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Table 4-25 is used as reference to check the compliance of the DUT.

Table 29 Eye Width Test Details

Symbol	Min	Max
T_{TXS}	246 ps	N/A

Test Definition Notes from the Specification

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This value can be reduced to 233 ps for simulation purposes at BER $10^{-12.}$
3. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification

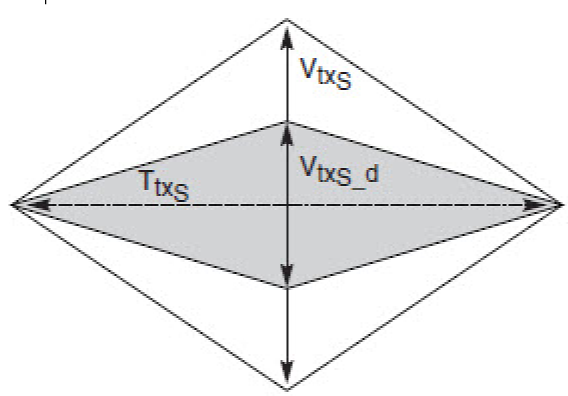


Figure 44 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 133 and select **Eye-Width.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 16.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 4.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements specified in section 4.8.13 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Table 4-25 is used as reference to check the compliance of the DUT.

Table 30 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200 mV

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages.

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification

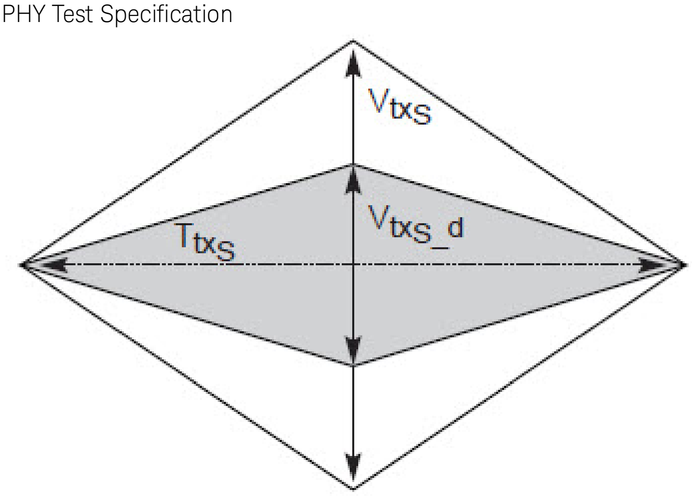


Figure 45 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 133 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 16.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

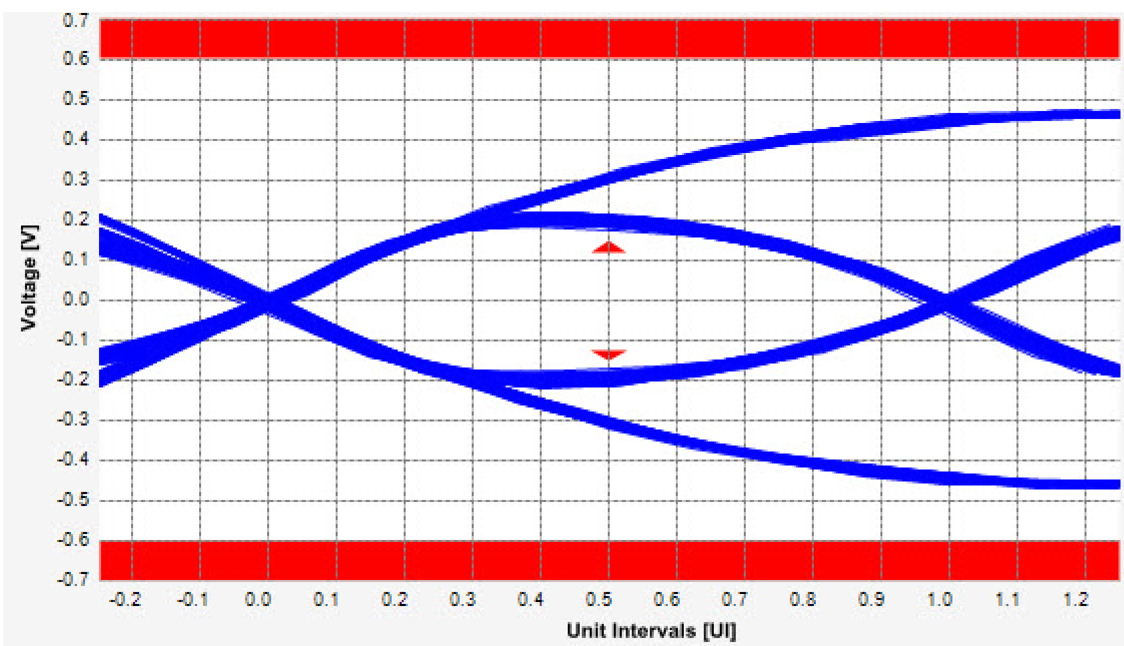


Figure 46 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye** requirements specified in section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Table 4-25 is used as reference to check the compliance of the DUT.

Table 31 Peak Differential Output Voltage (Non Transition) Test Details

Symbol	Min	Max
V_{TXS_d}	253 mV	1200 mV

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 8b/10b (refer to the PCI Express Base Specification) is being transmitted during the test.
- Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages.
- The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the Add-in Card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification

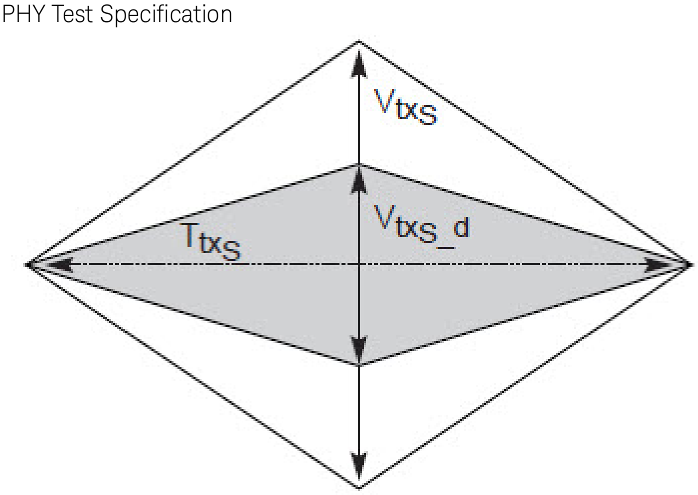


Figure 47 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 133 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 16.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the Online help.

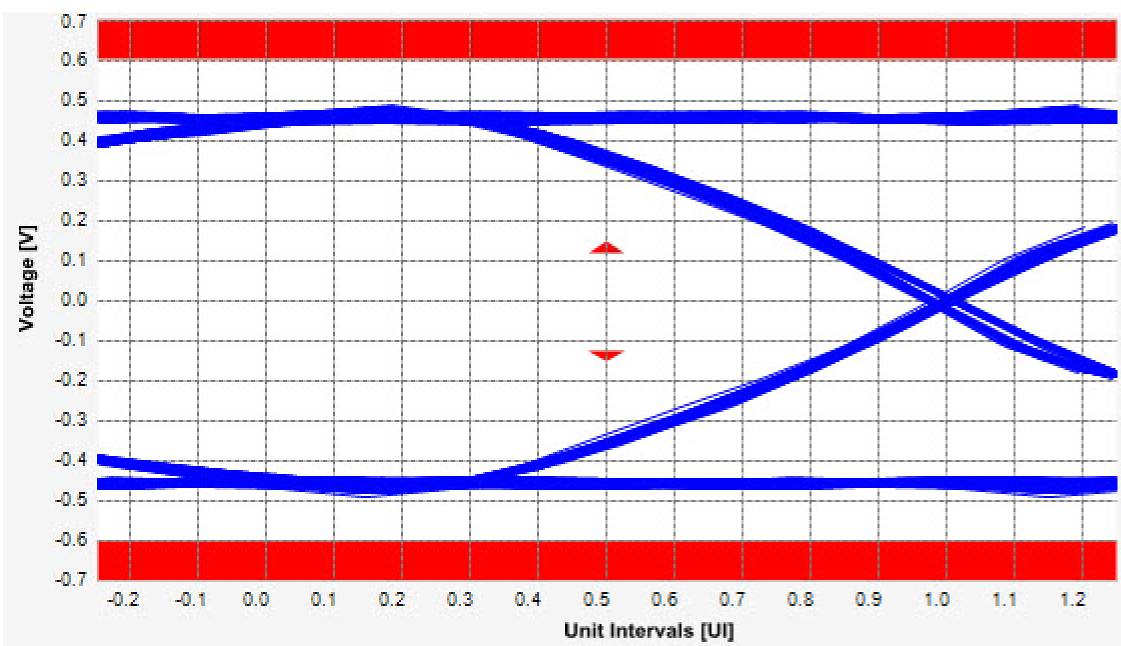


Figure 48 Reference Image for Peak Differential Output Voltage Test

7 Reference Clock Tests, 2.5 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe 5.0 Reference Clock tests at 2.5 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

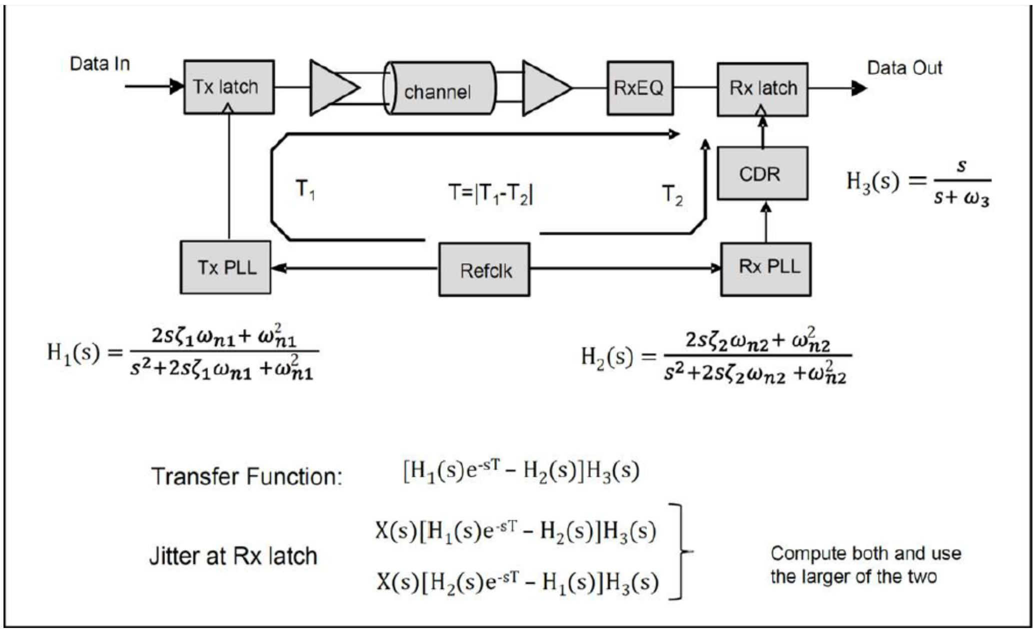
KEYSIGHT TECHNOLOGIES

Reference Clock Architectures

For 5.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 2.5 GT/s

PLL #1, PLL #2	0.01 dB peaking	3.0 dB peaking
BW_{PLL}(min) = 1.5 MHz	ω_{n1}= .336 Mrad/s ζ_1 = 14	ω_{n1}= 5.09 Mrad/s ζ_1 = 0.54
BW_{PLL}(max) = 22 MHz	ω_{n1}= 4.93 Mrad/s ζ_1 = 14	ω_{n1}= 74.68 Mrad/s ζ_1 = 0.54

BW_{CDR}(min) = 1.5 MHz, 1st order	**CDR**

16 combinations

2.5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73

PLL #2	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
$BW_{PLL}(max)$ = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15

$BW_{CDR}(min)$ = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 0.5 MHz	ω_{n1}= .112Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 1.8 MHz	ω_{n1}= .403Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

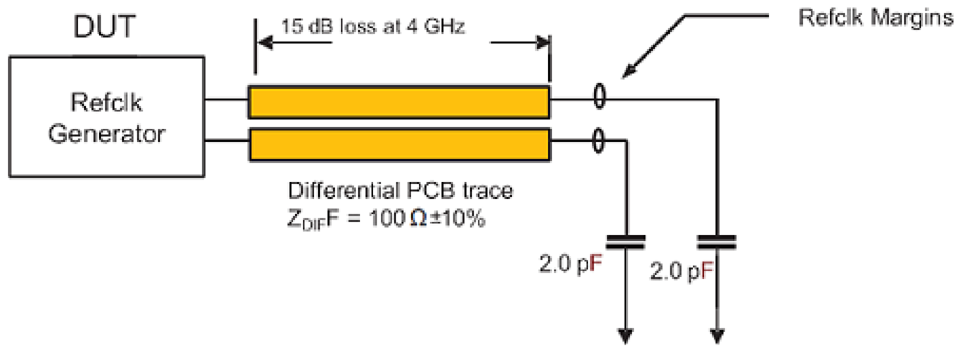


Figure 49 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 2.5 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

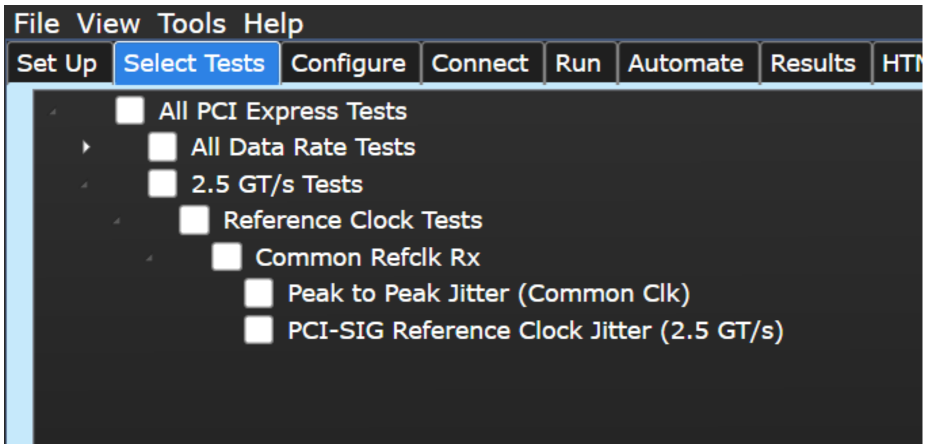


Figure 50 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

Peak to Peak Jitter (Common Clk) Test

This test verifies that the measured peak to peak jitter, $T_{REFCLK-PP-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 32 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-PP-CC}$	Peak to Peak Refclk jitter for common Refclk architecture	86 ps PP

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-73 (Common Refclk Rx Architecture for all Data Rates Except 32.0 GT/s); section 8.6.6 of PCI Express Base Specification Revision 5.0.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitter.
11 Reports filtered peak-peak jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

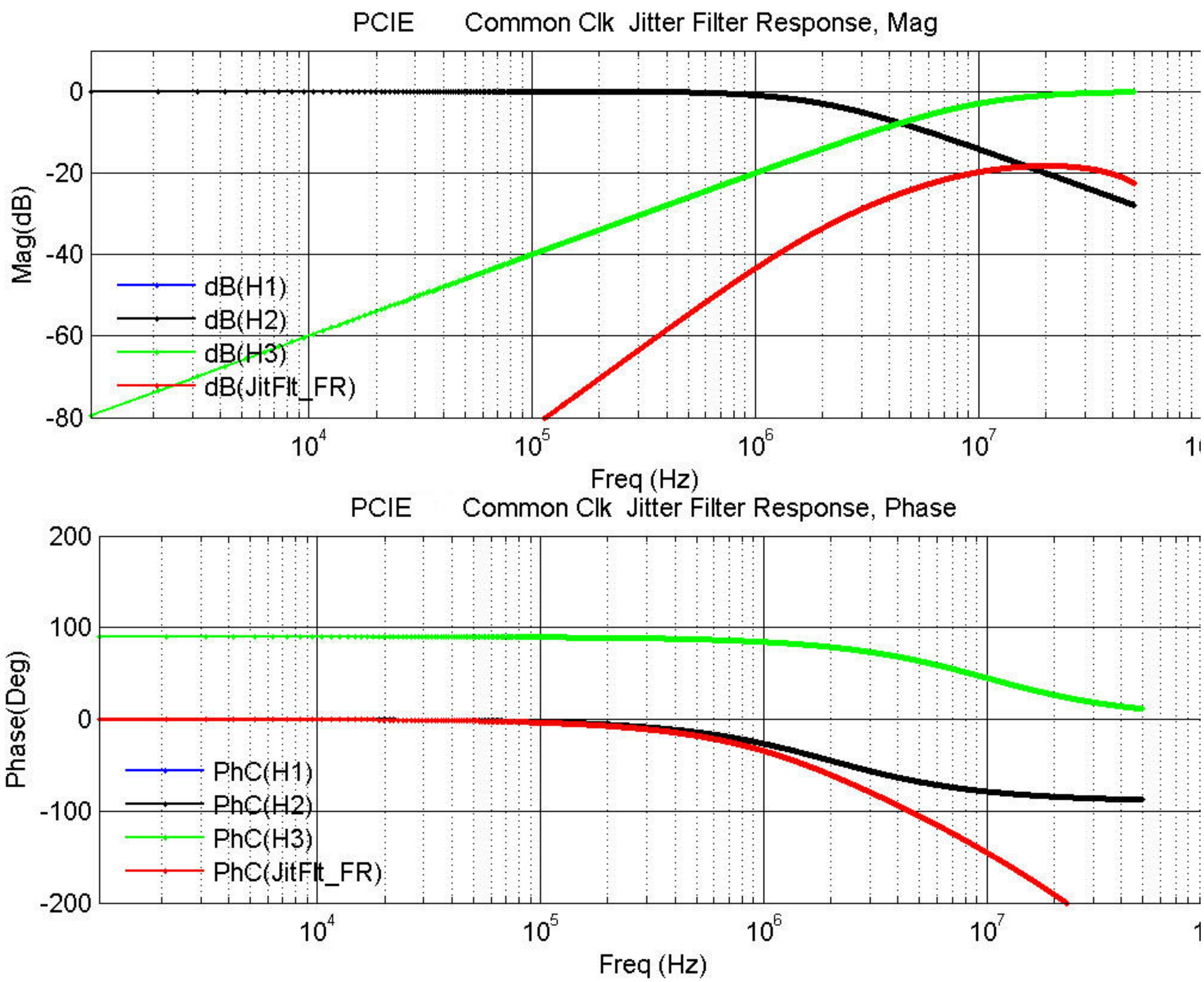


Figure 51 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

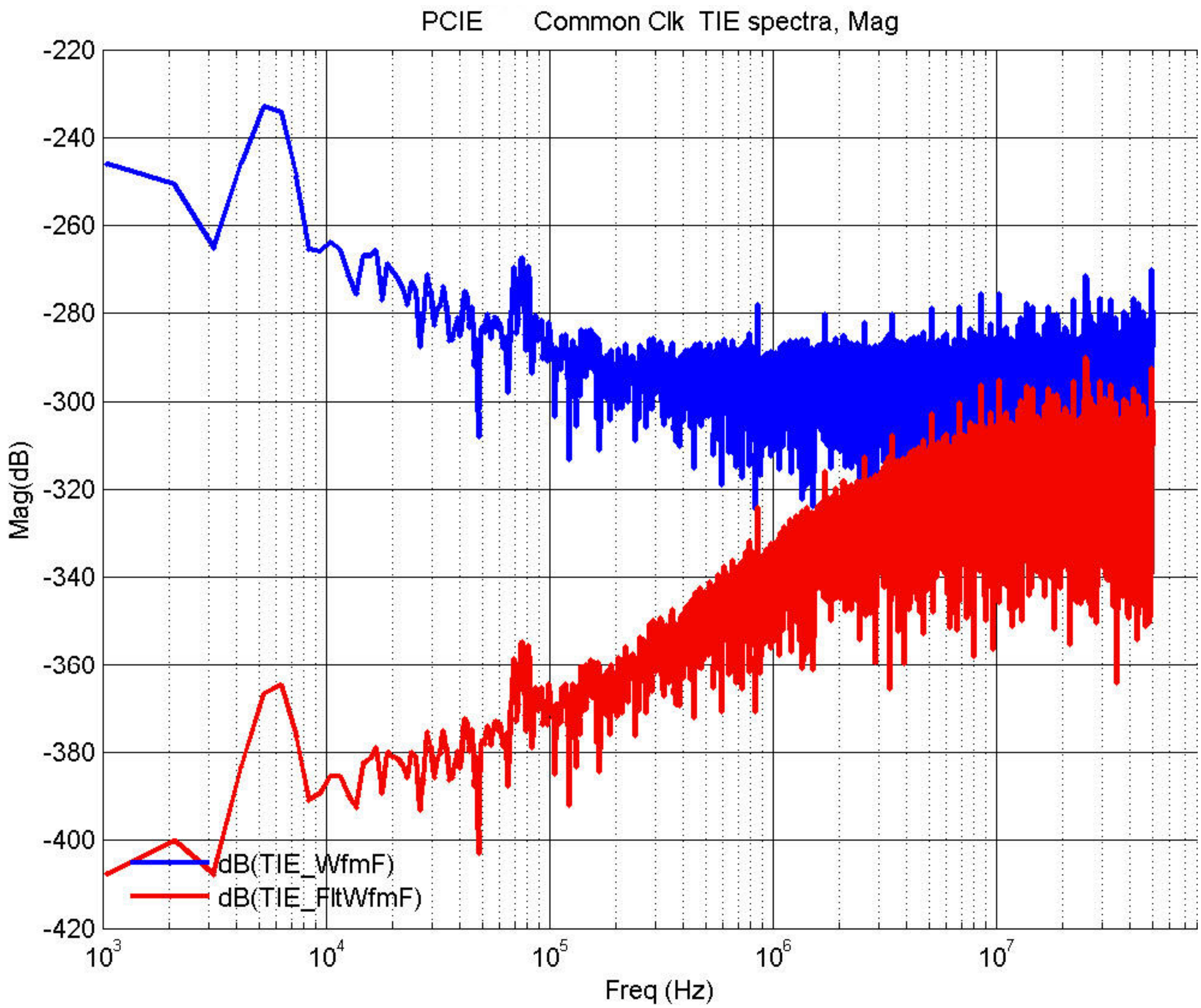


Figure 52 Reference Image for Common Clock TIE Spectra RMS Jitter Test

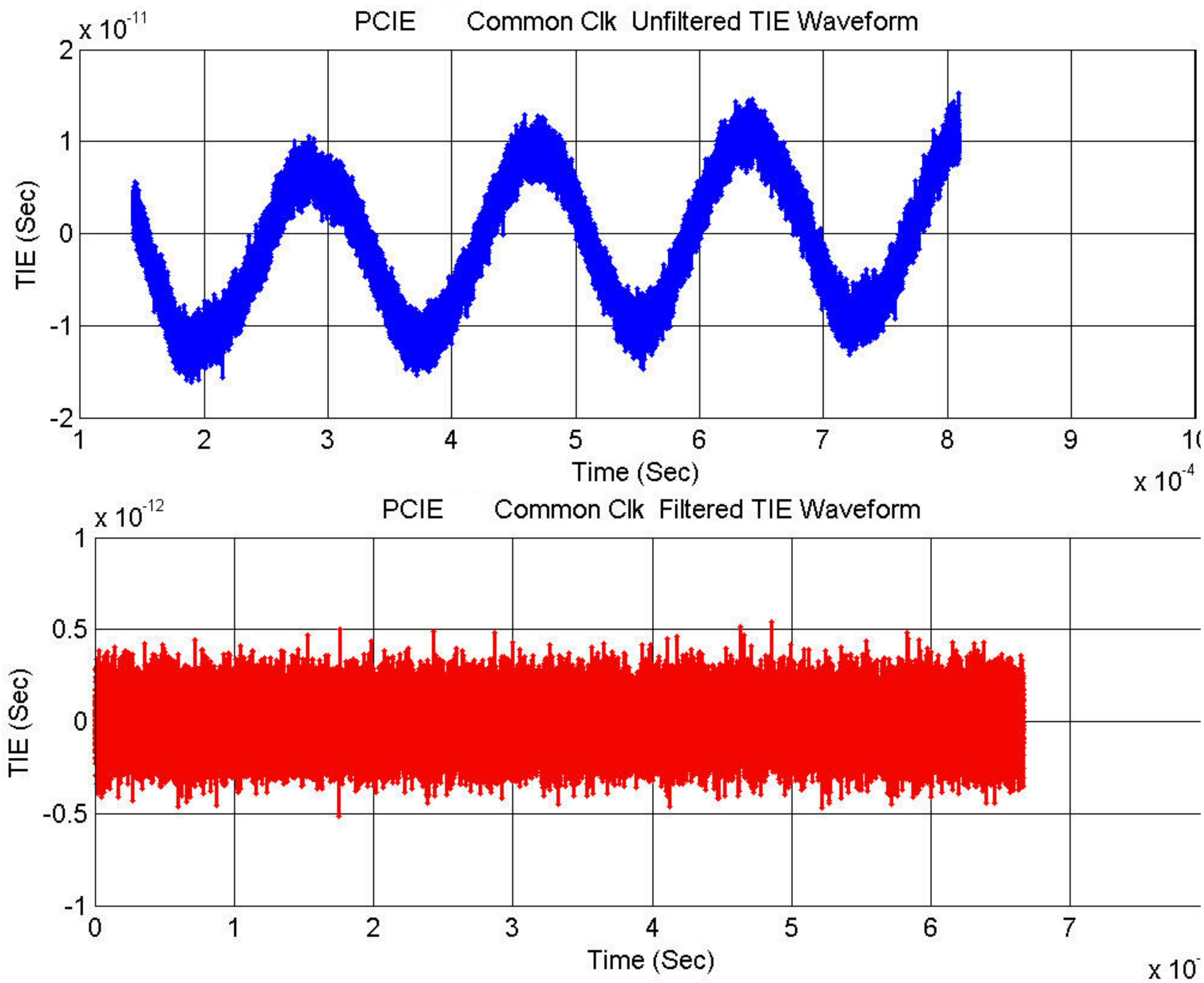


Figure 53 Reference Image for TIE Waveform RMS Jitter Test

PCI-SIG Reference Clock Jitter

This test measures PCI-SIG Reference Clock Jitter for PCIe 5.0 using Intel Clock Jitter Tool.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the PCI-SIG reference clock jitter.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Low Pass Filter**, **SSC Removal**, and **Noise Floor Deembed** option in the Clock Jitter Tool.
3. Performs compliance testing using the Clock Jitter Tool.
4. Captures the Noise Floor Signal if **Noise Floor Deembed** option is enabled.
5. Identifies overall test status.
6. Reports the overall test status, maximum phase jitter value, limits, and settings.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part IV
PCI-Express Gen5 5.0 GT/s Tests

8 Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 5.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

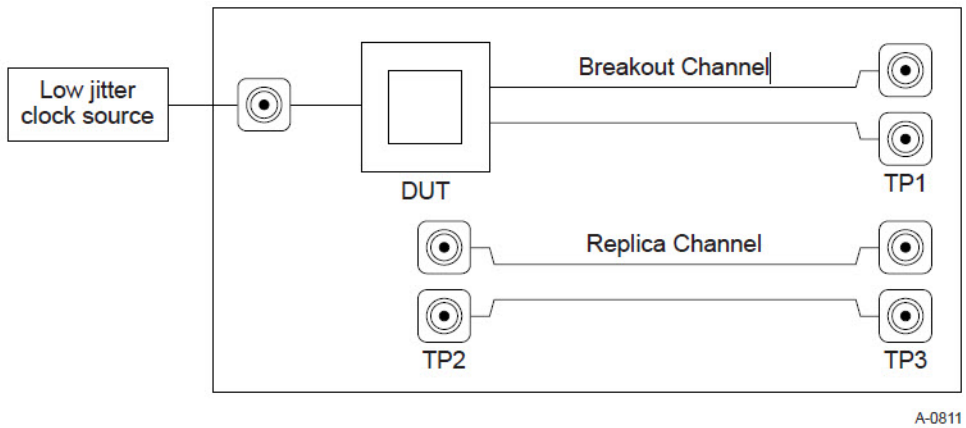


Figure 54 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 5.0 GT/s Tests > Transmitter (Tx) Tests**.

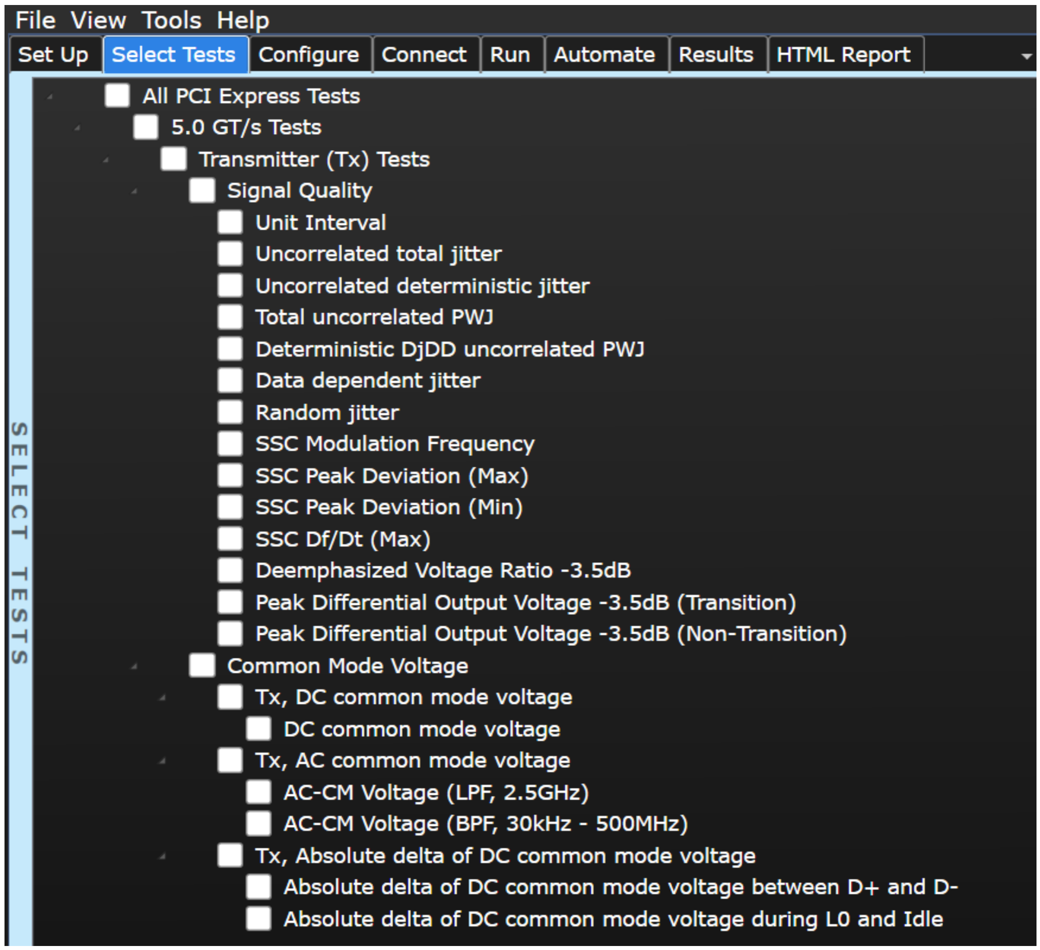


Figure 55 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 33 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

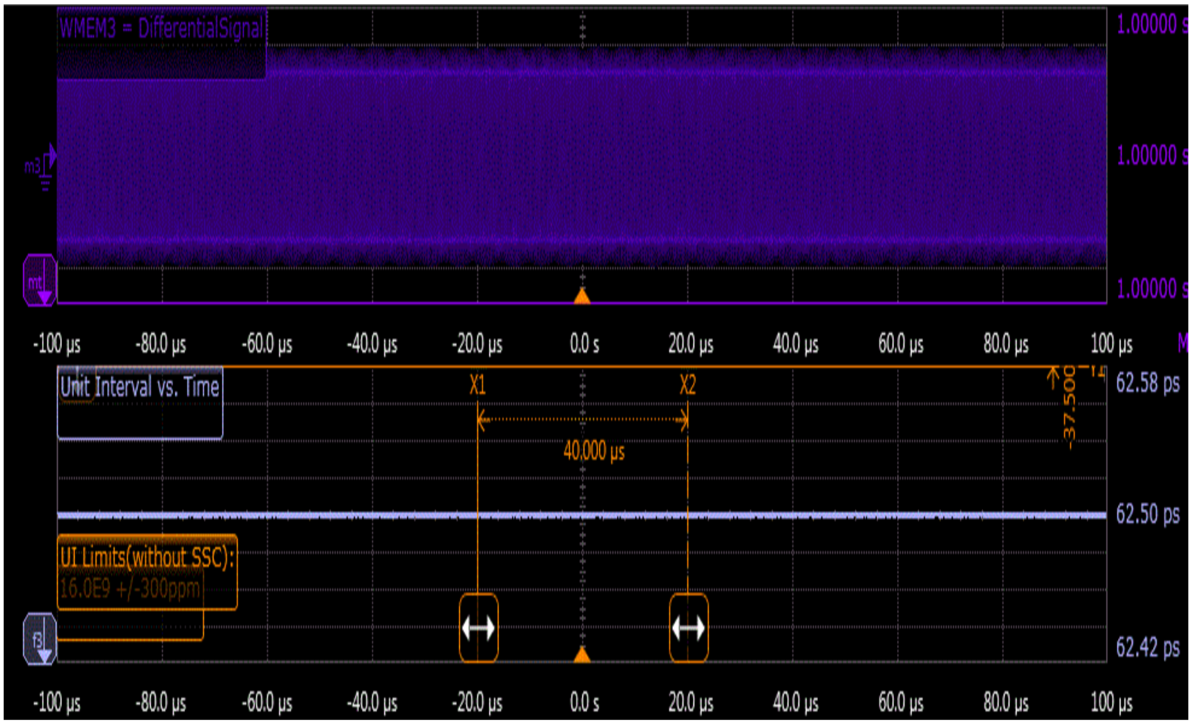


Figure 56 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 34 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	50 ps PP at 10^{-12}

Test Definition Notes from the Specification

- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.
- See PCI Express Base Specification, Revision 5.0, Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$))

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 35 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	30 ps PP

Test Definition Notes from the Specification

- See PCI Express Base Specification, Revision 5.0, Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$))

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak uncorrelated deterministic jitter value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX\text{-}UPW\text{-}TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 36 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UPW\text{-}TJ}$	Total uncorrelated PWJ	40 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See PCI Express Base Specification, Rev 5.0, Section 8.3.5.10 (Uncorrelated Total and Deterministic PWJ ($T_{TX\text{-}UPW\text{-}TJ}$ and $T_{TX\text{-}UPW\text{-}DJDD}$)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 37 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	40 ps PP

Test Definition Notes from the Specification

- See PCI Express Base Specification, Rev 5.0, Section 8.3.5.10 (Uncorrelated Total and Deterministic PWJ ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, T_{TX-DDJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 (Data Dependent Jitter) is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test (Information Only Test)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT. .

Table 38 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.4 - 3.6 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 39 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

a Enables and displays common mode measurements.

b Loads common mode signal to waveform memory.

c Loads and enhance dynamic range D+ signal and D- signal.

d Enables the average common mode measurement.

e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0 as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 2.5 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 40 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50 mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 2.5 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 41 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	Tx AC peak-peak common mode voltage	100 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50 mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 2.5 GHz) test.

1. Gets PCIE5 compliance signal.
2. Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25$ mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 42 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
- DC Common Mode Line Delta
- Average DC value of D+
- Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 43 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

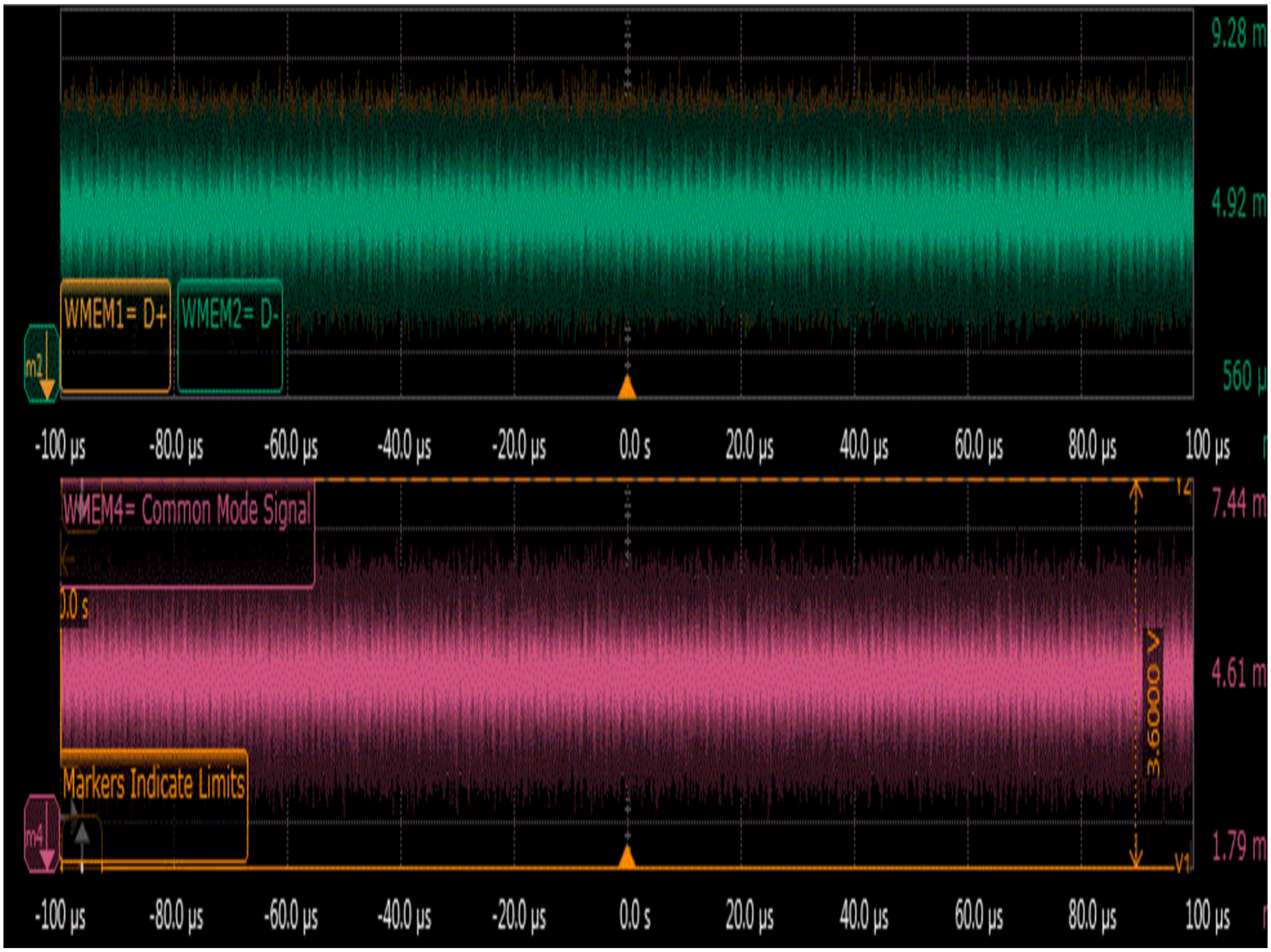


Figure 57 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 44 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 45 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 5.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 46 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 5.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 47 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   - *a* Generates a differential plot (x_n - x_{n-1}).
   - *b* The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

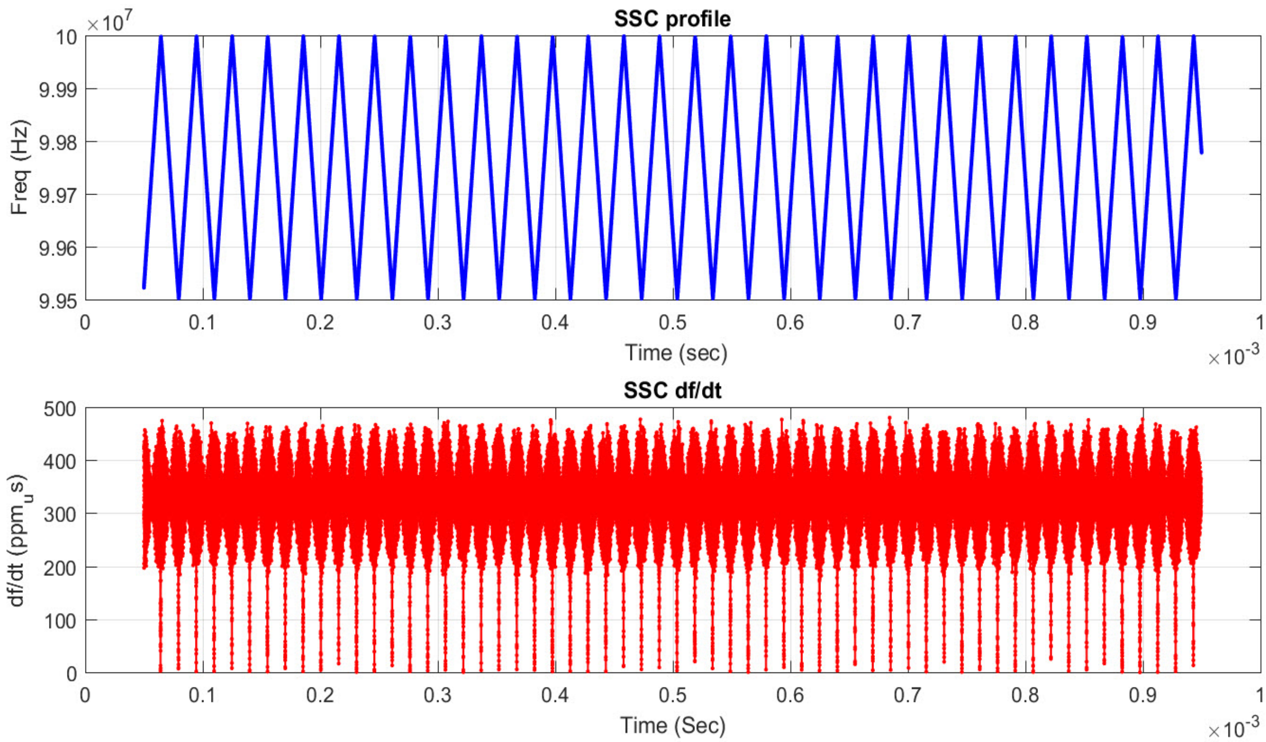


Figure 58 Maximum SSC Slew Rate

Deemphasized Voltage Ratio Test

The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, $V_{TX-DE-RATIO} = -20\log10 (V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 48 Deemphasized Voltage Ratio -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DE-RATIO}$	Deemphasized Voltage Ratio	-4.500 dB	-2.500 dB

Table 49 Deemphasized Voltage Ratio -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DE-RATIO}$	Deemphasized Voltage Ratio	-7.500 dB	-4.500 dB

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

  a Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with Damping Factor of 0.707.

  b Sets the value of **Nominal Data Rate** as **5.0 GT/s** depending on the data rate.

  c Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and bases.

7 Finds the differential value between the transition bits eye top and base as $V_{TX-DIFF-PP}$ using **Histogram**.

8 Finds the differential value between the non-transition bits eye top and base as $V_{TX-DE-EMPH-PP}$ using **Histogram**.

9 Calculates de-emphasis ratio using the following formula:

  De-emphasis ratio = $-20*\log10(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$

10 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the transition eye diagram data from the SigTest tools as $V_{TX\text{-}DIFF\text{-}PP}$.

2 Extracts the non-transition eye diagram data from the SigTest tools as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$.

3 Calculates de-emphasis ratio using the following formula:

De-emphasis ratio: $-20*\log_{10}(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$

4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$

Where,

‘i’ is the index of all waveform values.

‘V_{DIFF}’ is the differential voltage signal.

The **Peak Differential Input Voltage** test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the standard specifications.

$V_{RX\text{-}DIFFp\text{-}p} = 2*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 50 Peak Differential Output Voltage (Transition) -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.800 V	1.20 V

Table 51 Peak Differential Output Voltage (Transition) -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.800 V	1.20 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
   b. Sets the value of **Nominal Data Rate** as **5.0 GT/s**.
   c. Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the transition bits eye top and bases.
5. Finds the differential value between the transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the transition eye diagram data from the SigTest tools.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTest tools.
3. Compares the measured peak differential output/input voltage (transition) value to the compliance test limits.
4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}, Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.6, Table 8-6.

Table 52 Peak Differential Output Voltage (Non-Transition) -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.4765 V	1.20 V

Table 53 Peak Differential Output Voltage (Non-Transition) -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.3374 V	1.20 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   - *a* Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
   - *b* Sets the value of **Nominal Data Rate** as **5.0 GT/s**.
   - *c* Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and bases.
5. Finds the differential value between the non-transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the non-transition eye diagram data from the SigTest tools.
2 Gets largest non-transition amplitude (outer eye), smallest non-transition amplitude (inner eye) test results from SigTest tools.
3 Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

9 CEM-EndPoint Tests, 5.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-EndPoint tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.
Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB, and 5.0 GHz at 6.0 dB.

2 Connect cables up as follows:
   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test).
   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test).

NOTE

When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running CEM-EndPoint Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 5.0 GT/s Tests > CEM EndPoint Tests**.

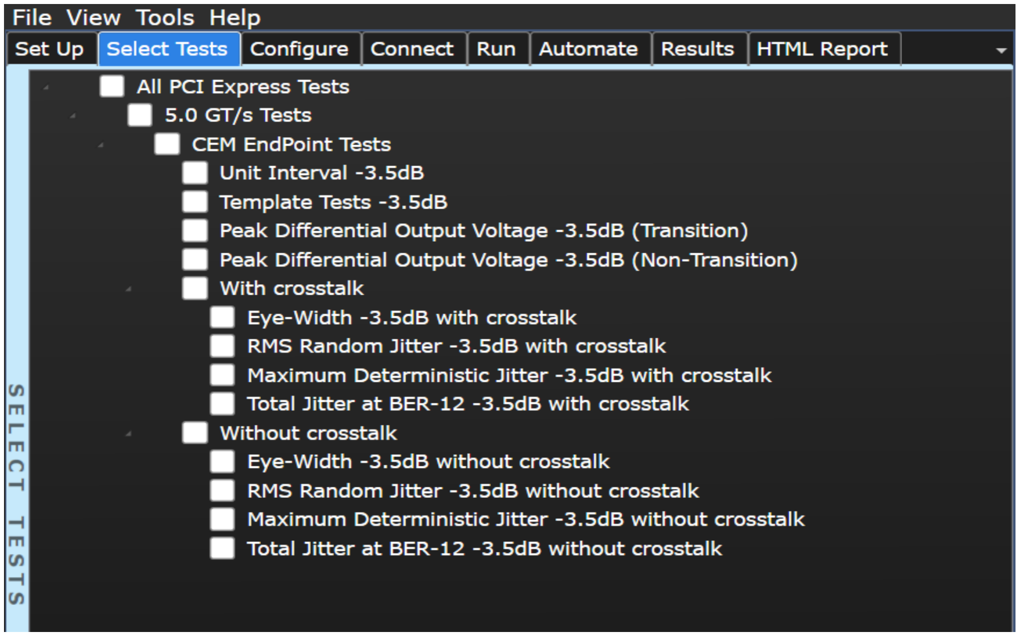


Figure 59 Selecting CEM EndPoint Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 54 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 4.0. To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Unit Interval.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

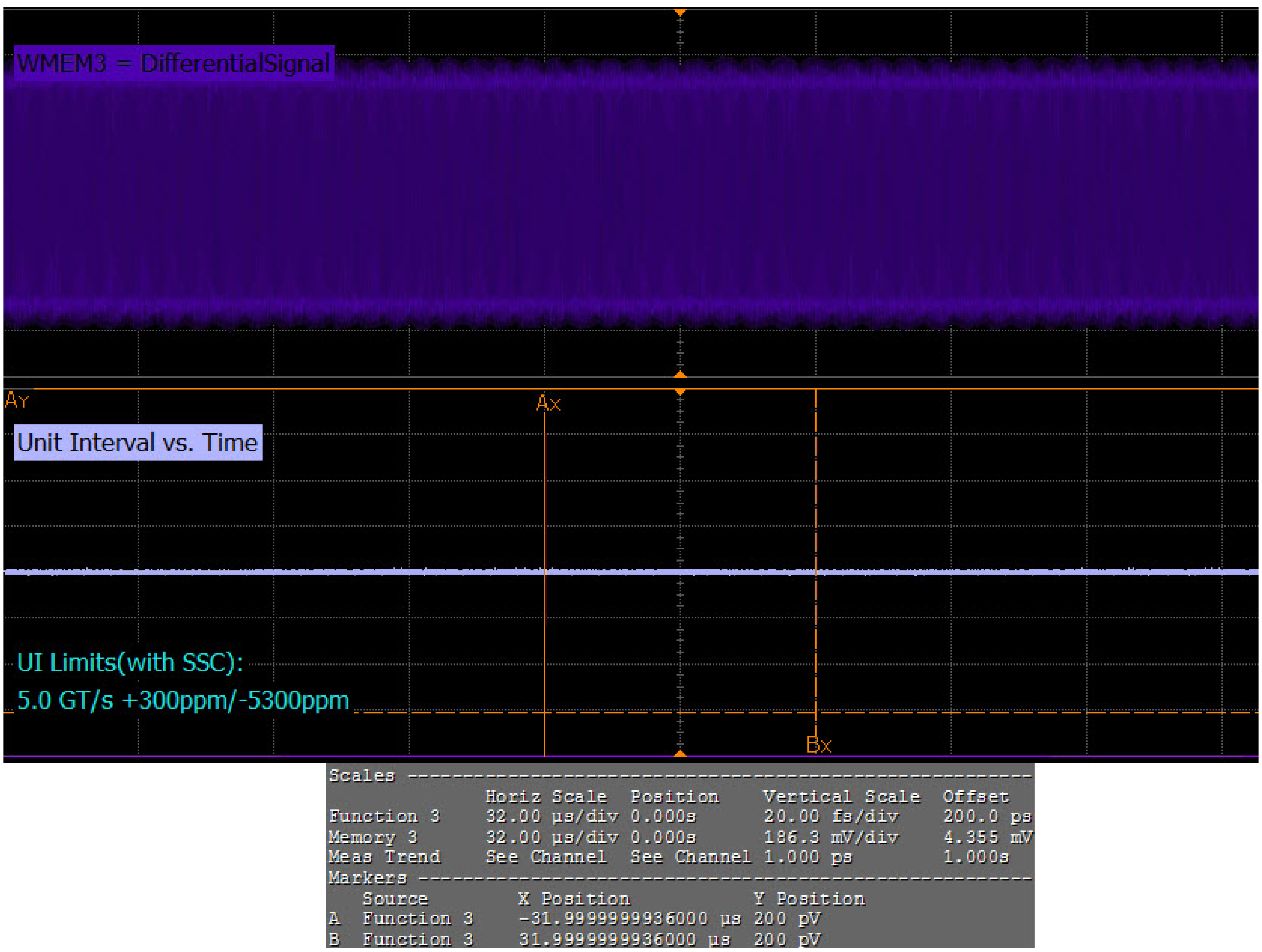


Figure 60 Reference Image for Unit Interval Test

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 2.0, Section 4.7.2, Table 4-8 and Table 4-10 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-7.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_{A_d}).

There exists two different tests for template test with the same test procedure and exception of the template files used for the -3.5dB and 6.0 dB as follows:

- Template test -3.5dB
- Template test -6.0dB

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.1, Figure 4-7 are used as reference to check the compliance of the DUT.

Table 55 Template Test Details -3.5dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	380 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	380 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

Table 56 Template Test Details -6.0dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	306 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	260 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are measured using the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

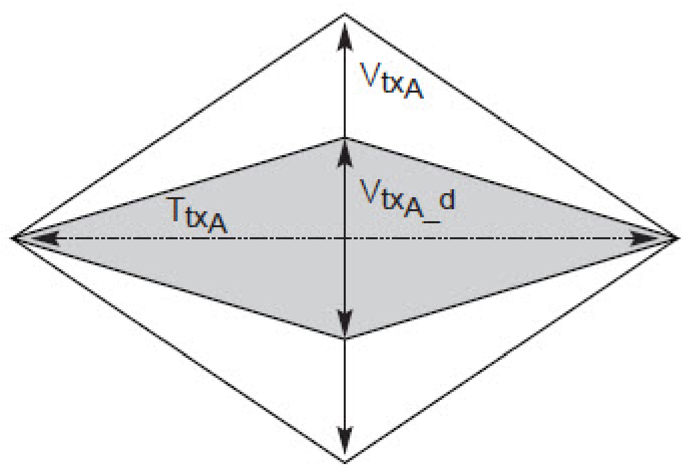


Figure 61 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 4.0. To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Template Tests -3.5dB**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs compliance testing using the SigTestWrapper.dll file.
   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

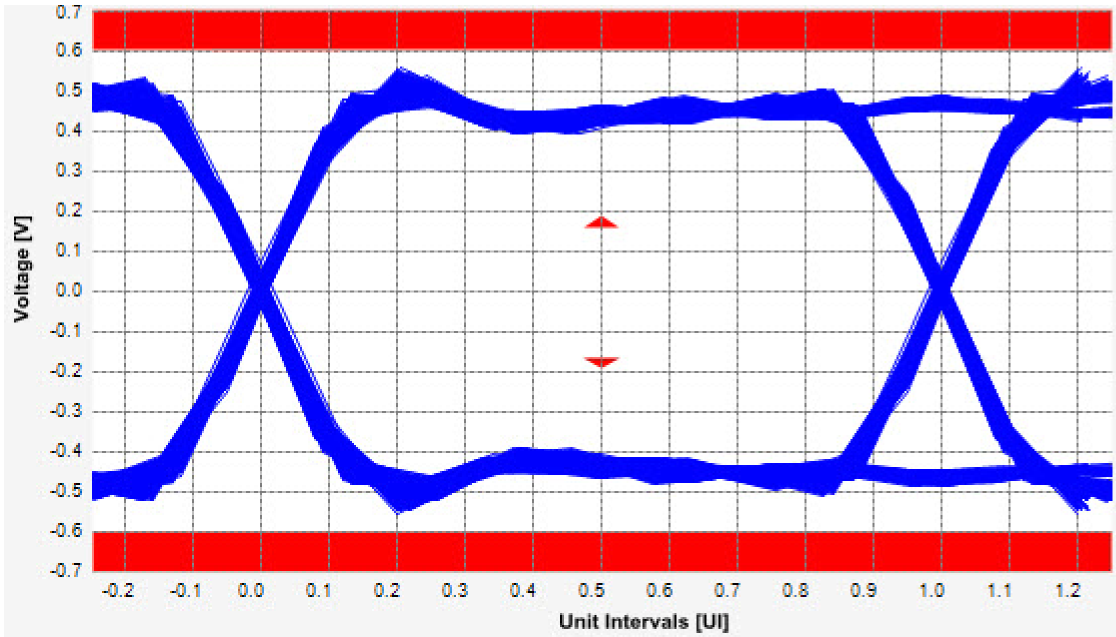


Figure 62 Reference Image for Template (Transition) Test

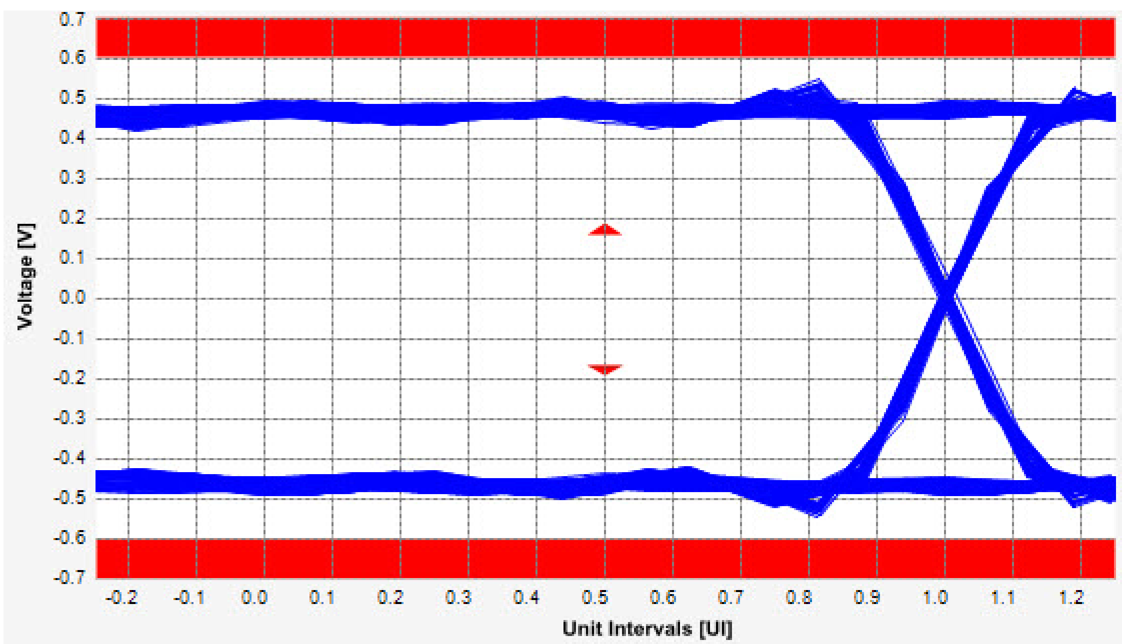


Figure 63 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

There exists two different tests for peak differential output voltage test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB as follows:

- Peak differential output voltage test -3.5dB (Non-transition)
- Peak differential output voltage test -6.0dB (Non-transition)

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.2, Table 4-10 and Table 4-12 are used as reference to check the compliance of the DUT.

Table 57 Template Test Details -3.5dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	380 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	380 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

Table 58 Template Test Details -6.0dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	306 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	260 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are measured using the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

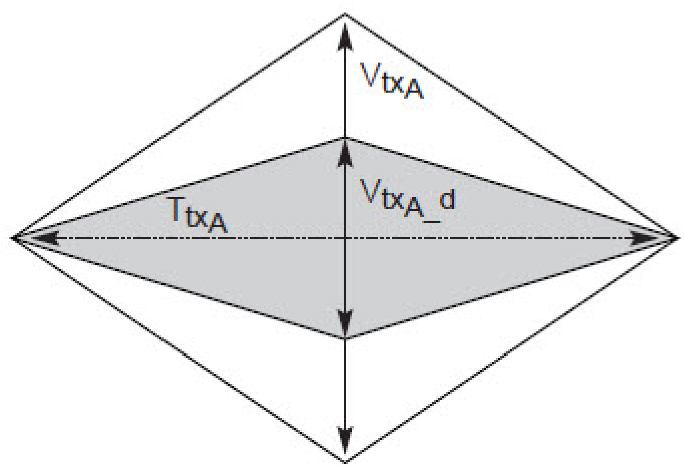


Figure 64 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Peak Differential Output Voltage -3.5dB (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test (-3.5dB, -6.0dB) with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.fies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

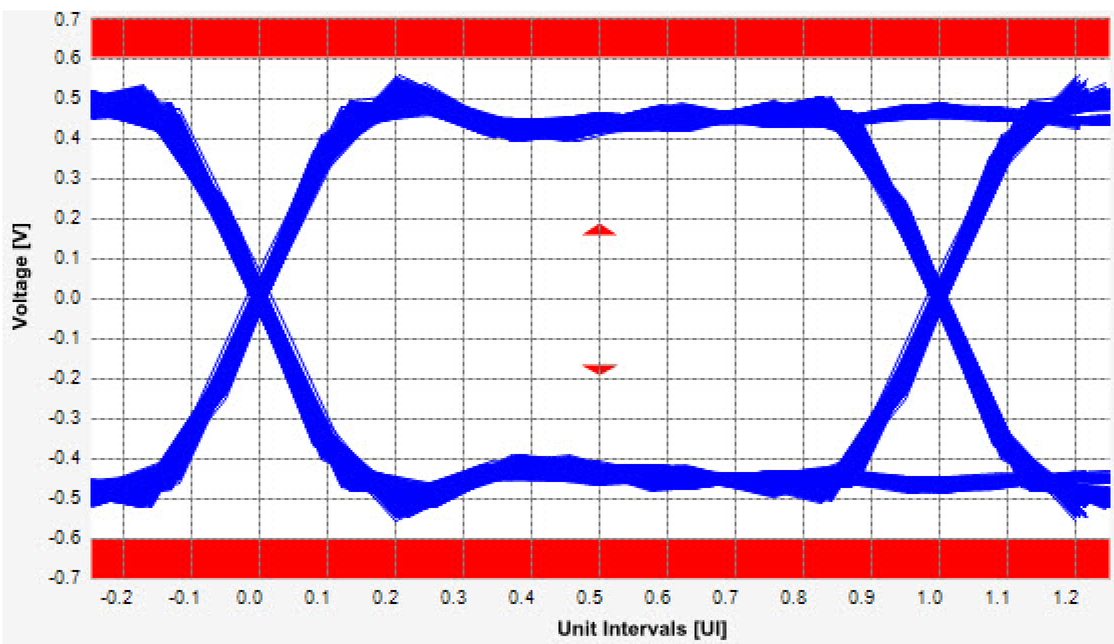


Figure 65 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

‘i’ is the index of all waveform values.

‘V_{DIFF}’ is the differential voltage signal.

There exists two different tests for peak differential output voltage test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB as follows:

- Peak differential output voltage test -3.5dB (Non-transition)
- Peak differential output voltage test -6.0dB (Non-transition)

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.2, Table 4-10 and Table 4-12 are used as reference to check the compliance of the DUT.

Table 59 Template Test Details -3.5dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	380 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	380 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

Table 60 Template Test Details -6.0dB De-emphasis

Symbol	Min	Max	Comments
V_{TXA}	306 mV	1200 mV	Notes 1, 2, 4
V_{TXA_d}	260 mV	1200 mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123 ps	N/A	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126 ps	N/A	

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}. If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are measured using the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

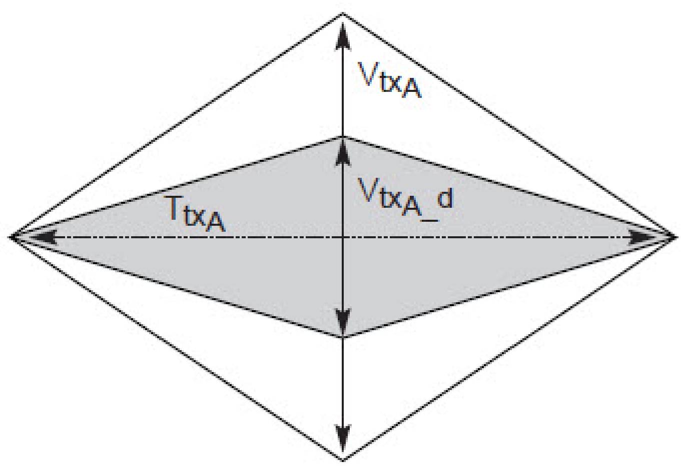


Figure 66 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Peak Differential Output Voltage -3.5dB (Non Transition).**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test (-3.5dB, -6.0dB) with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

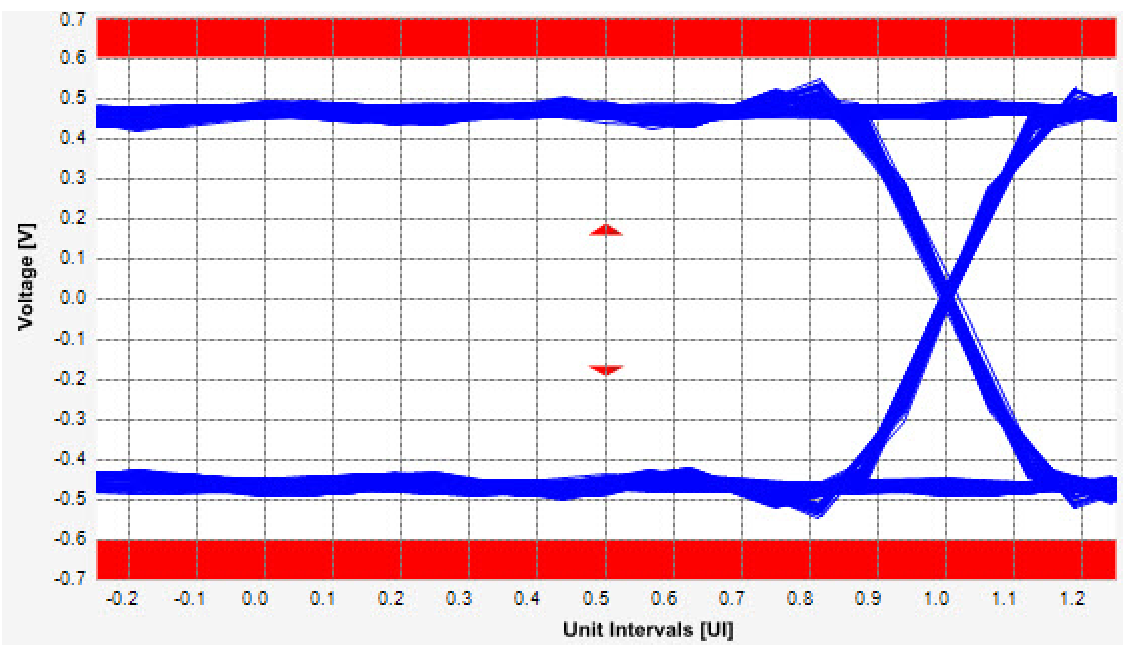


Figure 67 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye - width = [\boldsymbol{M}eanUnitInterval] - [TotalJitteratBER - 12]$$

There exists four different tests for the eye-width test with the same test procedure and exception of the compliance test limits used for the -3.5 dB and 6.0 dB (for with and without crosstalk) as follows:

- Eye-width -3.5 dB with crosstalk
- Eye-width -3.5 dB without crosstalk
- Eye-width -6.0 dB with crosstalk
- Eye-width -6.0 dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.2, Table 4-10 and Table 4-12 is used as reference to check the compliance of the DUT.

Table 61 Eye Width -3.5dB (with or without crosstalk) Test Details

Symbol	Min	Comments
$T_{TXA\ (with\ crosstalk)}$	123 ps	Notes 1, 3, 4
$T_{TXA\ (without\ crosstalk)}$	126 ps	Notes 1, 3, 4

Table 62 Eye Width -6.0dB (with or without crosstalk) Test Details

Symbol	Min	Comments
$T_{TXA\ (with\ crosstalk)}$	123ps	Notes 1, 3, 4
$T_{TXA\ (without\ crosstalk)}$	126ps	Notes 1, 3, 4

Test Definition Notes from the Specification

1 An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA}, and V_{TXA_d} are minimum differential peak-peak output voltages.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} to meet or exceed T_{TXA} . If the Add-in Card uses non-interleaved routing, then crosstalk will be present in the measured data. If the Add-in Card uses interleaved routing, then crosstalk is not present, and an adjusted minimum eye width is used.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

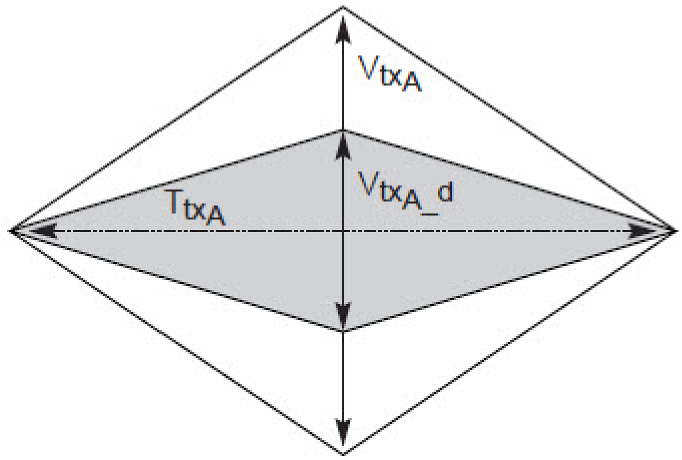


Figure 68 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Eye Width -3.5dB with crosstalk/Eye Width -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter Test (Information Only)

The **Random Jitter < 1.5 MHz** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10 kHz – 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the RMS random jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0dB (for with and without crosstalk) as follows:

- RMS Random Jitter -3.5dB with crosstalk
- RMS Random Jitter -3.5dB without crosstalk
- RMS Random Jitter -6.0dB with crosstalk
- RMS Random Jitter -6.0dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.2, Table 4-11 and Table 4-13 are used as reference to check the compliance of the DUT.

Table 63 RMS Random Jitter-3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Max Rj
With crosstalk	1.4 ps RMS
Without crosstalk	1.4 ps RMS

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **RMS Random Jitter -3.5dB with crosstalk/RMS Random Jitter -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the RMS Random Jitter test results from SigTestWrapper.dll file.
2 Compares the measured RMS Random Jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 5.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10 kHz – 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5 dB and 6.0 dB (for with and without crosstalk) as follows:

- Maximum Deterministic Jitter -3.5 dB with crosstalk
- Maximum Deterministic Jitter -3.5 dB without crosstalk
- Maximum Deterministic Jitter -6.0 dB with crosstalk
- Maximum Deterministic Jitter -6.0 dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.2, Table 4-11 and Table 4-13 is used as reference to check the compliance of the DUT.

Table 64 Maximum Deterministic Jitter-3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	54

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Maximum Deterministic Jitter -3.5dB with crosstalk/Maximum Deterministic Jitter -3.5dB without crosstalk.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the maximum deterministic jitter test results from the SigTestWrapper.dll file.
2 Compares the measured maximum deterministic jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 5.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10 kHz – 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5 dB and 6.0 dB (for with and without crosstalk) as follows:

- Total Jitter at BER-12 -3.5 dB with crosstalk
- Total Jitter at BER-12 -3.5 dB without crosstalk
- Total Jitter at BER-12 -6.0 dB with crosstalk
- Total Jitter at BER-12 -6.0 dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.2, Table 4-11 and Table 4-13 is used as reference to check the compliance of the DUT.

Table 65 Total Jitter at BER-12 -3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Tj at BER 10^{-12}(ps)
With crosstalk	77
Without crosstalk	74

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-EndPoint Tests" on page 203 and select **Total Jitter at BER-12 -3.5dB with crosstalk/Total Jitter at BER-12 -3.5dB without crosstalk.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the total jitter at BER-12 test results from the SigTestWrapper.dll file.
2 Compares the measured total jitter at BER-12 values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

10 CEM-RootComplex Tests, 5.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-RootComplex tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.
   The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.
2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.
3 Connect cables up as follows:
   a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR
   b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running CEM-RootComplex Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 5.0 GT/s Tests > CEM RootComplex Tests**.

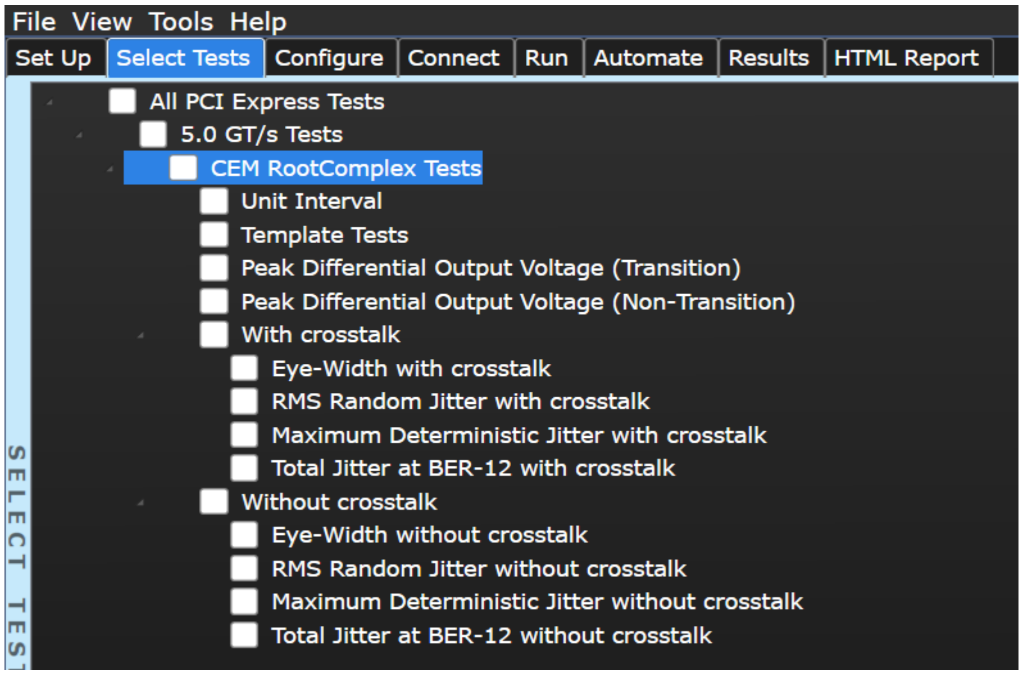


Figure 69 Selecting System Board (Tx) Tests

Unit Interval Test (Information only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 66 Unit Interval Test Details

Symbol	Parameter	Min	Max	Comments
UI	Unit Interval	199.94 ps	200.06 ps	For each reference clock source, the UI has tolerance of +/-300 ppm. Period does not account for SSC dictated variations.

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0. To execute the test, follow the procedure in** "Running CEM-RootComplex Tests" **on page 227** **and select Unit Interval.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

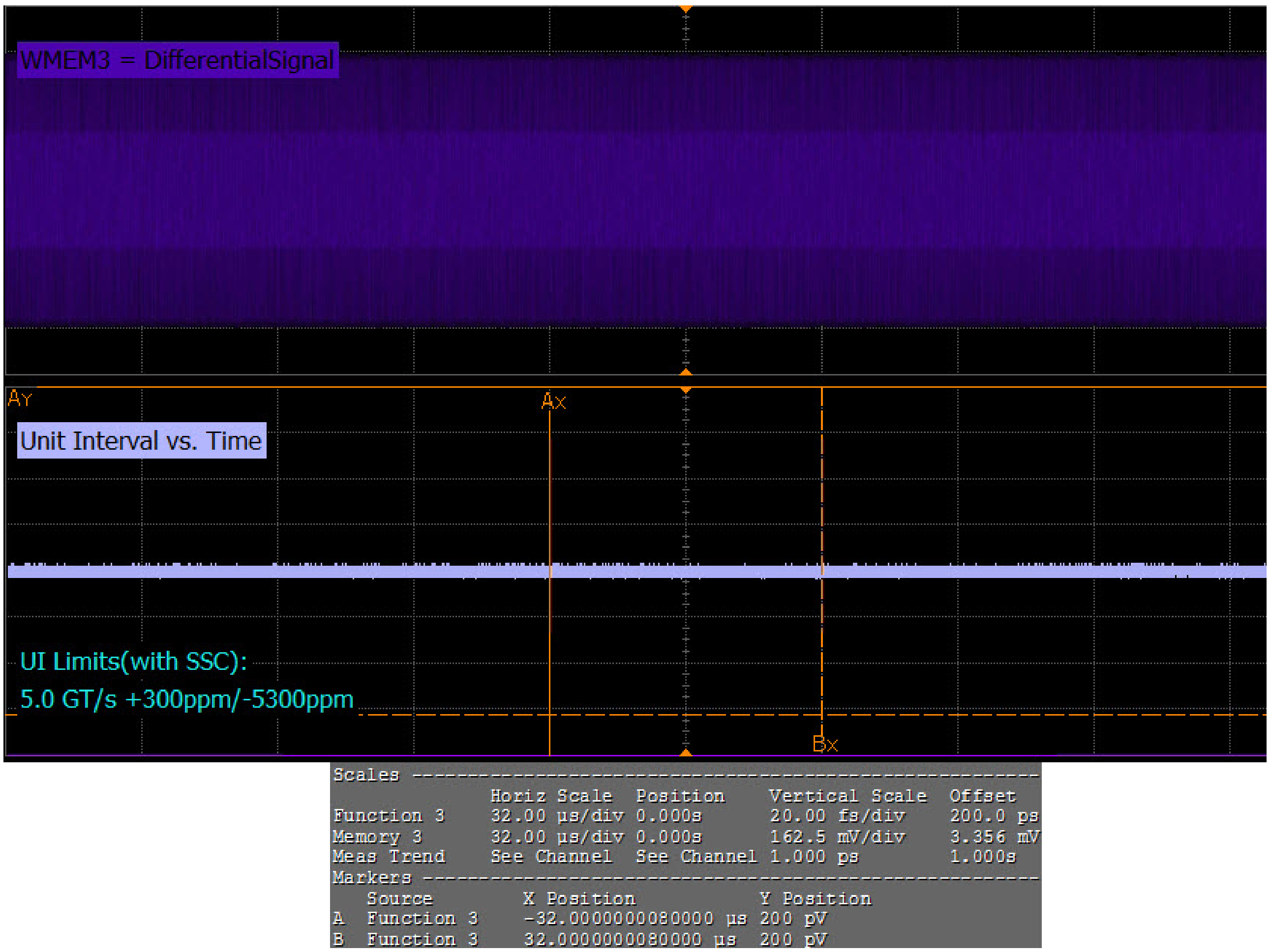


Figure 70 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.7.6, Table 4-15 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Figure 4-9 fis used as reference to check the compliance of the DUT.

Table 67 Template Test Details

Symbol	Min	Max
V_{TXS}	225 mV	1200 mV
V_{TXS_d}	225 mV	1200 mV
T_{TXS} (with crosstalk)	95 ps	
T_{TXS} (without crosstalk)	108 ps	

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages.

3 T_{TXS} is the minimum eye width. The sample size for the dual port measurement is required to be at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must meet or exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge-finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

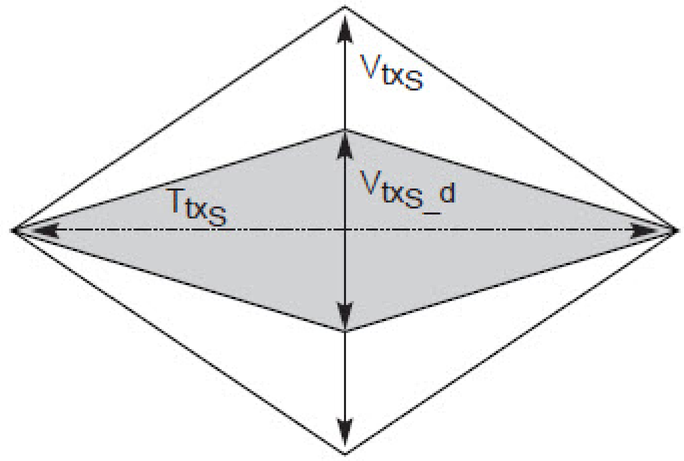


Figure 71 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0. To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 227 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

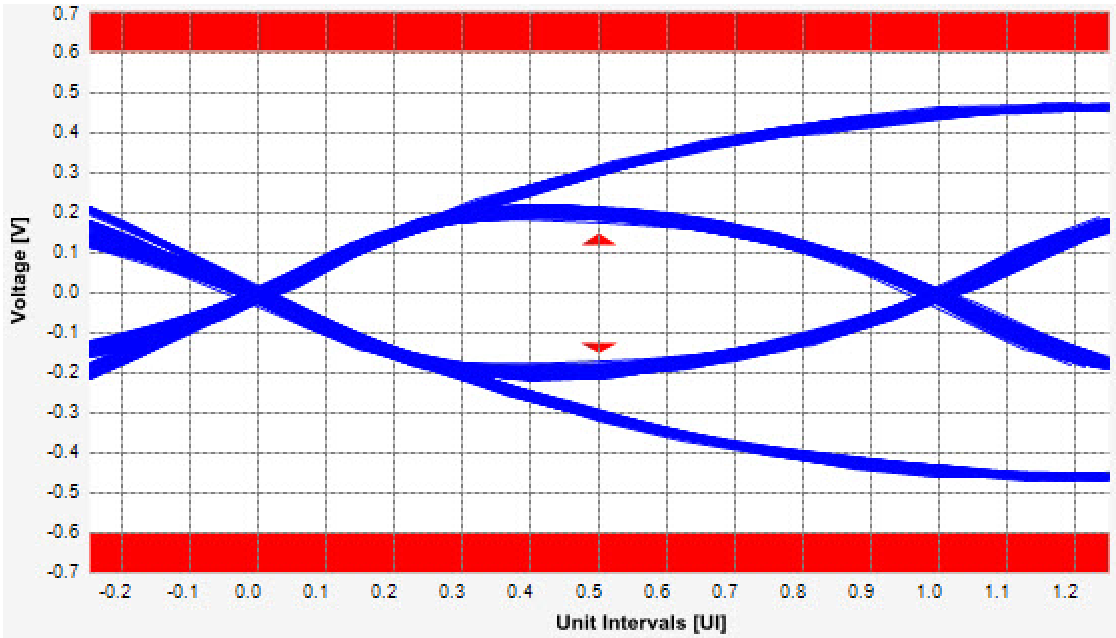


Figure 72 Reference Image for Template (Transition) Test

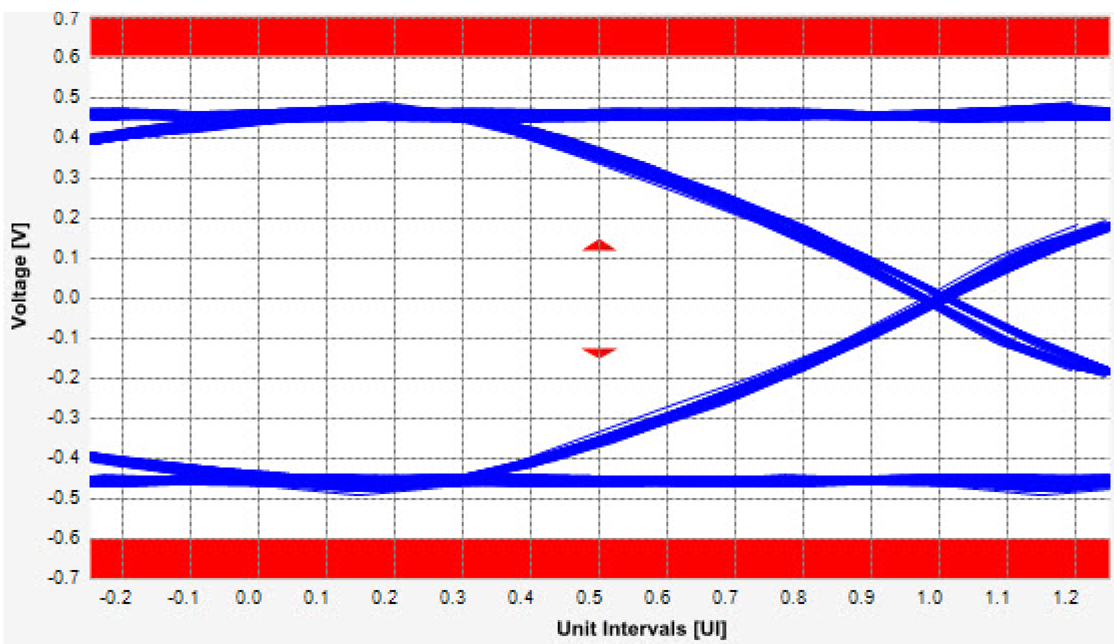


Figure 73 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2 * Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-26 is used as reference to check the compliance of the DUT.

Table 68 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max
V_{TXS}	225 mV	1200 mV
V_{TXS_d}	225 mV	1200 mV

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages.

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge-finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

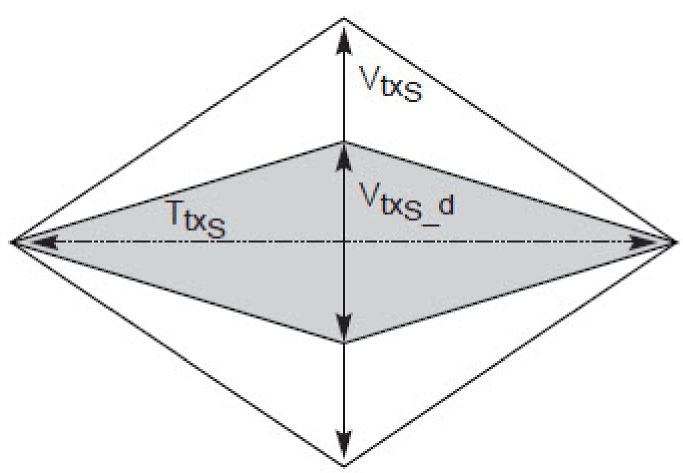


Figure 74 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 227 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

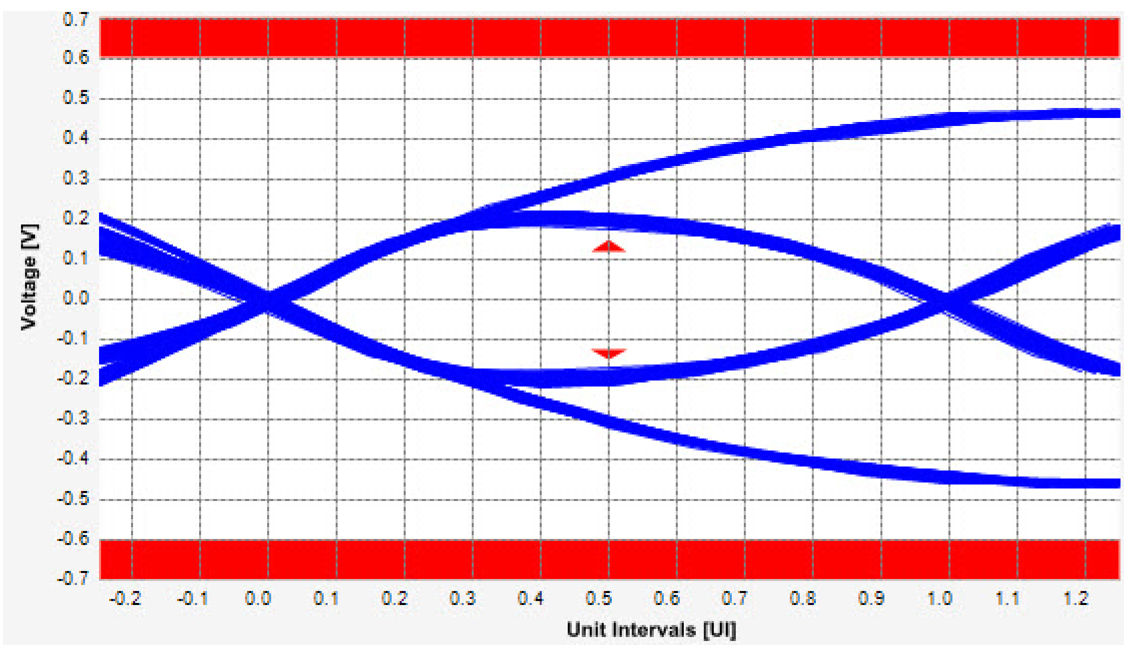


Figure 75 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-26 is used as reference to check the compliance of the DUT.

Table 69 Peak Differential Output Voltage (Non-transition) Test Details

Symbol	Min	Max
V_{TXA}	225 mV	1200 mV
V_{TXA_d}	225 mV	1200 mV

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages.

3 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge-finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification.

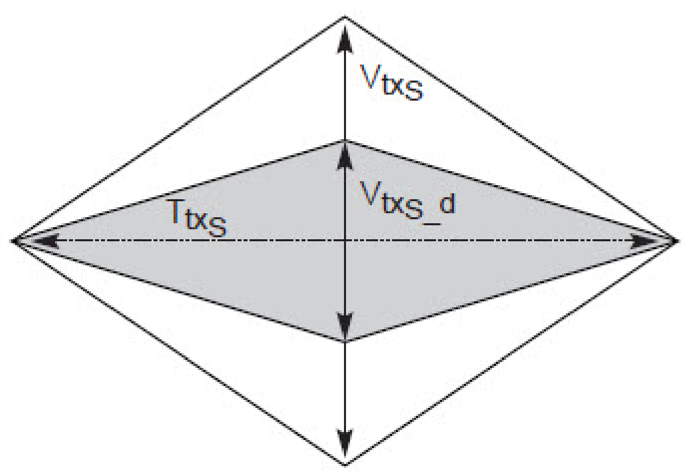


Figure 76 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in “Running CEM-RootComplex Tests" on page 227 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.
5 Reports the measured peak differential output voltage (non-transition) value as the measurement result and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

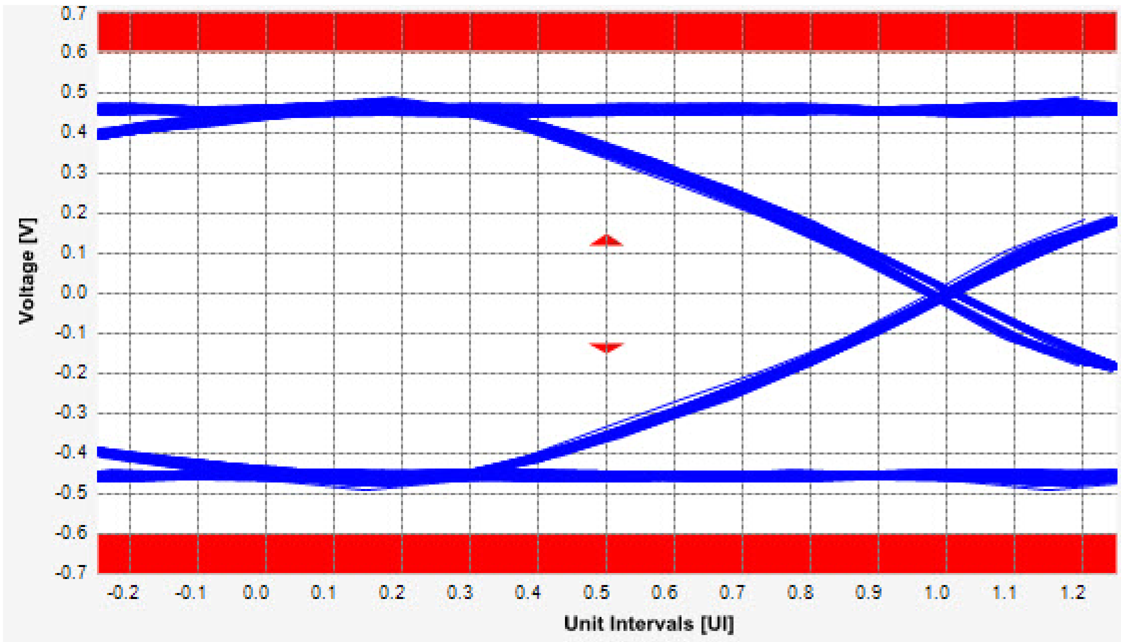


Figure 77 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

There exists two different tests for the eye-width test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Eye-width with crosstalk
- Eye-width without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-26 is used as reference to check the compliance of the DUT.

Table 70 Eye Width (with or without crosstalk) Test Details

Symbol	Min
$T_{TXS\ (with\ crosstalk)}$	95 ps
$T_{TXS\ (without\ crosstalk)}$	108 ps

Test Definition Notes from the Specification

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that compliance pattern with 8b/10b encoding (refer to the PCI Express Base Specification) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.
2. T_{TXS} is the minimum eye width. The sample size for the dual port measurement is required to be at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must meet or exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present, and an adjusted minimum eye width is used.
3. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge-finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the PCI Express Architecture PHY Test Specification

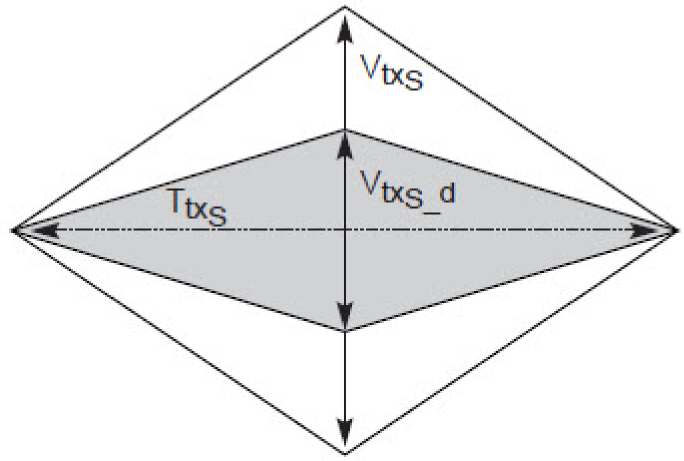


Figure 78 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 227 and select **Eye-Width with crosstalk/Eye-Width without crosstalk.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter Test (Information Only)

The **Random Jitter < 1.5MHz** test is a timing measurement in PCI Express 5.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10 kHz – 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the RMS random jitter test with the same test procedure and exception of the compliance test limits used for the -3.5 dB and 6.0 dB (for with and without crosstalk) as follows:

- RMS Random Jitter with crosstalk
- RMS Random Jitter without crosstalk

NOTE The RMS range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-27 is used as reference to check the compliance of the DUT.

Table 71 RMS Random Jitter (with or without crosstalk) Test Details

Parameter	Max Rj
With crosstalk	3.410 ps RMS
Without crosstalk	3.410 ps RMS

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 227 and select **RMS Random Jitter with crosstalk/RMS Random Jitter without crosstalk.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the RMS Random Jitter test results from SigTestWrapper.dll file.
2 Compares the measured RMS Random Jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 5.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10 kHz – 1.5 MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5 dB and 6.0 dB (for with and without crosstalk) as follows:

- Maximum Deterministic Jitter with crosstalk
- Maximum Deterministic Jitter without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-27 is used as reference to check the compliance of the DUT.

Table 72 Maximum Deterministic Jitter (with or without crosstalk) Test Details

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	44

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running CEM-RootComplex Tests" on page 227 and select **Maximum Deterministic Jitter with crosstalk/Maximum Deterministic Jitter without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the maximum deterministic jitter test results from the SigTestWrapper.dll file.
2 Compares the measured maximum deterministic jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 5.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used with and without crosstalk as follows:

- Total Jitter at BER-12 with crosstalk
- Total Jitter at BER-12 without crosstalk

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.14, Table 4-27 is used as reference to check the compliance of the DUT.

Table 73 Total Jitter at BER-12 (with or without crosstalk) Test Details

Parameter	Tj at BER 10^{-12}(ps)
With crosstalk	105
Without crosstalk	92

Understanding the Test Flow

NOTE To execute the test, follow the procedure in “Running CEM-RootComplex Tests" on page 227 and select **Total Jitter at BER-12 with crosstalk/Total Jitter at BER-12 without crosstalk.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 5.0 GT/s

1 Obtains the total jitter at BER-12 test results from the SigTestWrapper.dll file.
2 Compares the measured total jitter at BER-12 values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

11 Reference Clock Tests, 5.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 5.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE

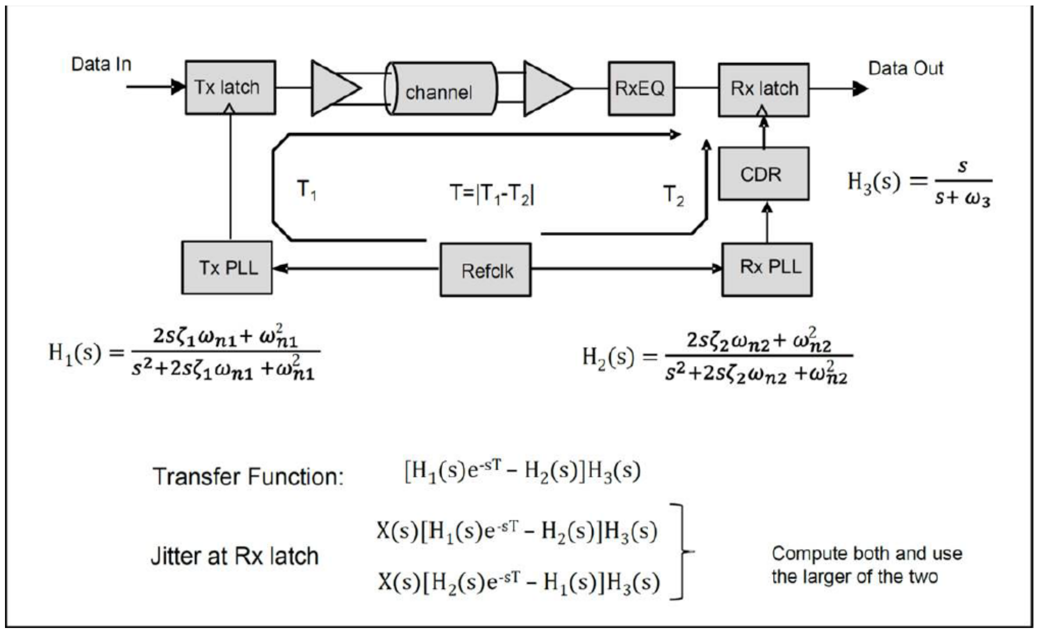
It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 5.0 GT/s, PCI-E 5.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 5 GT/s

PLL #1	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(min)$ = 5.0 MHz	ω_{n1}= 1.12 Mrad/s ζ_1 = 14	ω_{n1}= 11.01 Mrad/s ζ_1 = 1.16
$BW_{PLL}(max)$ = 16 MHz	ω_{n1}= 3.58 Mrad/s ζ_1 = 14	ω_{n1}= 35.26 Mrad/s ζ_1 = 1.16

PLL #2	0.01 dB peaking	3.0 dB peaking
$BW_{PLL}(min)$ = 8.0 MHz	ω_{n2}= 1.79 Mrad/s ζ_2 = 14	ω_{n2}= 26.86 Mrad/s ζ_2 = 0.54
$BW_{PLL}(max)$ = 16 MHz	ω_{n2}= 3.58 Mrad/s ζ_2 = 14	ω_{n2}= 53.73 Mrad/s ζ_2 = 0.54

$BW_{CDR}(min)$ = 5 MHz, 1st order

64 combinations

5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s, ζ_1 = 14	ω_{n1}= 6.02 Mrad/s, ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s, ζ_1 = 14	ω_{n1}= 12.04 Mrad/s, ζ_1 = 0.73

PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s, ζ_2 = 14	ω_{n2}= 4.62 Mrad/s, ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s, ζ_2 = 14	ω_{n2}= 11.53 Mrad/s, ζ_2 = 1.15

BW_{CDR}(min) = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s, ζ_1 = 14	ω_{n1}= 1.51 Mrad/s, ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s, ζ_1 = 14	ω_{n1}= 5.42 Mrad/s, ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

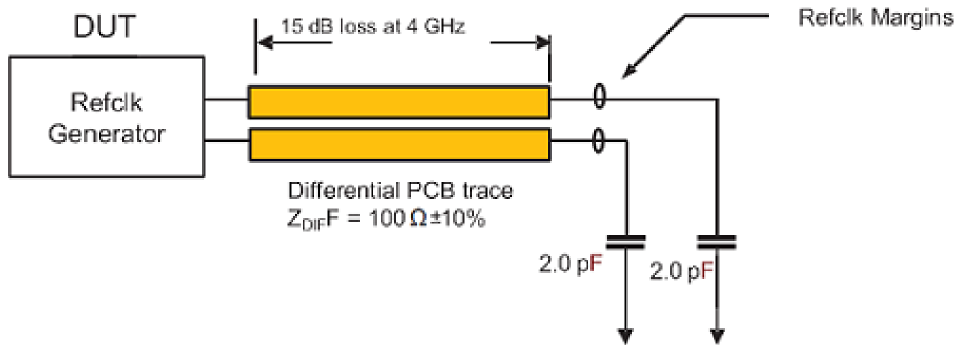


Figure 79 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 5.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

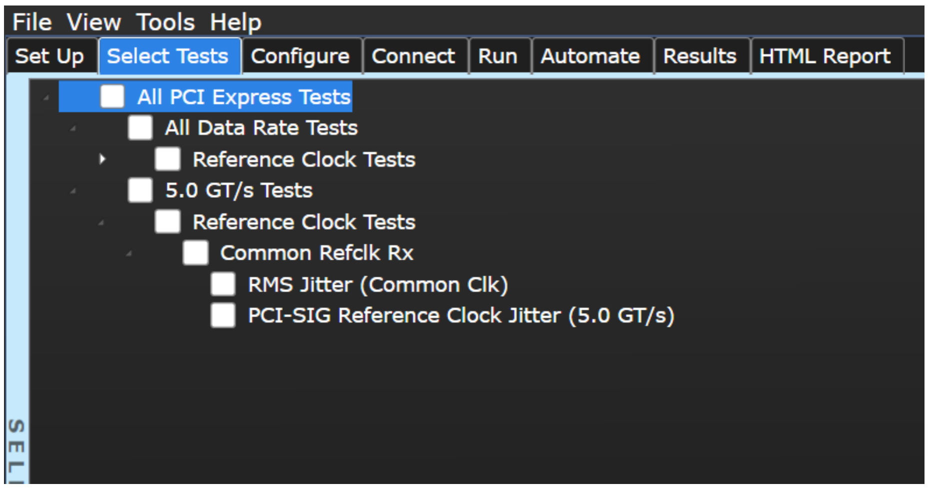


Figure 80 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK\text{-}RMS\text{-}CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 74 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK\text{-}RMS\text{-}CC}$	RMS Refclk jitter for common Refclk architecture	3.1 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-73 (Common Refclk Rx Architecture for all Data Rates Except 32.0 GT/s); section 8.6.6 of PCI Express Base Specification Revision 5.0.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

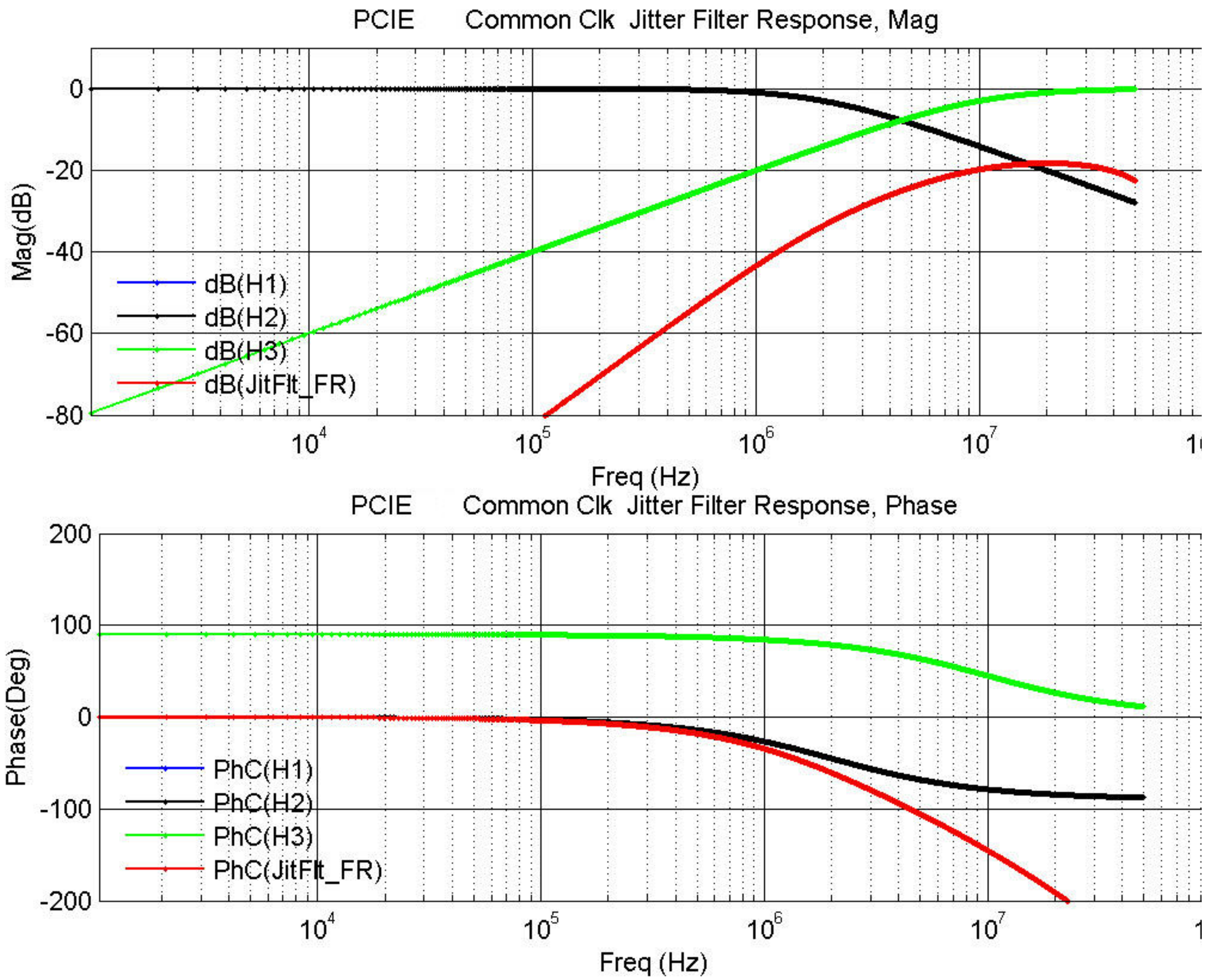


Figure 81 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

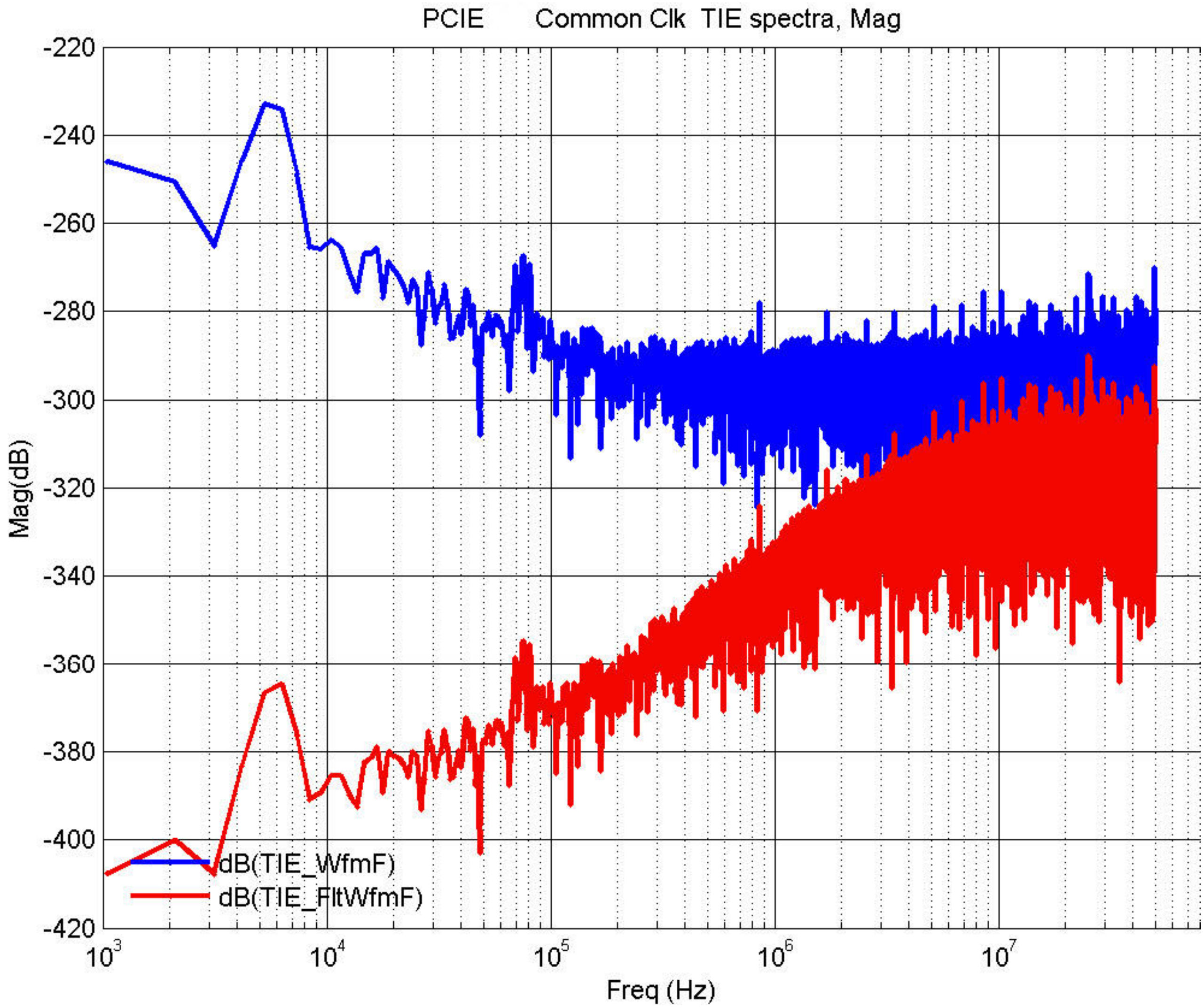


Figure 82 Reference Image for Common Clock TIE Spectra RMS Jitter Test

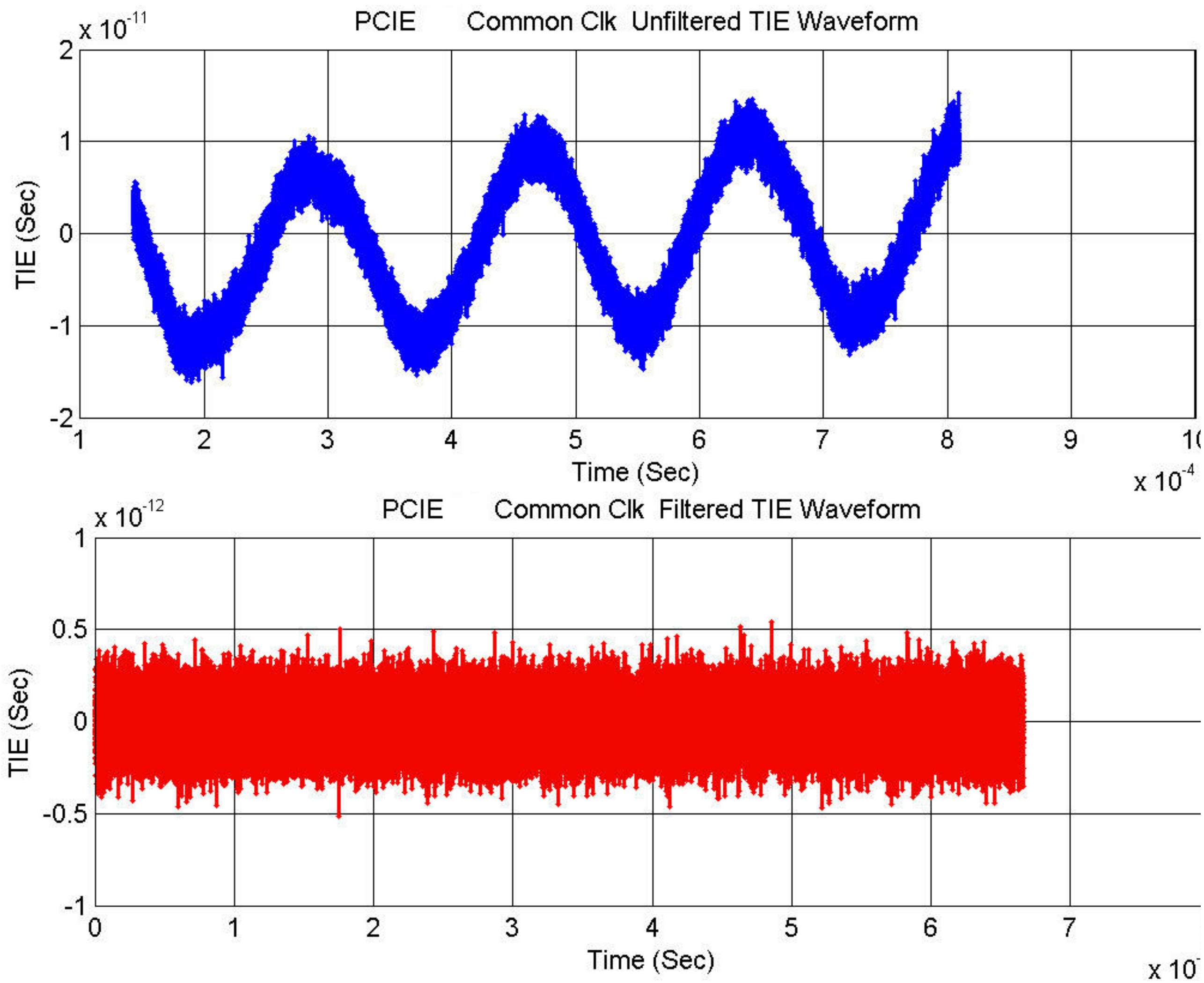


Figure 83 Reference Image for TIE Waveform RMS Jitter Test

PCI-SIG Reference Clock Jitter

This test measures PCI-SIG Reference Clock Jitter for PCIe 5.0 using Intel Clock Jitter Tool.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the PCI-SIG reference clock jitter.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Low Pass Filter**, **SSC Removal**, and **Noise Floor Deembed** option in the Clock Jitter Tool.
3. Performs compliance testing using the Clock Jitter Tool.
4. Captures the Noise Floor Signal if **Noise Floor Deembed** option is enabled.
5. Identifies overall test status.
6. Reports the overall test status, maximum phase jitter value, limits, and settings.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part V
PCI-Express Gen5 8.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

12 Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 8.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE **It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.**

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

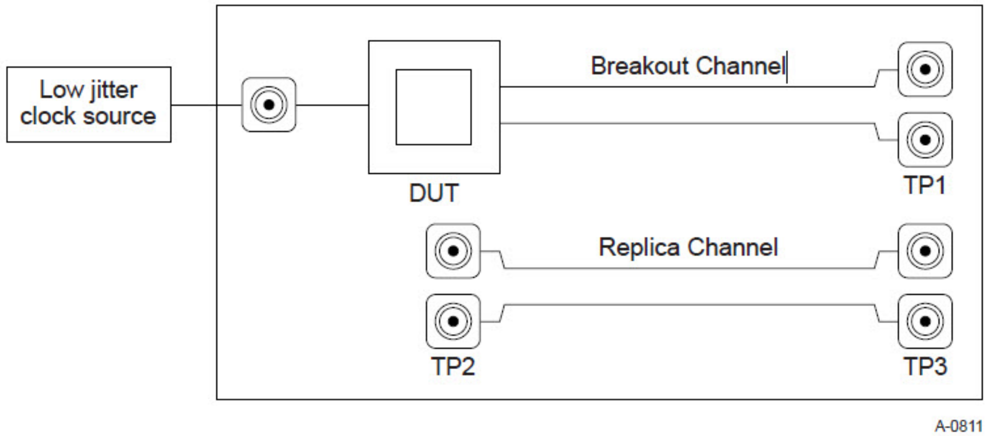


Figure 84 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 8.0 GT/s Tests > Transmitter (Tx) Tests**.

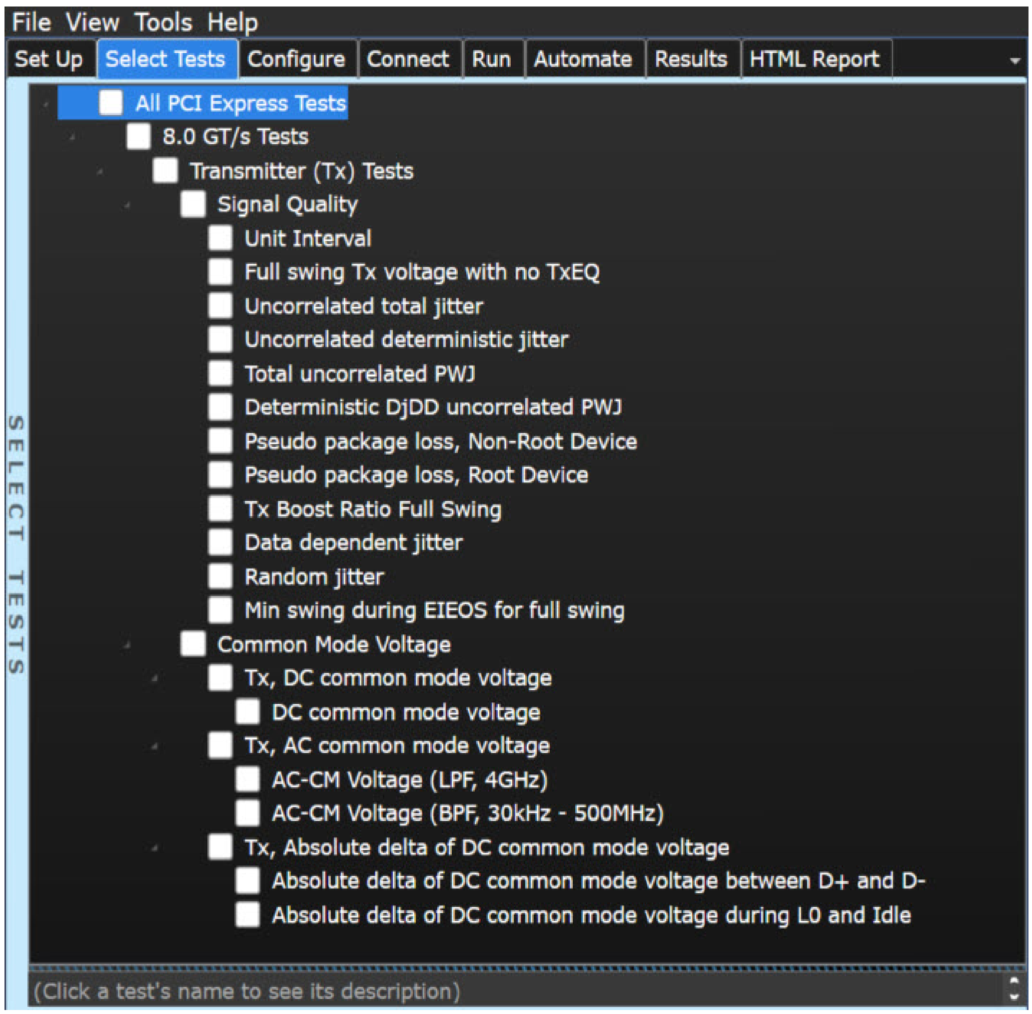


Figure 85 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 75 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	Clean Clock: 124.9625 ps	Clean Clock 125.0375 ps
		SSC: 124.9625 ps	SSC: 125.6603 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
  a Selects **Unit Interval** as data measurement analysis unit.
  b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

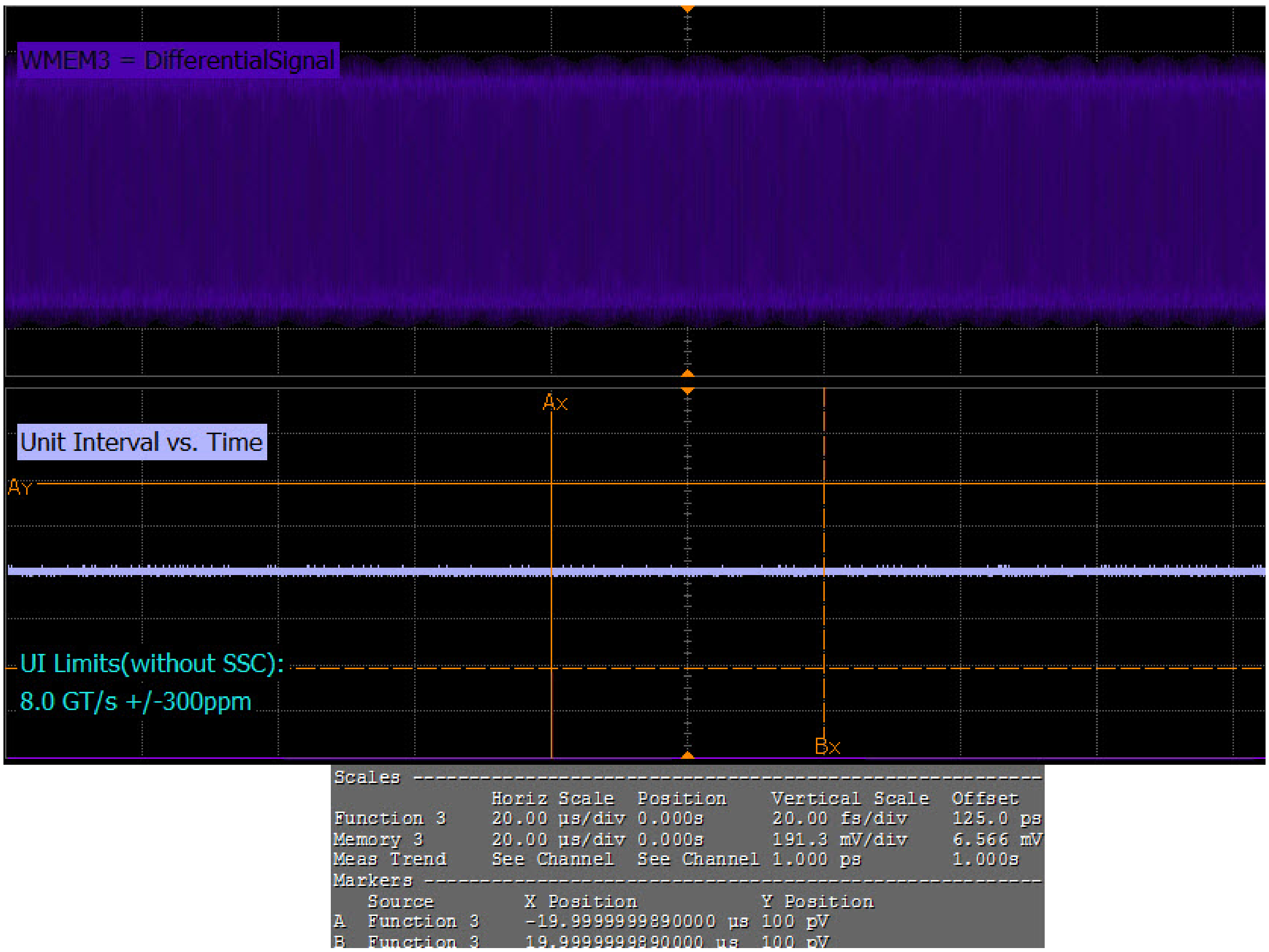


Figure 86 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 87. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP}$ is used as reference to check the compliance of the DUT.

Table 76 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$	Full swing Tx voltage with no TxEQ	800 mV_{PP}	1300 mV_{PP}

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

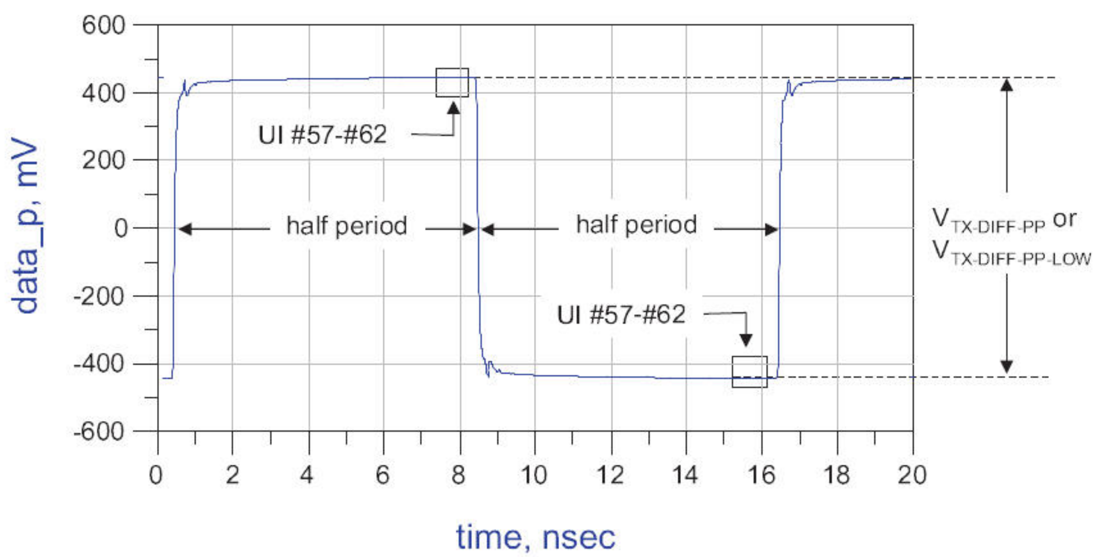


Figure 87 $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 88. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 4.3.3.13.1, Table 4-19, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 77 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as 2 × | V_{TXD+}-V_{TXD-}|
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

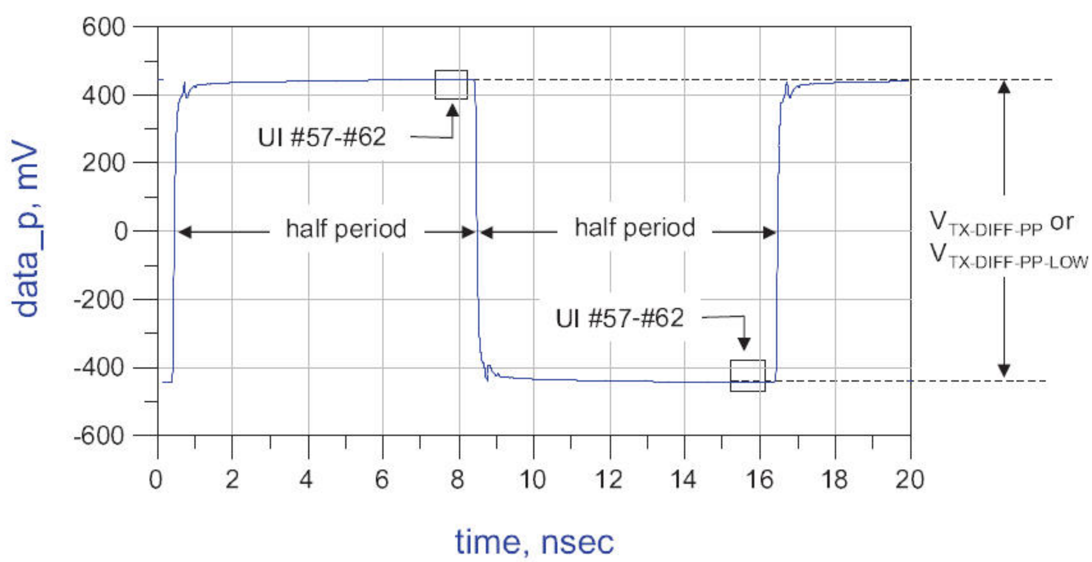


Figure 88 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 78 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0 and 32.0 GT/s that ensures that these parameters are met.

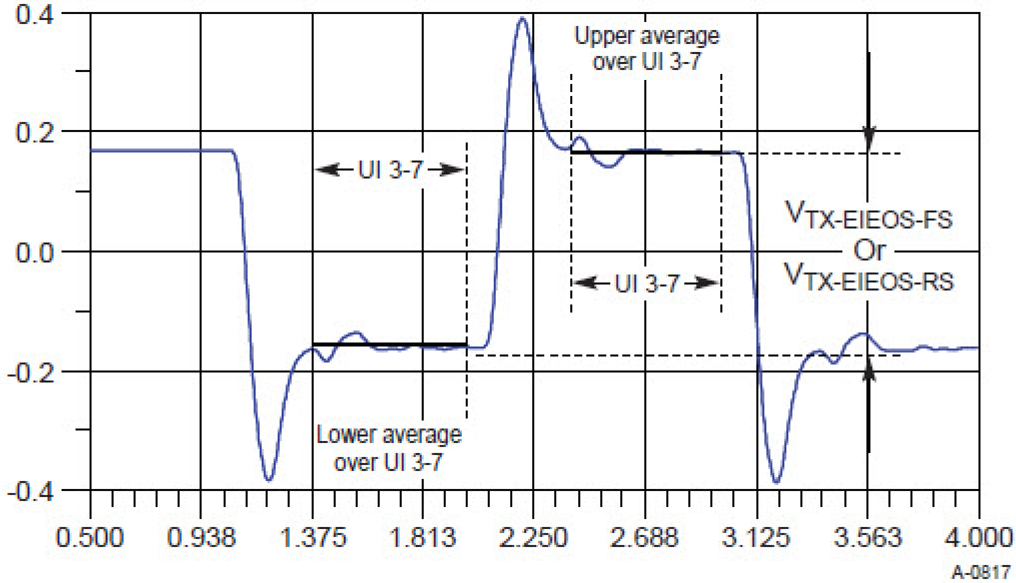


Figure 89 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTestWrapper tools.
7. Finds and updates the worst case test result values.
8. Gets the average EIEOS high voltage.
9. Gets the average EIEOS low voltage.
10. Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 79 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

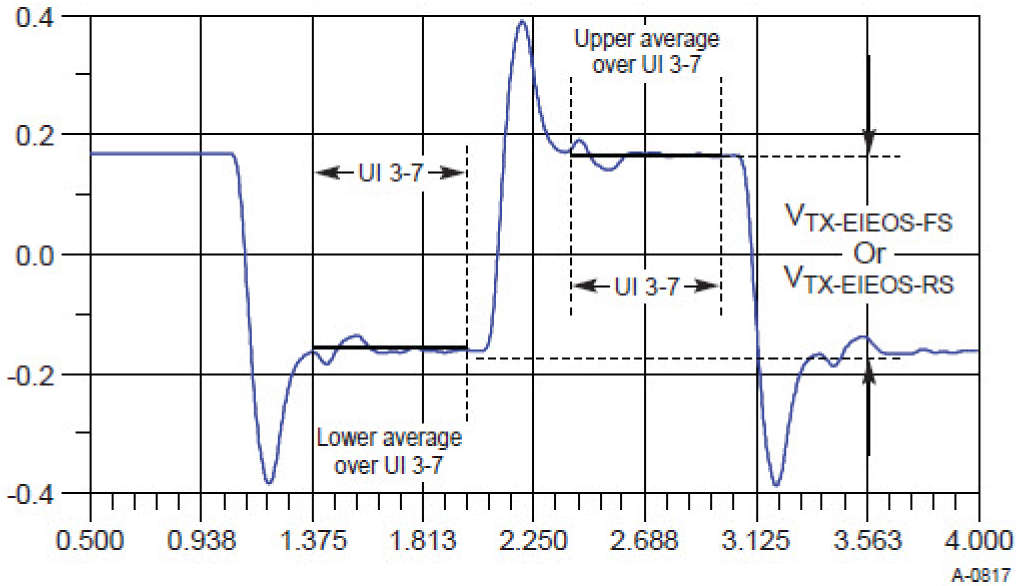


Figure 90   Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 80 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	27.55 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 81 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	12 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 82 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	24 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 83 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	10 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V111) against a 1010 pattern (V101). Tx package loss measurement is made with c-1 and c+1 both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V101 and V111. Multiple measurements shall be made and averaged to obtain stable values for V101 and V111. Due to the HF content of V101, ps21 TX measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V101 and V111 is made towards the end of each interval to minimize ISI and low frequency effects. V101 is defined as the peak-peak voltage between minima and maxima of the clock pattern. V111 is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 84 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	3.0 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	3.0 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.

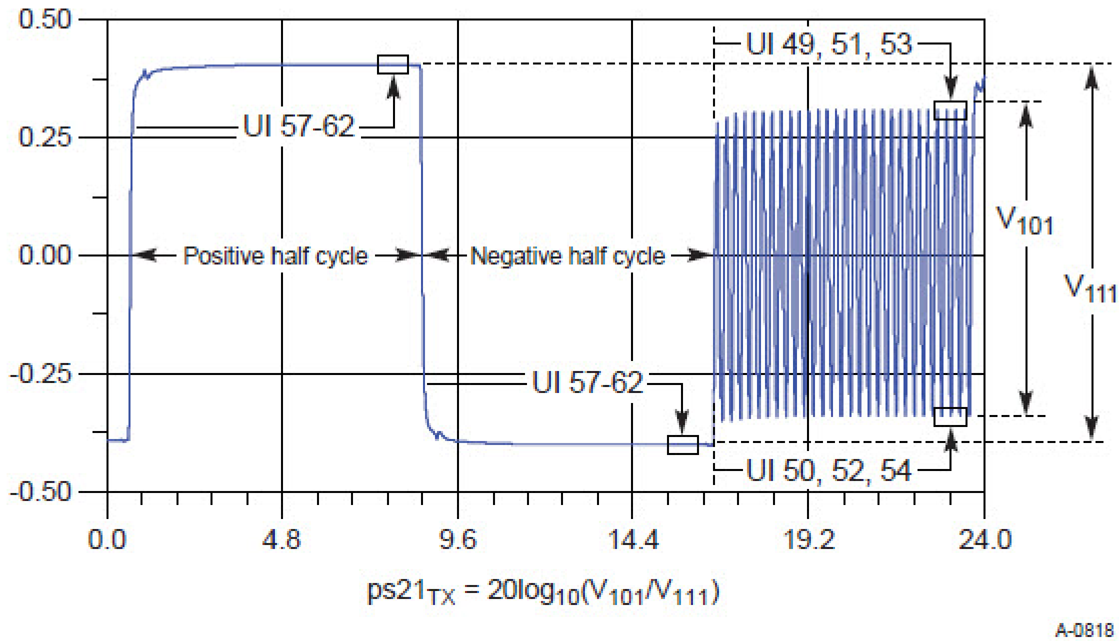


Figure 91 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the number of package loss measurements taken.
8. Reports the package loss ration value.
9. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX-BOOST-FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 85 Tx Boost Ratio Full Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P10.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P10 signal in *.bin format.
13 Inputs the P10 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P10.
15 Reports the measurement of Vb during preset values P10 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX\text{-}BOOST\text{-}RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 86 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}BOOST\text{-}RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 5.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 87 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.17 - 1.97 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the data dependent value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 88 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

a Enables and displays common mode measurements.

b Loads common mode signal to waveform memory.

c Loads and enhance dynamic range D+ signal and D- signal.

d Enables the average common mode measurement.

e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

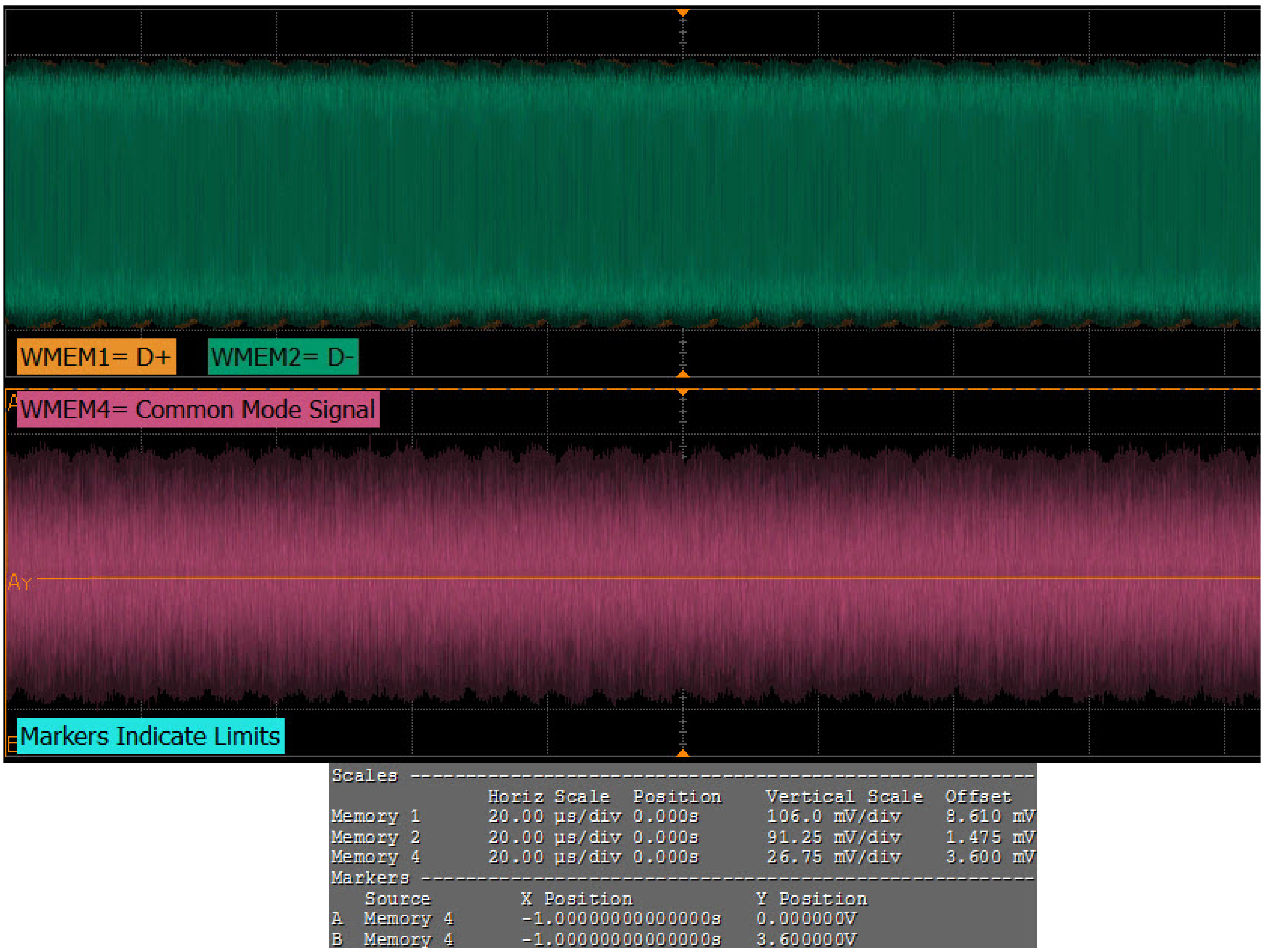


Figure 92 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 4 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 89 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- VTX-AC-CM-PP is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Figure 93 Reference Image for AC-CM voltage (4GHz LPF) Test

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 90 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 4 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

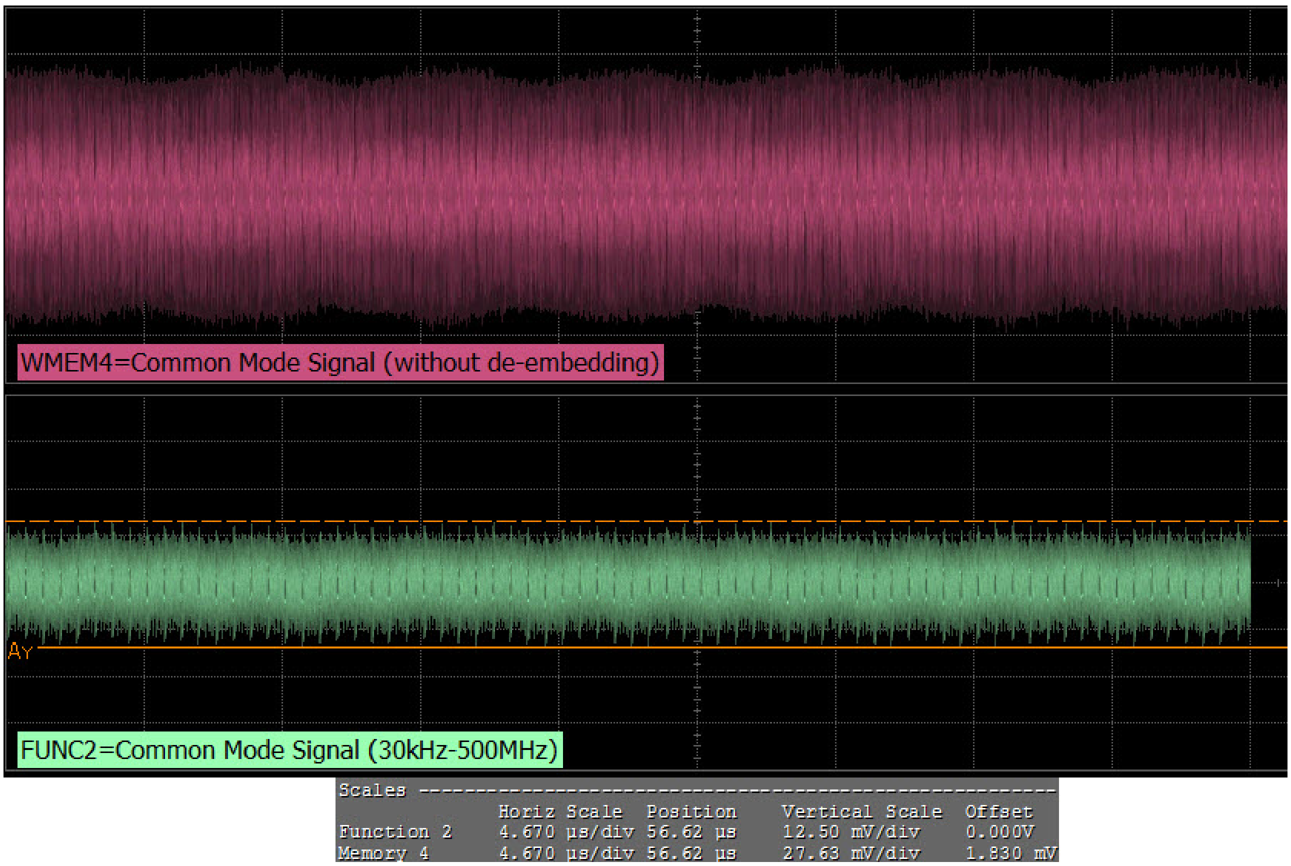


Figure 94 Reference Image for AC-CM voltage (30KHz - 500MHz) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25\ mV$

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 91 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT..

Table 92 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

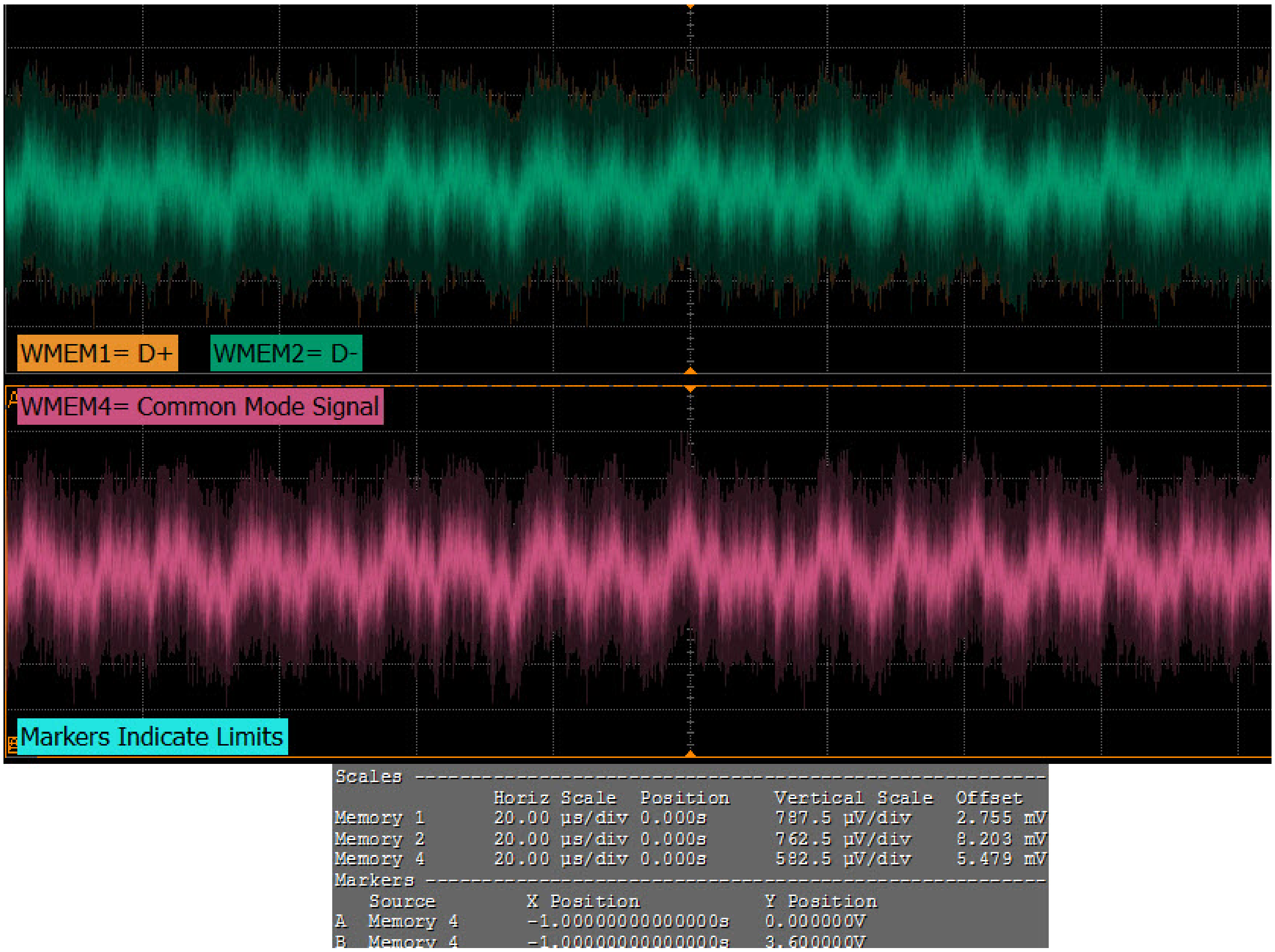


Figure 95 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 93 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 8.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 94 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 8.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 95 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 8.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 96 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   - *a* Generates a differential plot (x_n - x_{n-1}).
   - *b* The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

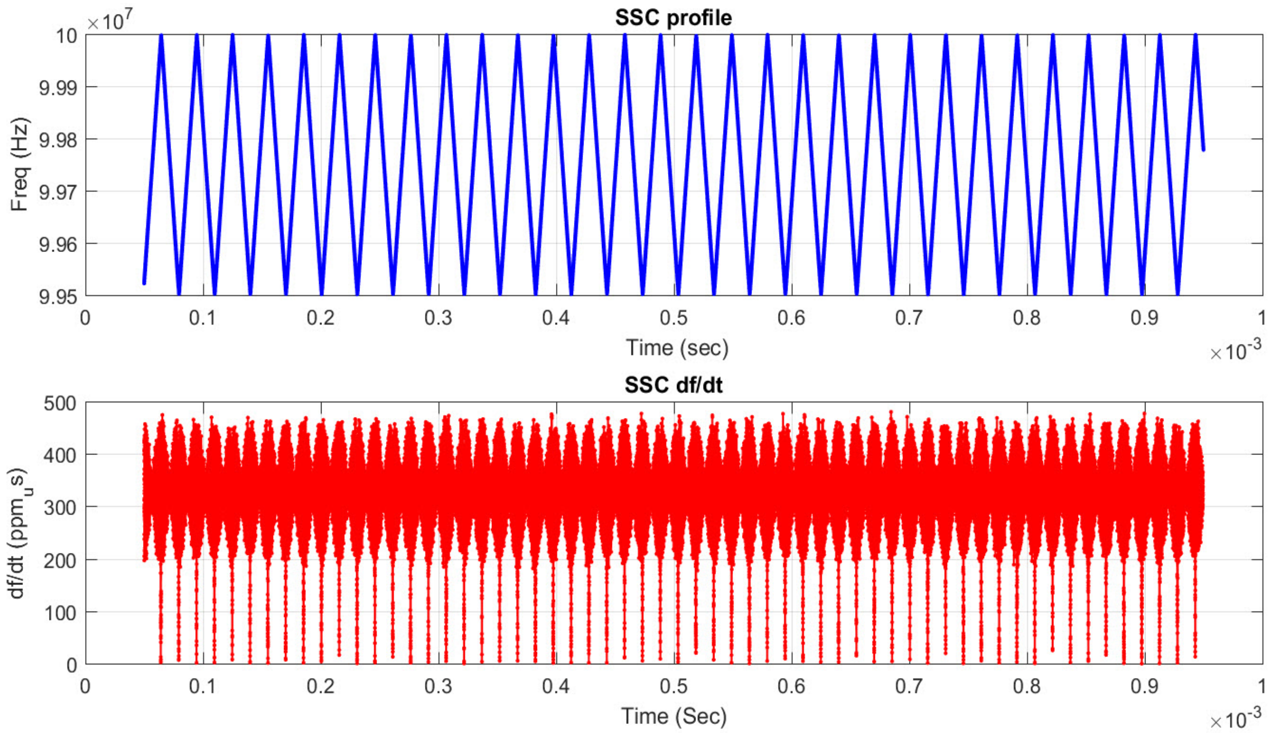


Figure 96 Maximum SSC Slew Rate

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to "Equalization Presets Tests".

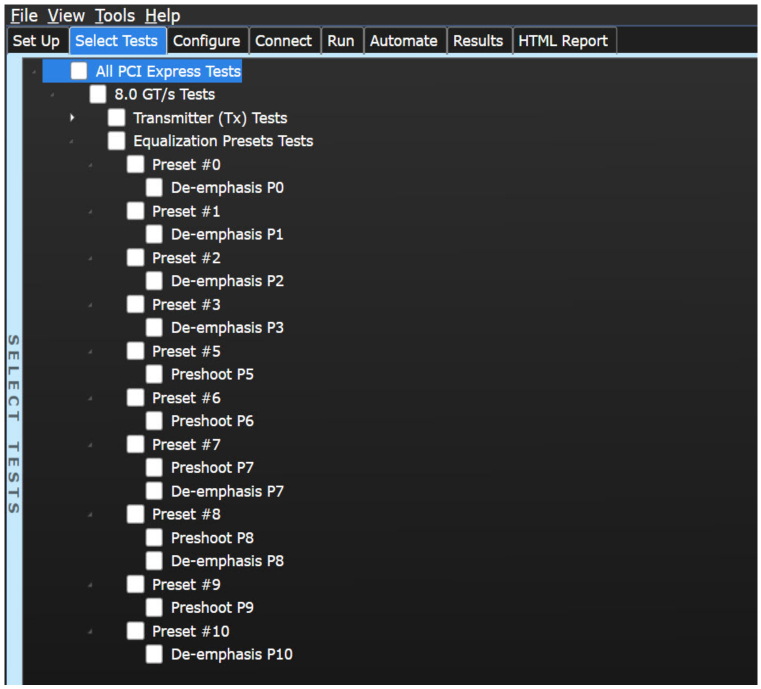


Figure 97 Selecting Equalization Presets Tests

Preset #0 Measurement (P0), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 98.

Table 97 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

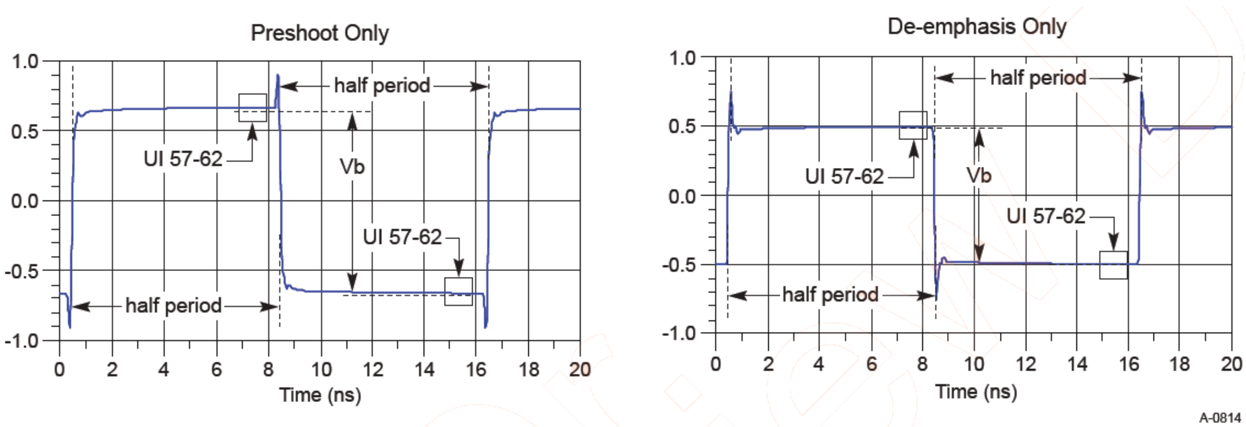


Figure 98 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 98 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	–6.0 ± 1.5 dB	0.000	–0.250	1.000	0.500	0.500

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P0.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P0 signal in *.bin format.
12. Inputs the P4 and P0 saved waveform into SigTest tool.
13. Computes the de-emphasis at preset value P0.
14. Reports the measurement of Vb during preset values P0 and P4.
15. Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (P1), De-emphasis Test

This test verifies that the de-emphasis of the preset number P1 is within the conformance limits as specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 99.

Table 99 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

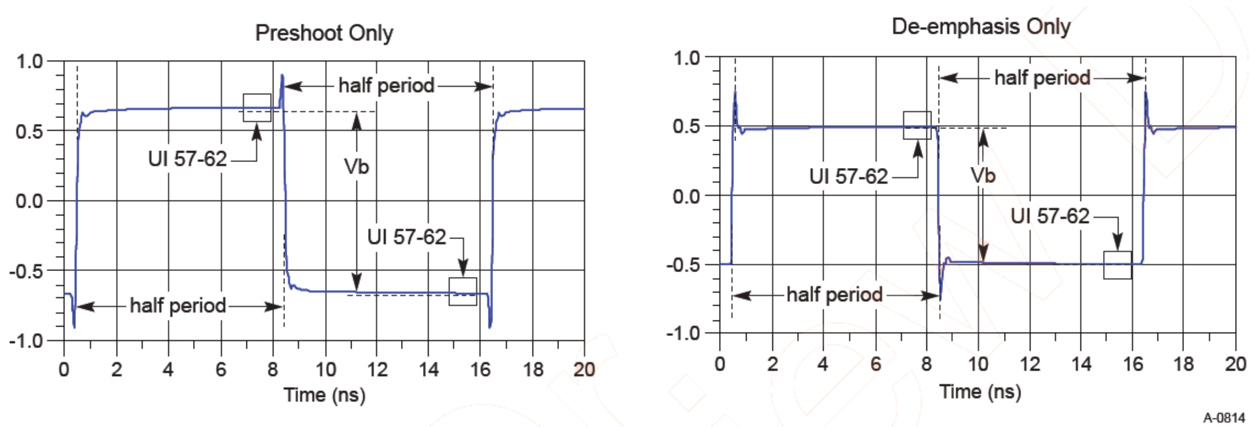


Figure 99 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 100 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	–3.5 ± 1 dB	0.000	–0.167	1.000	0.668	0.668

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P1.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P1 signal in *.bin format.
12. Inputs the P4 and P1 saved waveform into SigTest tool.
13. Computes the de-emphasis at preset value P1.
14. Reports the measurement of Vb during preset values P1 and P4.
15. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 100.

Table 101 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

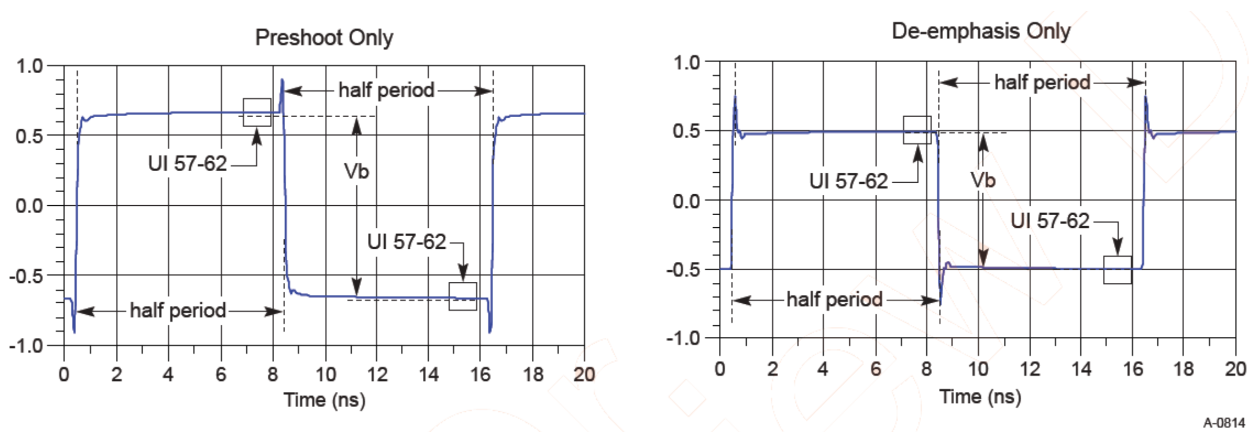


Figure 100 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 102 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	–4.4 ± 1.5 dB	0.000	–0.200	1.000	0.600	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain** Scale to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P2.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P2 signal in *.bin format.
12. Inputs the P4 and P2 saved waveform into SigTest tool.
13. Computes the de-emphasis at preset value P2.
14. Reports the measurement of Vb during preset values P2 and P4.
15. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis Test

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 101.

Table 103 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

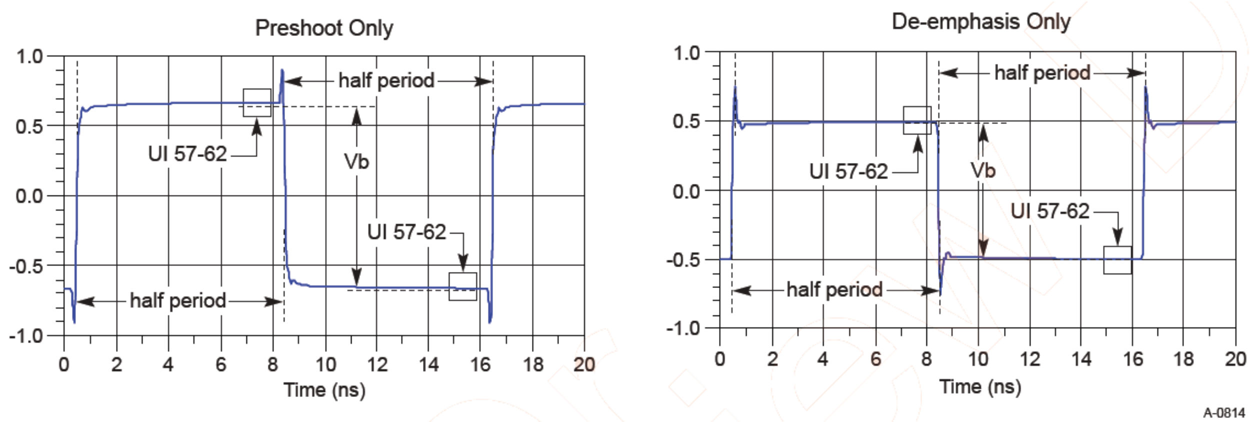


Figure 101 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 104 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	–2.5 ± 1 dB	0.000	–0.125	1.000	0.750	0.750

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P3.
14 Reports the measurement of Vb during preset values P1 and P3.
15 Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot Test

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 102

Table 105 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

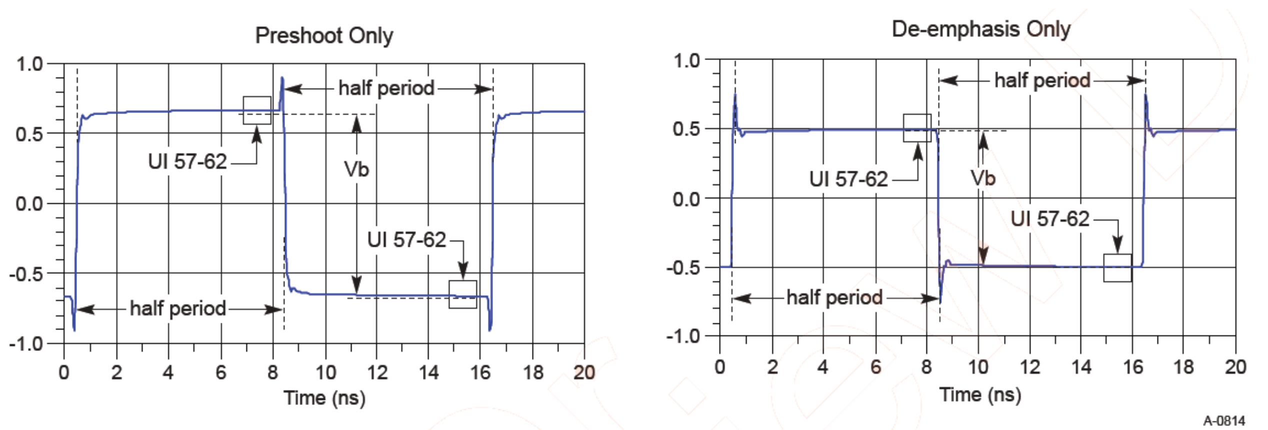


Figure 102 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 106 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	−0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P5.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P5 signal in *.bin format.
12 Inputs the P4 and P5 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P5.
14 Reports the measurement of Vb during preset values P4 and P5.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot Test

This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 103.

Table 107 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

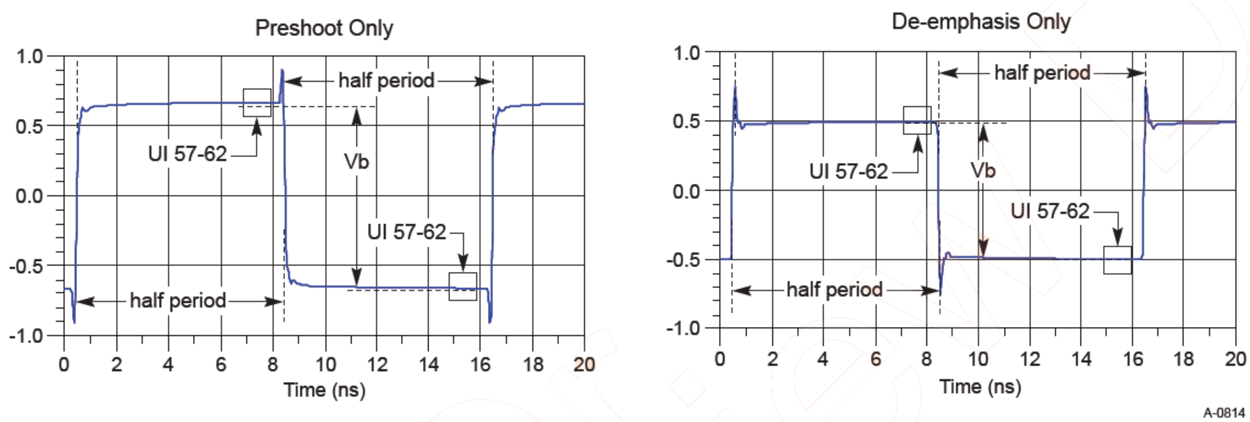


Figure 103 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 108 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	–0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P6.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P6 signal in *.bin format.
12. Inputs the P4 and P6 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P6.
14. Reports the measurement of Vb during preset values P6 and P4.
15. Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot Test

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 104.

Table 109 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

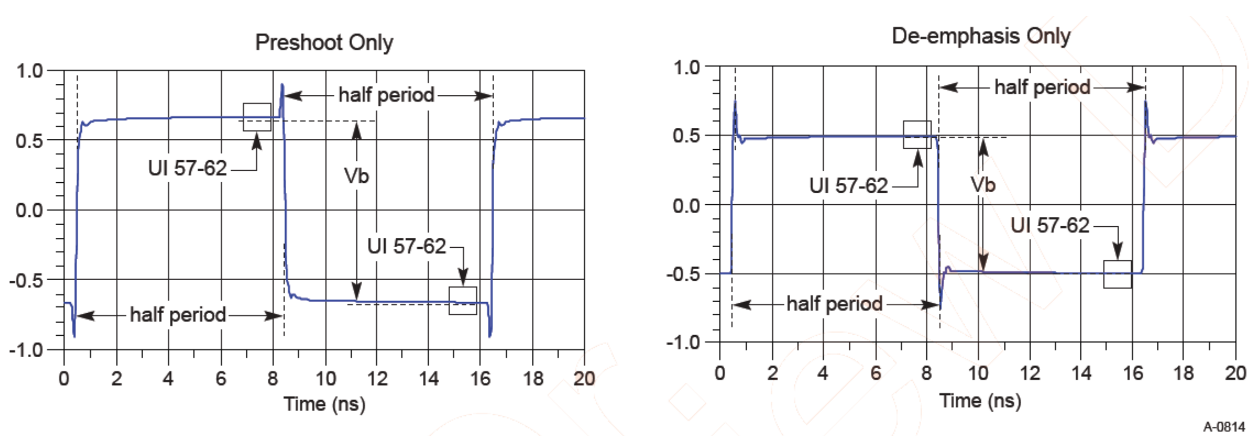


Figure 104 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 110 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P2.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P2 signal into *.bin format.
7. Configures the DUT to operate in preset value #P7.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P7 signal in *.bin format.
12. Inputs the P2 and P7 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P7.
14. Reports the measurement of Vb during preset values P2 and P7.
15. Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis Test

This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 105.

Table 111 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

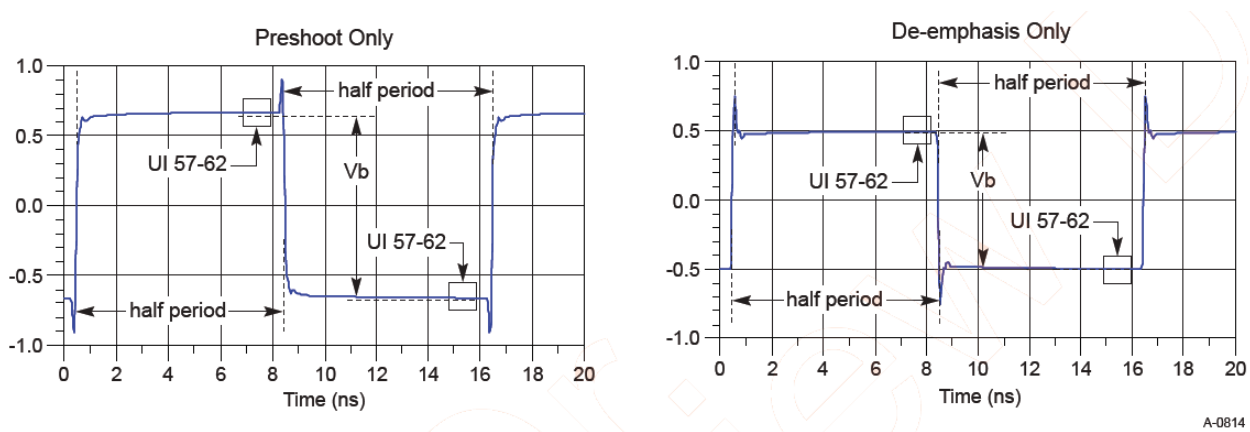


Figure 105 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 112 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P5.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P5 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P5 and P7 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P7.
14 Reports the measurement of Vb during preset values P5 and P7.
15 Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot Test

This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 106.

Table 113 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

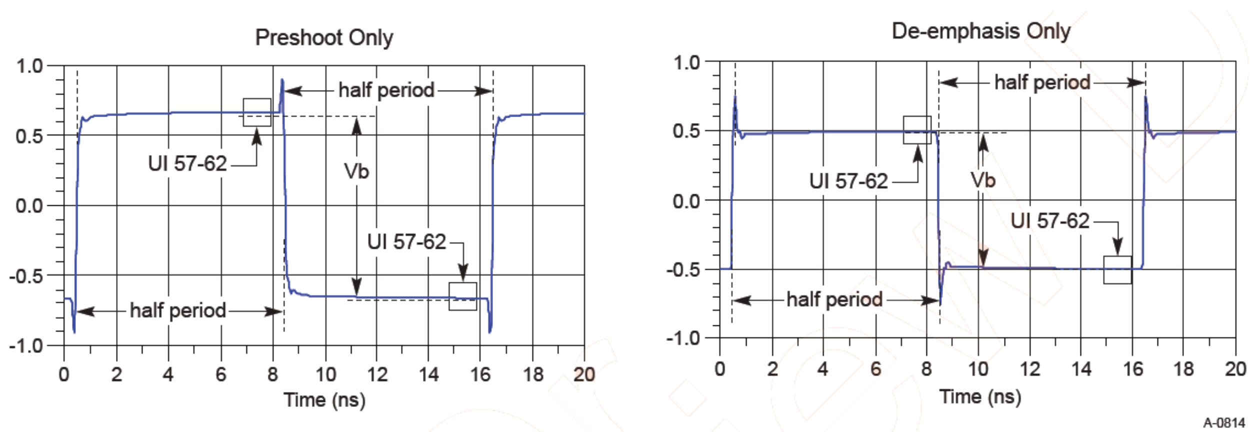


Figure 106 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 114 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P3.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P3 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P3 and P8 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P8.
14 Reports the measurement of Vb during preset values P3 and P8.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis Test

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 107.

Table 115 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

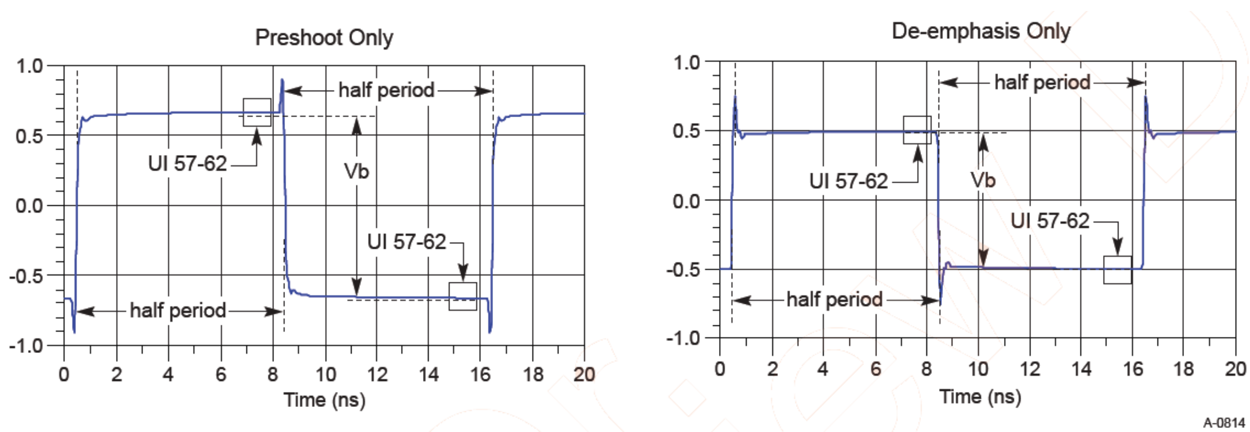


Figure 107 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 116 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P6.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P6 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P6 and P8 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P8.
14 Reports the measurement of Vb during preset values P6 and P8.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot Test

This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 108.

Table 117 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

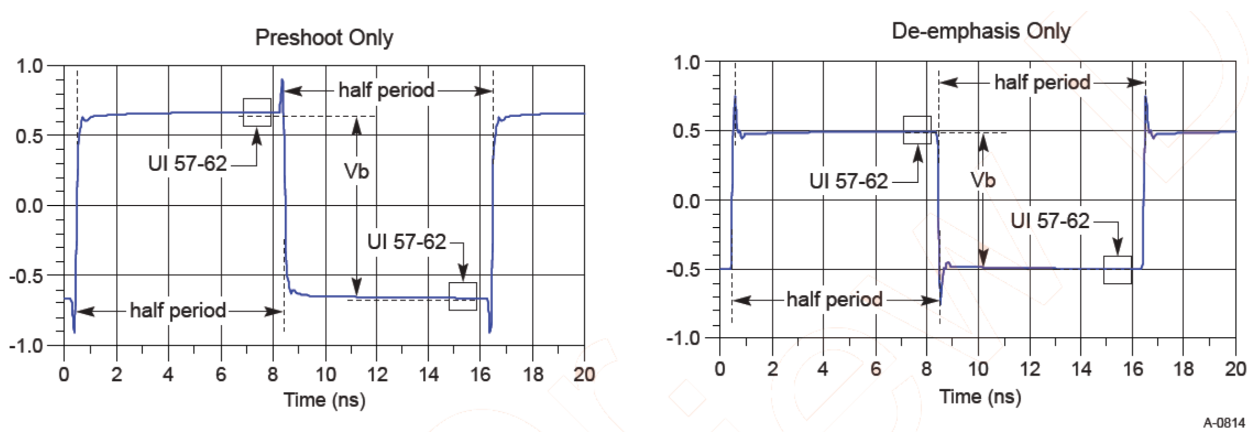


Figure 108 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 118 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P9.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P9 signal in *.bin format.
12. Inputs the P4 and P9 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P9.
14. Reports the measurement of Vb during preset values P9 and P4.
15. Compares the preshoot value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis Test

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 109.

Table 119 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

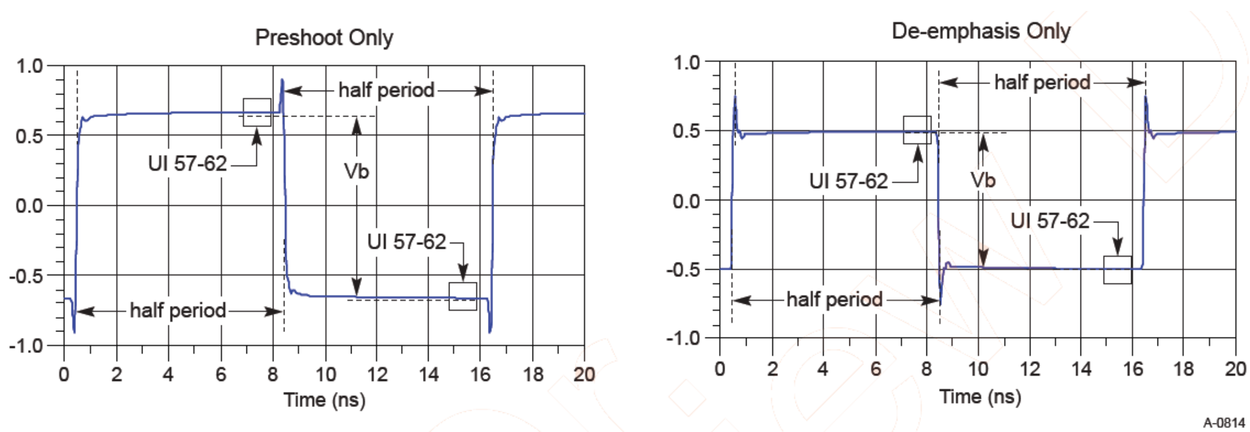


Figure 109 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 120 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	See below Note.	0.000	See below Note.	1.000	See below Note.	See below Note.

Test Definition Notes from the Specification

P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P10.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P10 signal in *.bin format.
12. Inputs the P4 and P1 saved waveform into SigTest tool.
13. Computes the de-emphasis at preset value P10.
14. Reports the measurement of Vb during preset values P10 and P4.
15. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

13 CEM-EndPoint Tests, 8.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-EndPoint tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB, and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test).

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running CEM-EndPoint Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 8.0 GT/s Tests > CEM EndPoint Tests**.

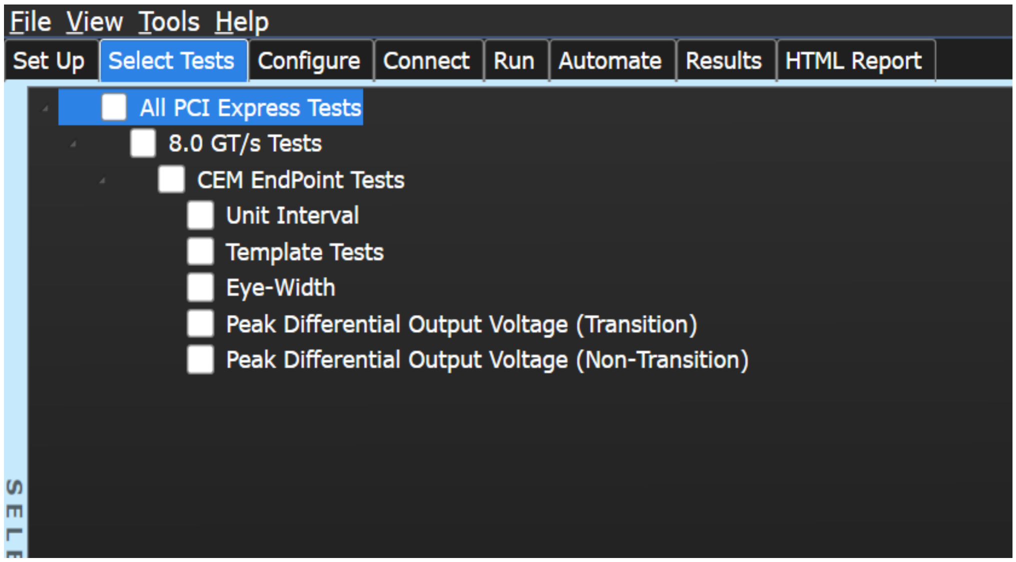


Figure 110 Selecting CEM EndPoint Tests

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The worst case recovered TX UI is reported here. The UI range is not specified for this test point. It is provided here as informative data only.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 121 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	124.9625 ps	125.0375 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Fits and displays all sample data on screen.
3. Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a. Selects **Unit Interval** as data measurement analysis unit.
   b. Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

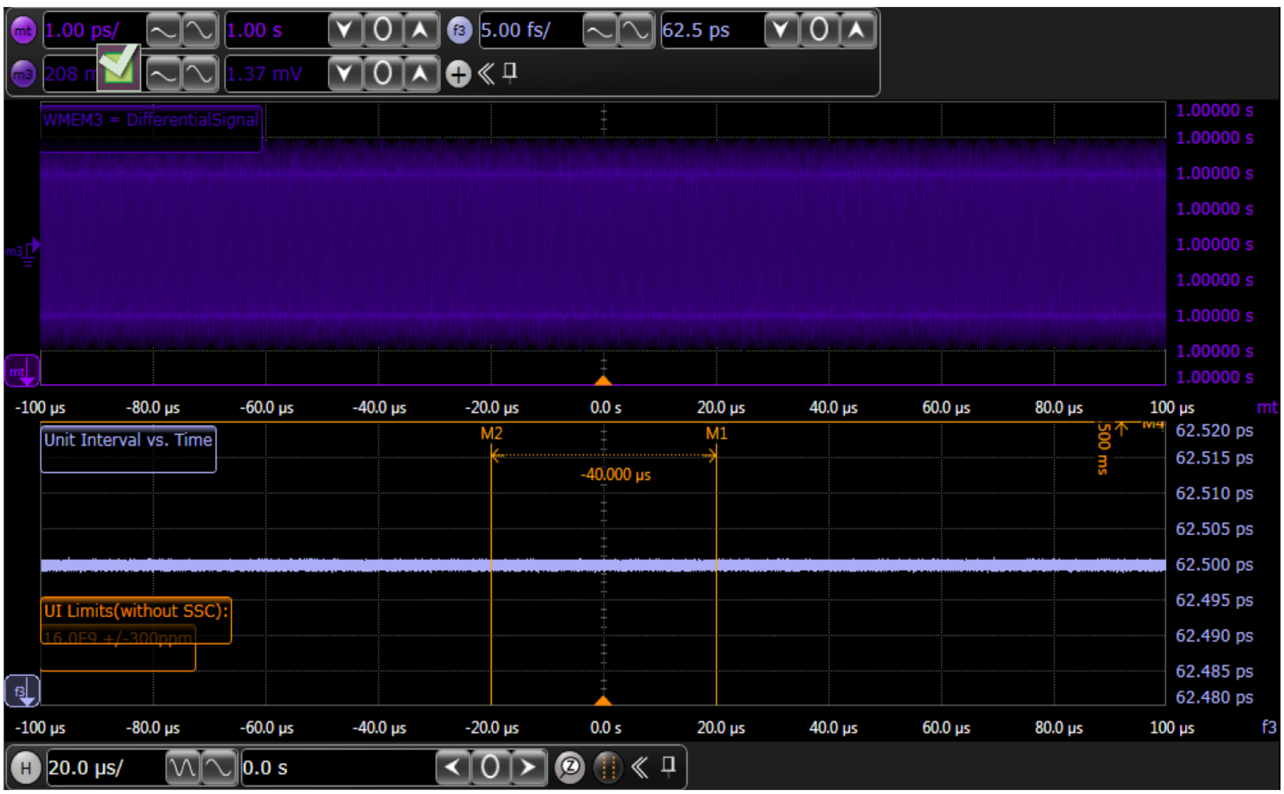


Figure 111 Reference Image for Unit Interval Test

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.15, Table 4-28 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_{A_d}).

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.1, Figure 4-7 is used as reference to check the compliance of the DUT.

Table 122 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	34.00 mV	1300 mV	Notes 1, 2, 4
V_{TXS_d}	34.00 mV	1300 mV	Notes 1, 2, 4
T_{TXS}	41.25 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 1 ps RMS jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and $V_{TXA_}$d are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

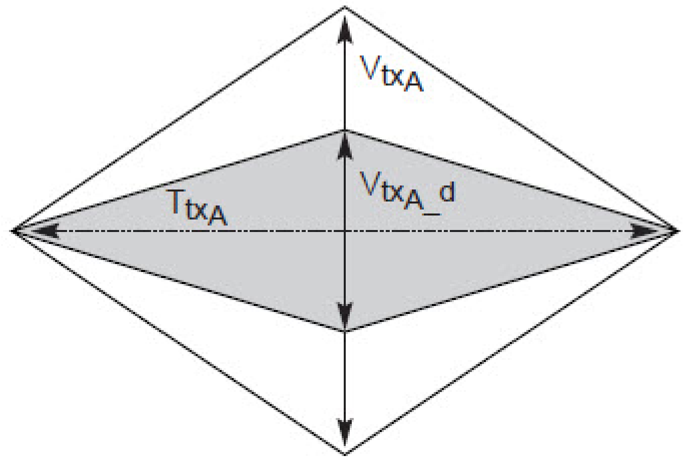


Figure 112 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs compliance testing using the SigTestWrapper.dll file.
   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

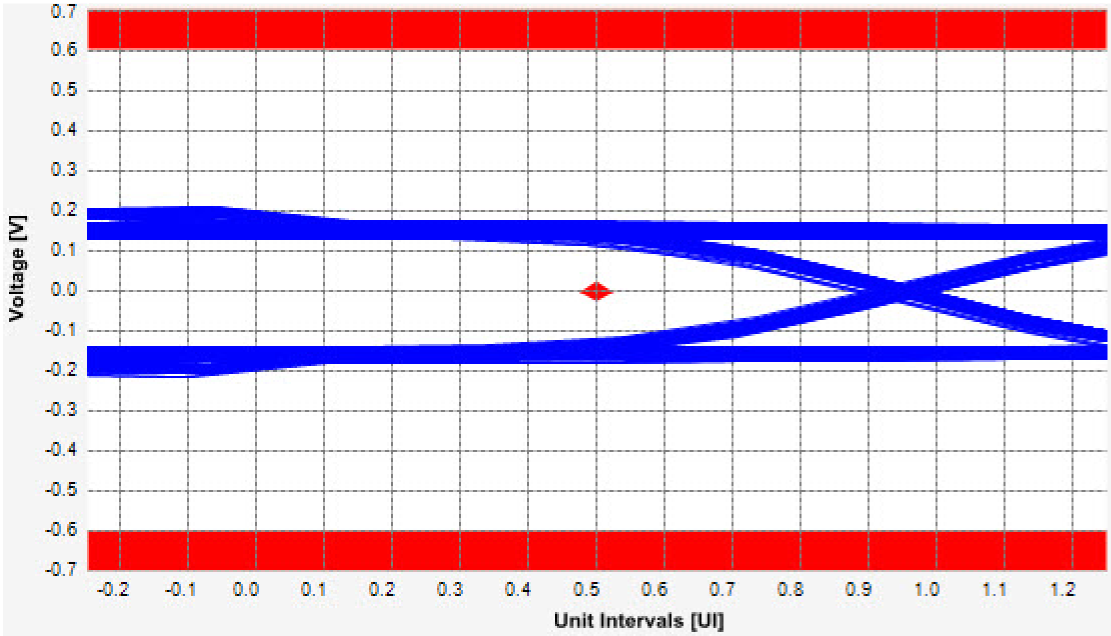


Figure 113 Reference Image for Template (Transition) Test

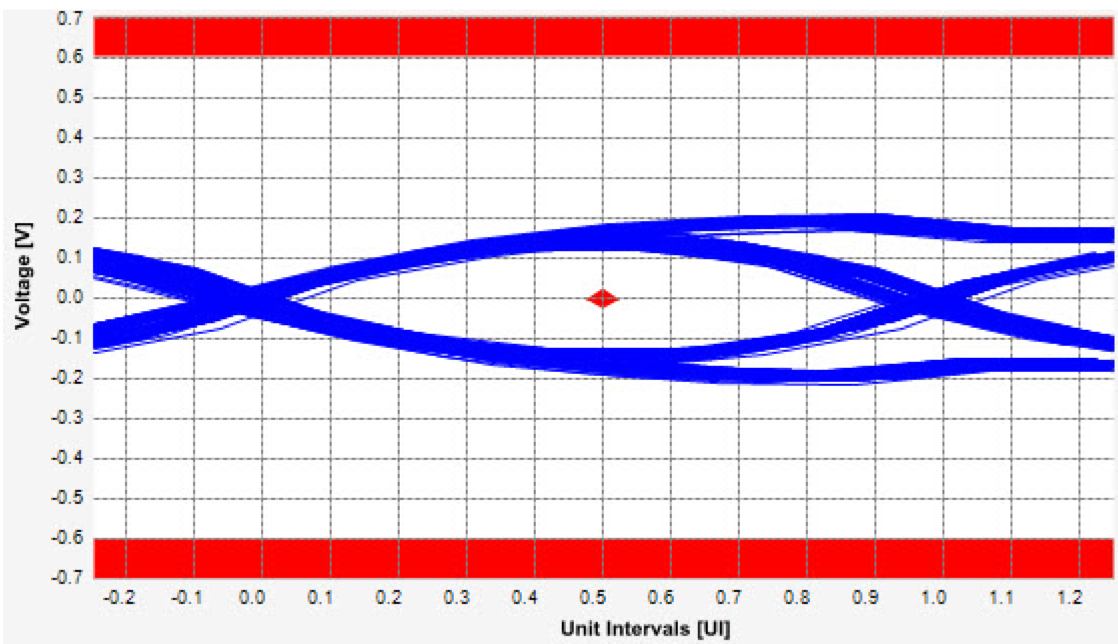


Figure 114 Reference Image for Template (Non-Transition) Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.3, Table 4-14 is used as reference to check the compliance of the DUT.

Table 123 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max	Comments
T_{TXA}	41.25 ps	N/A	Notes 1, 3, 4

Test Definition Notes from the Specification

1. A worst-case reference clock with 1 ps RMS jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA}_d are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

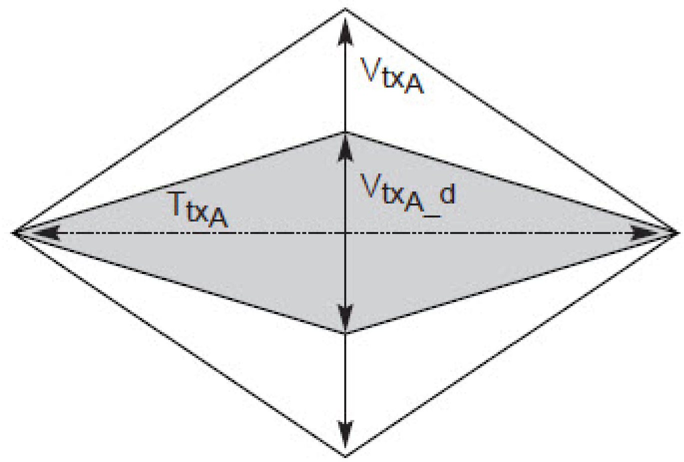


Figure 115 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 8.0 GT/s

1. Obtains the eye-width test results from SigTestWrapper.dll file.
2. Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3. Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.3 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.3, Table 4-14 is used as reference to check the compliance of the DUT.

Table 124 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max	Comments
$V_{TX-DIFF-PP}$	34 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 1 ps RMS jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA}_d are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

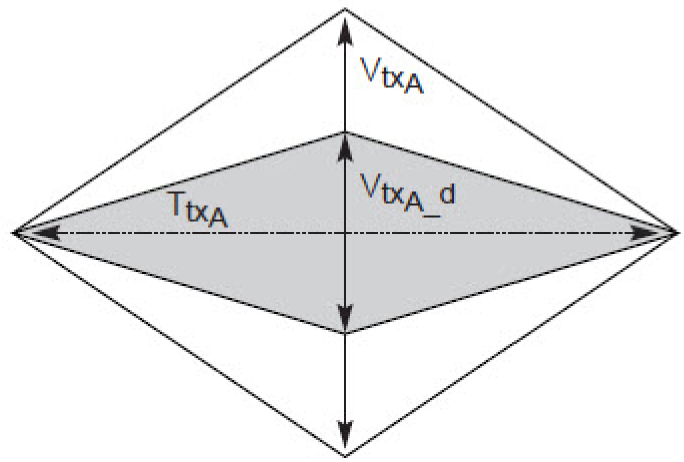


Figure 116 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 8.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

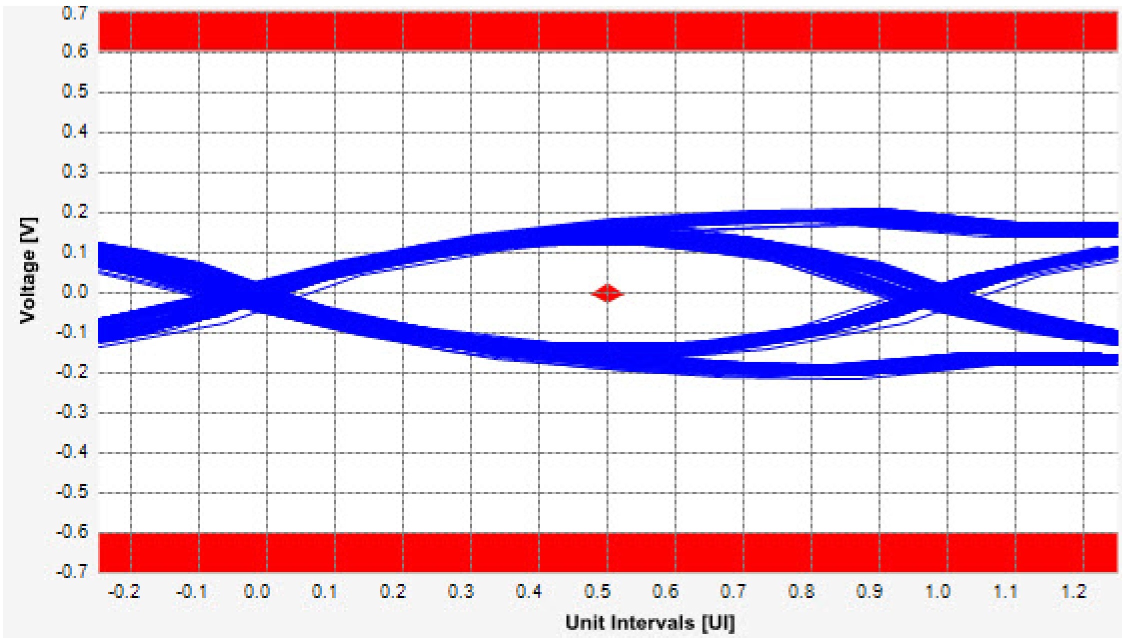


Figure 117 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.3, Table 4-14 is used as reference to check the compliance of the DUT.

Table 125 Peak Differential Output Voltage (Non-transition) Test Details

Symbol	Min	Max	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	34 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 1 ps RMS jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA}_d are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 Ω trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

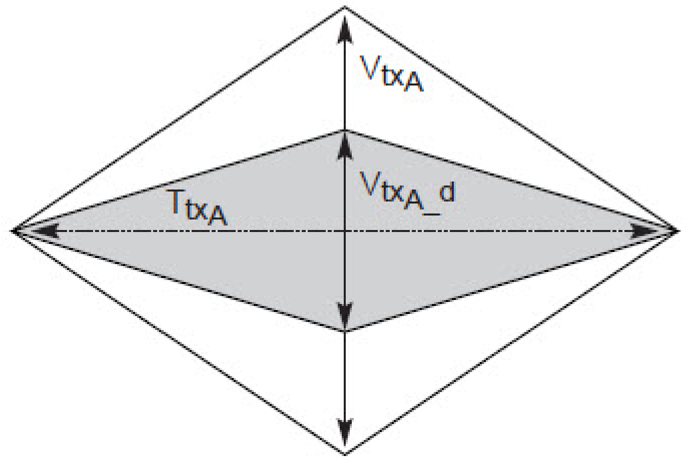


Figure 118 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> This test requires the template test with the following specifications:
>
> Device: PCIE 5.0
>
> Data Rate: 8.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

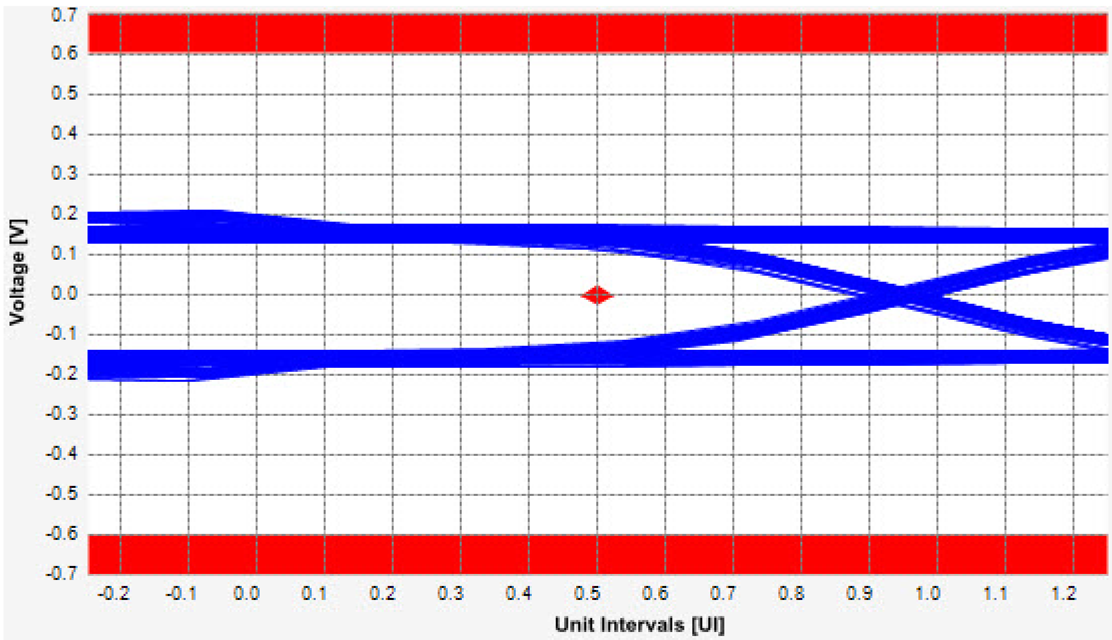


Figure 119 Reference Image for Peak Differential Output Voltage Test

14 CEM-RootComplex Tests, 8.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-RootComplex tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

KEYSIGHT TECHNOLOGIES

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1. With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.
   The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.
2. Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.
3. Connect cables up as follows:
   - *a* Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR
   - *b* Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running CEM-RootComplex Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 8.0 GT/s Tests > CEM RootComplex Tests**.

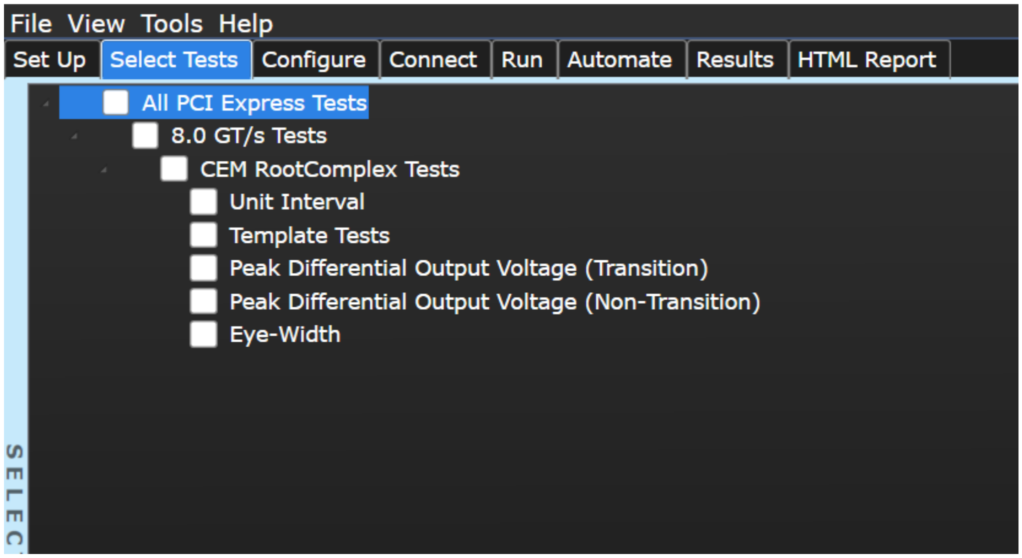


Figure 120 Selecting System Board (Tx) Tests

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^th 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 126 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	124.9600 ps	125.0375 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

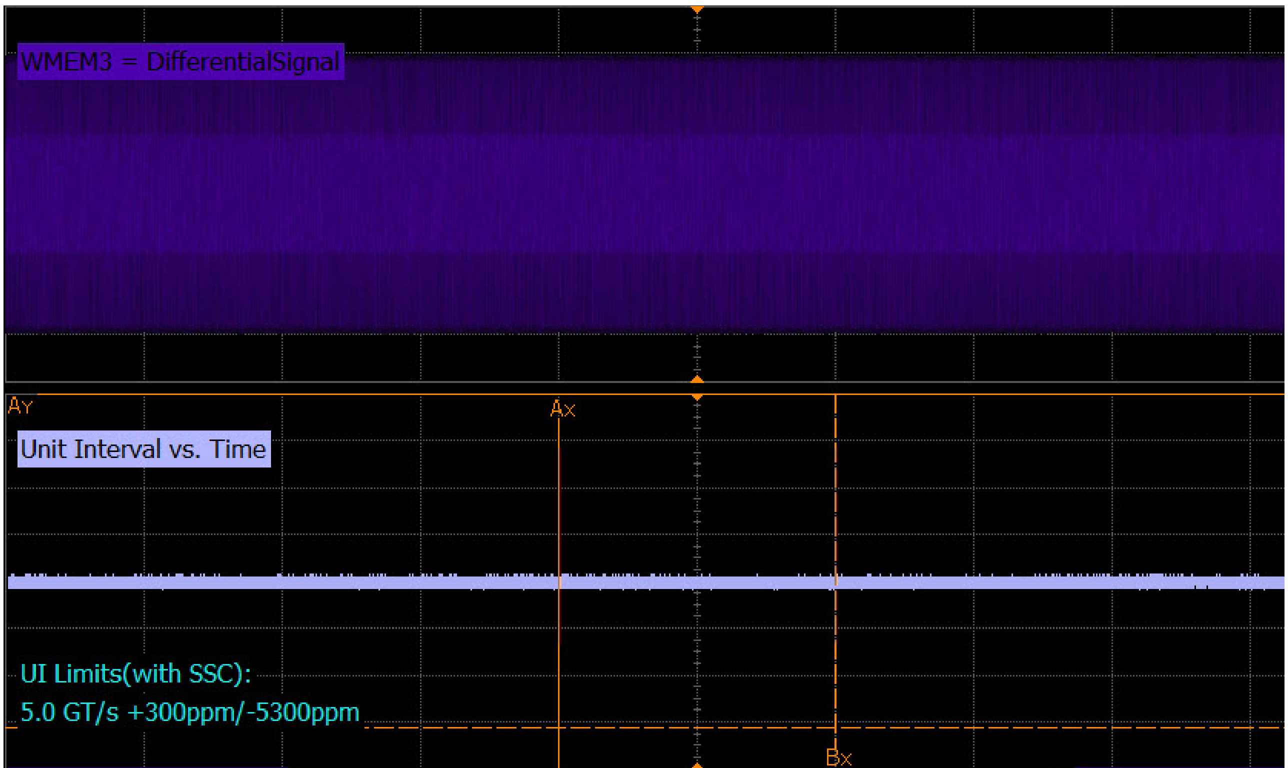
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	162.5 mV/div	3.356 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-32.0000000080000 µs	200 pV
B	Function 3	32.0000000080000 µs	200 pV

Figure 121 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.15, Table 4-28 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.13, Figure 4-9 is used as reference to check the compliance of the DUT.

Table 127 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	34 mV	1300 mV	Notes 1, 2, 4
V_{TXS_d}	34 mV	1300 mV	Notes 1, 2, 4
T_{TXS}	41.25 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

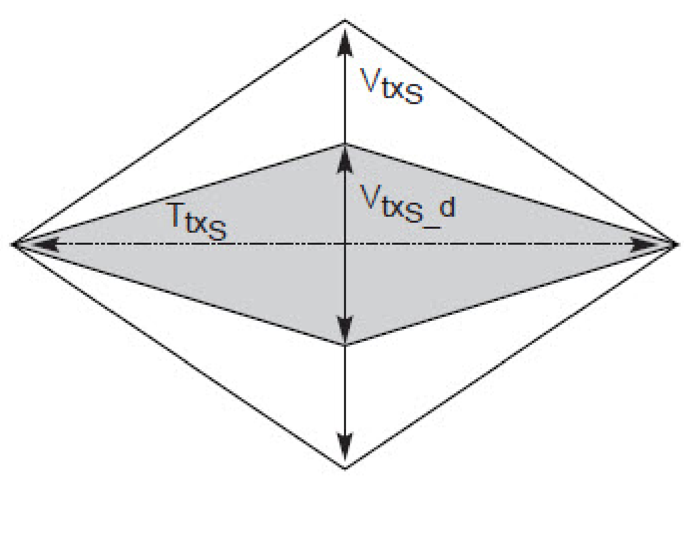


Figure 122 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

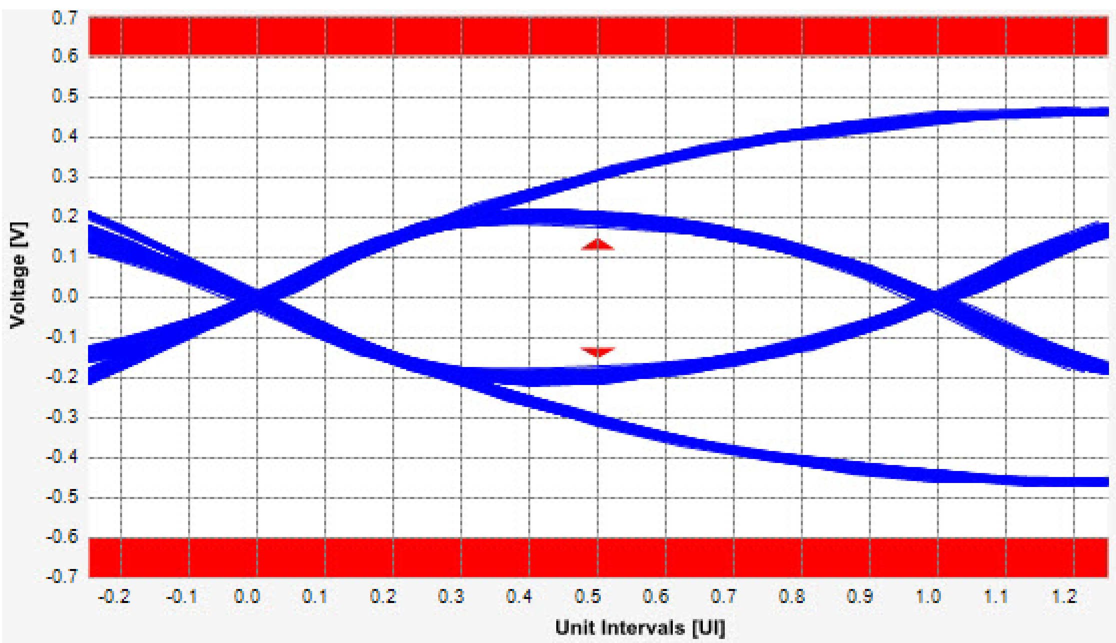


Figure 123 Reference Image for Template (Transition) Test

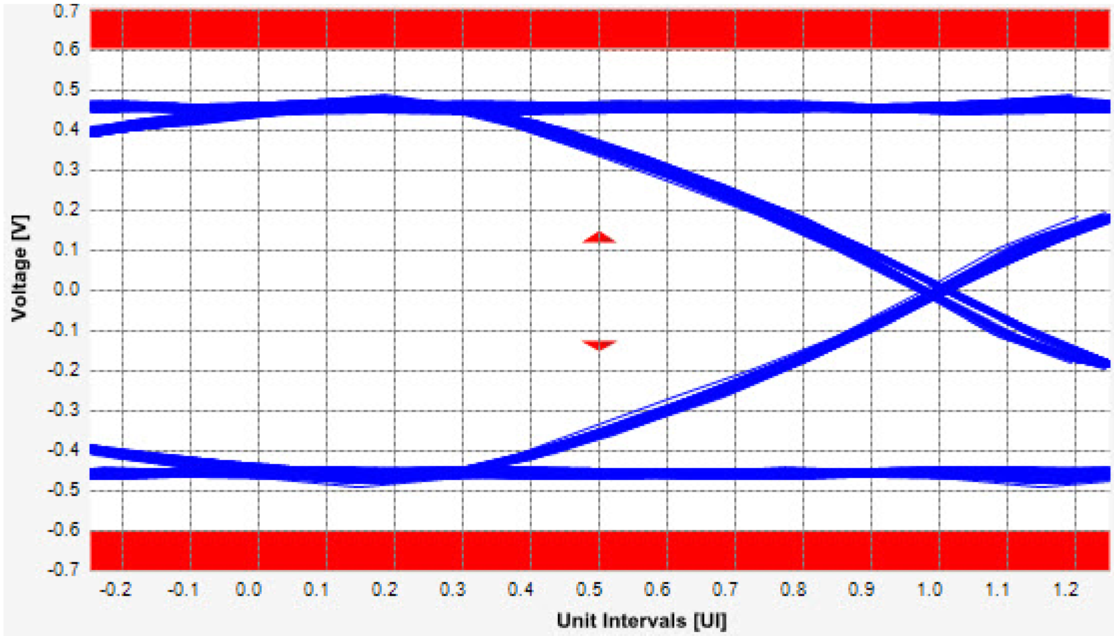


Figure 124 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.15, Table 4-28 is used as reference to check the compliance of the DUT.

Table 128 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	34 mV	1200 mV	Notes 1, 2, 4
V_{TXS_d}	34 mV	1200 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is required to be least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

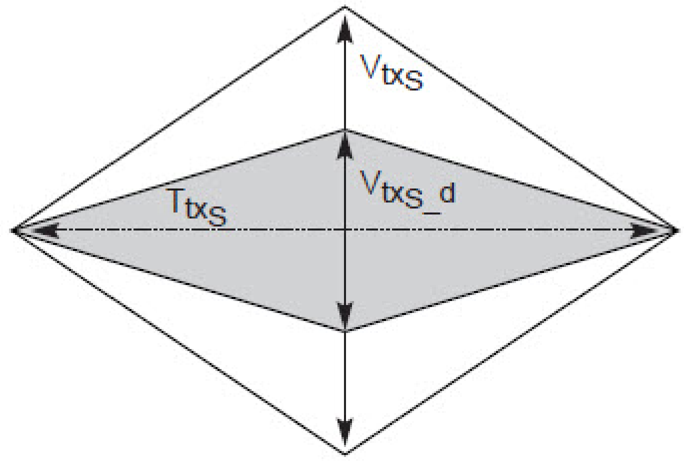


Figure 125 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 8.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

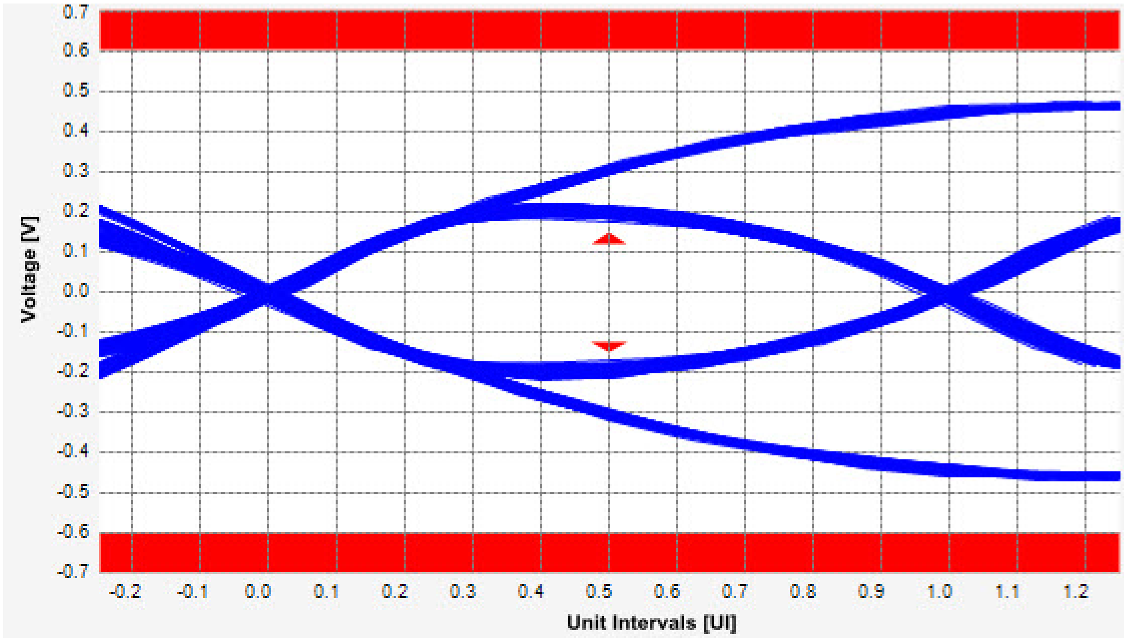


Figure 126 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.15, Table 4-28 is used as reference to check the compliance of the DUT.

Table 129 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	34 mV	1200 mV	Notes 1, 2, 4
V_{TXS_d}	34 mV	1200 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

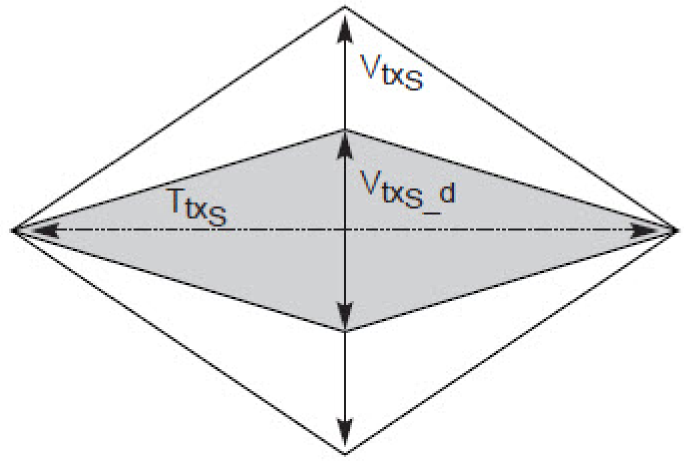


Figure 127 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 8.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

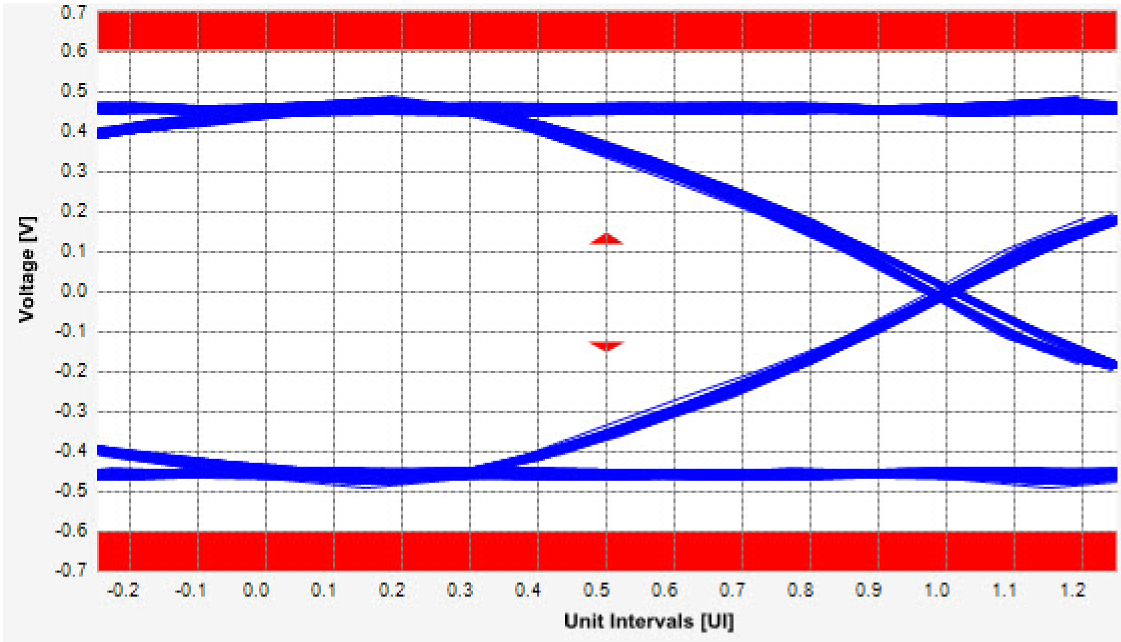


Figure 128 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye - width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.15, Table 4-28 is used as reference to check the compliance of the DUT.

Table 130 Template Test Details

Symbol	Min	Max	Comments
T_{TXS}	41.25 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS}, and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be least 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

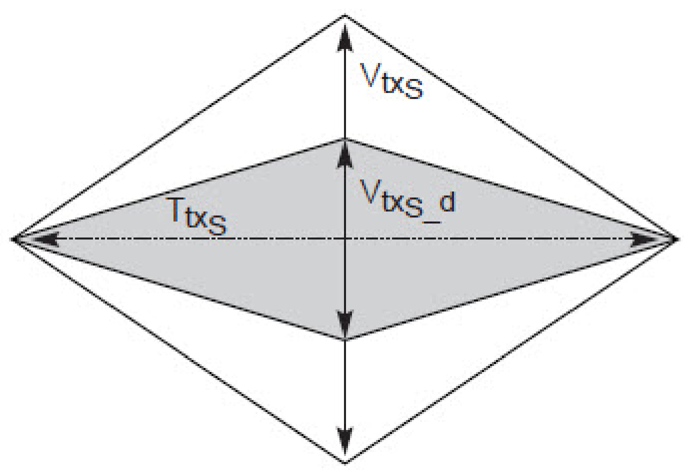


Figure 129 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> This test requires the template test with the following specifications:
>
> Device: PCIE 5.0
>
> Data Rate: 8.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

15 Reference Clock Tests, 8.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe 5.0 Reference Clock tests at 8.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

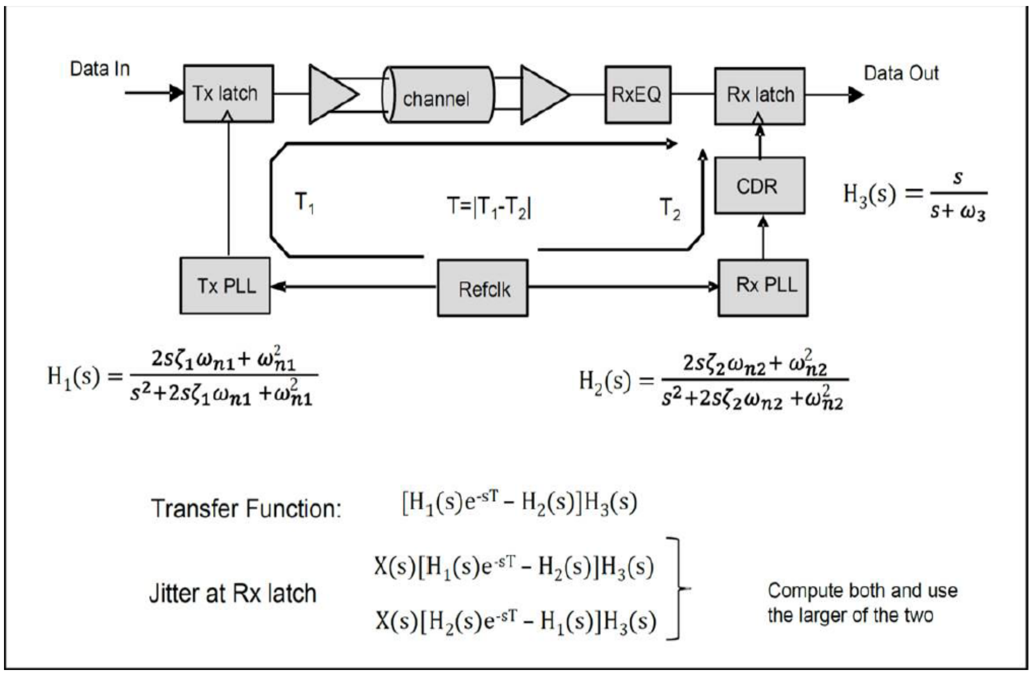
NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 8.0 GT/s, PCI-E 5.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

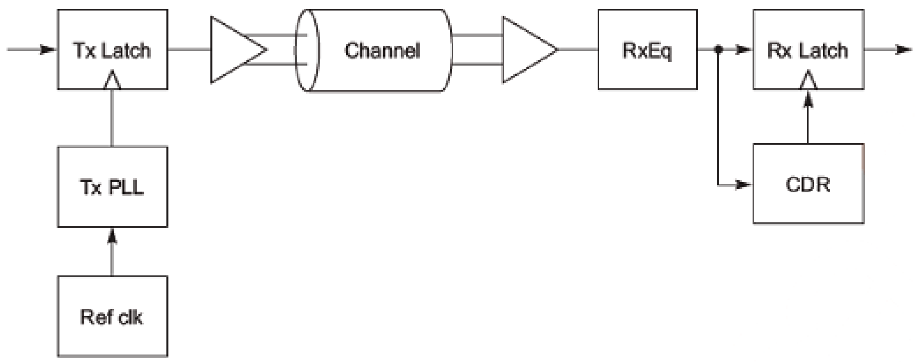
Common Clock Architecture

This section describes the common Refclk Rx architecture.



Data Clock Architecture

This section describes the data driving architecture.



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1}^2 + \omega_{n1}^2}\right] \qquad H_3(s) = \left[\frac{2s\zeta_3\omega_{n3} + \omega_{n3}^2}{s^2 + 2s\zeta_3\omega_{n3}^2 + \omega_{n3}^2}\right]$$

$$H(s) = H_1(s)[1 - H_3(s)]$$

	0.01 dB Peaking	2.0 dB Peaking
$BW_{PLL}(min) =$ 2.0 MHz	$\omega_{n1} = 0.448$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 6.02$ Mrad/s $\zeta_1 = 0.73$
$BW_{PLL}(max) =$ 4.0 MHz	$\omega_{n1} = 0.896$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 12.04$ Mrad/s $\zeta_1 = 0.73$

	0.01 dB Peaking	1.0 dB Peaking
$BW_{PLL}(min) =$ 2.0 MHz	$\omega_{n2} = 0.448$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 4.62$ Mrad/s $\zeta_2 = 1.15$
$BW_{PLL}(max) =$ 5.0 MHz	$\omega_{n2} = 1.12$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 11.53$ Mrad/s $\zeta_2 = 1.15$

	0.5 dB Peaking	2.0 dB Peaking
$BW_{CDR}(min) =$ 10 MHz	$\omega_{n3} = 16.57$ Mrad/s $\zeta_3 = 1.75$	$\omega_{n3} = 33.8$ Mrad/s $\zeta_3 = 0.73$

A-0843

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

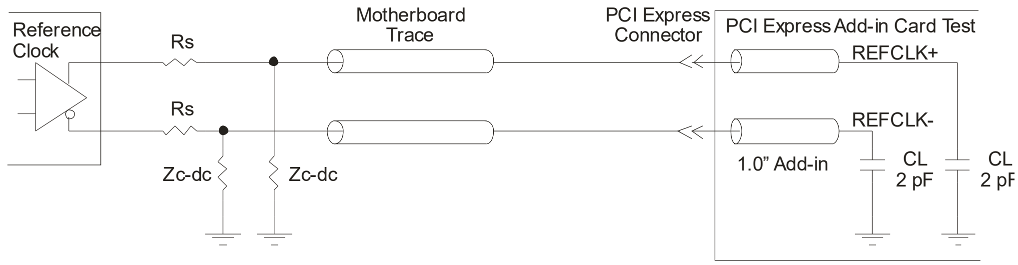


Figure 130 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 8.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

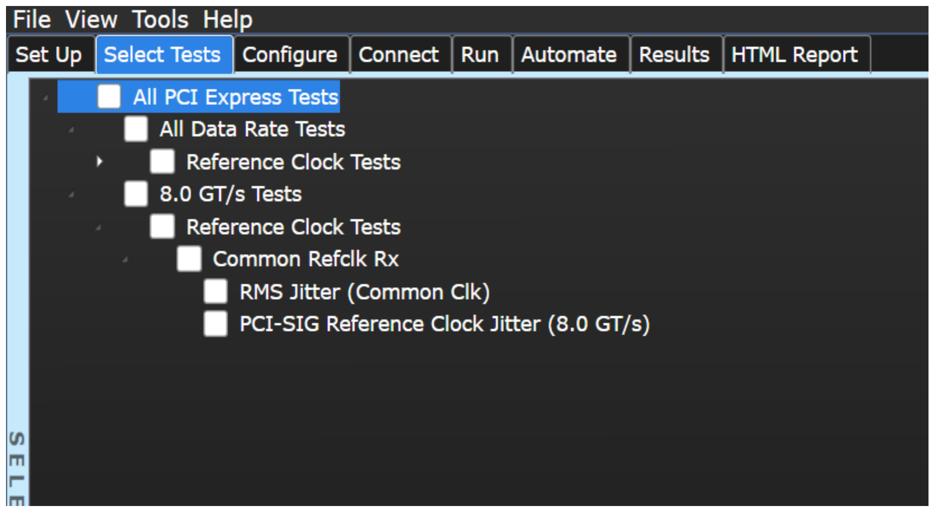


Figure 131 Selecting Reference Clock Tests when Clean Clock or SSC is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 131 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	1.0 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal frequency is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.
10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
  a Converts time domain TIE data to frequency domain.
  b Applies the PLL filter using parameters for common clocked architecture.
  c Converts back the frequency domain TIE data to time domains.
  d Computes the filtered peak-peak jitters and RMS jitter.
11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

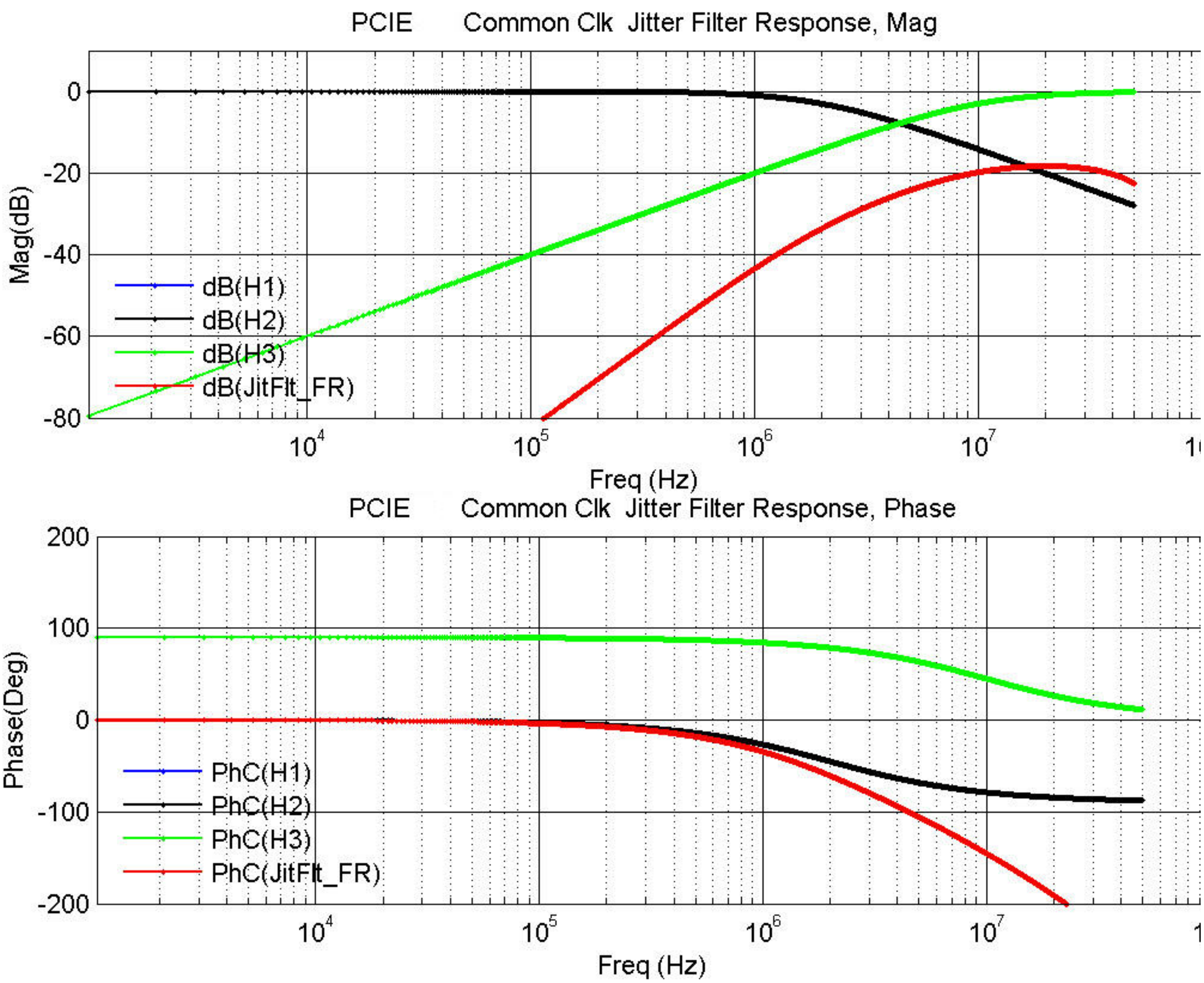


Figure 132 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

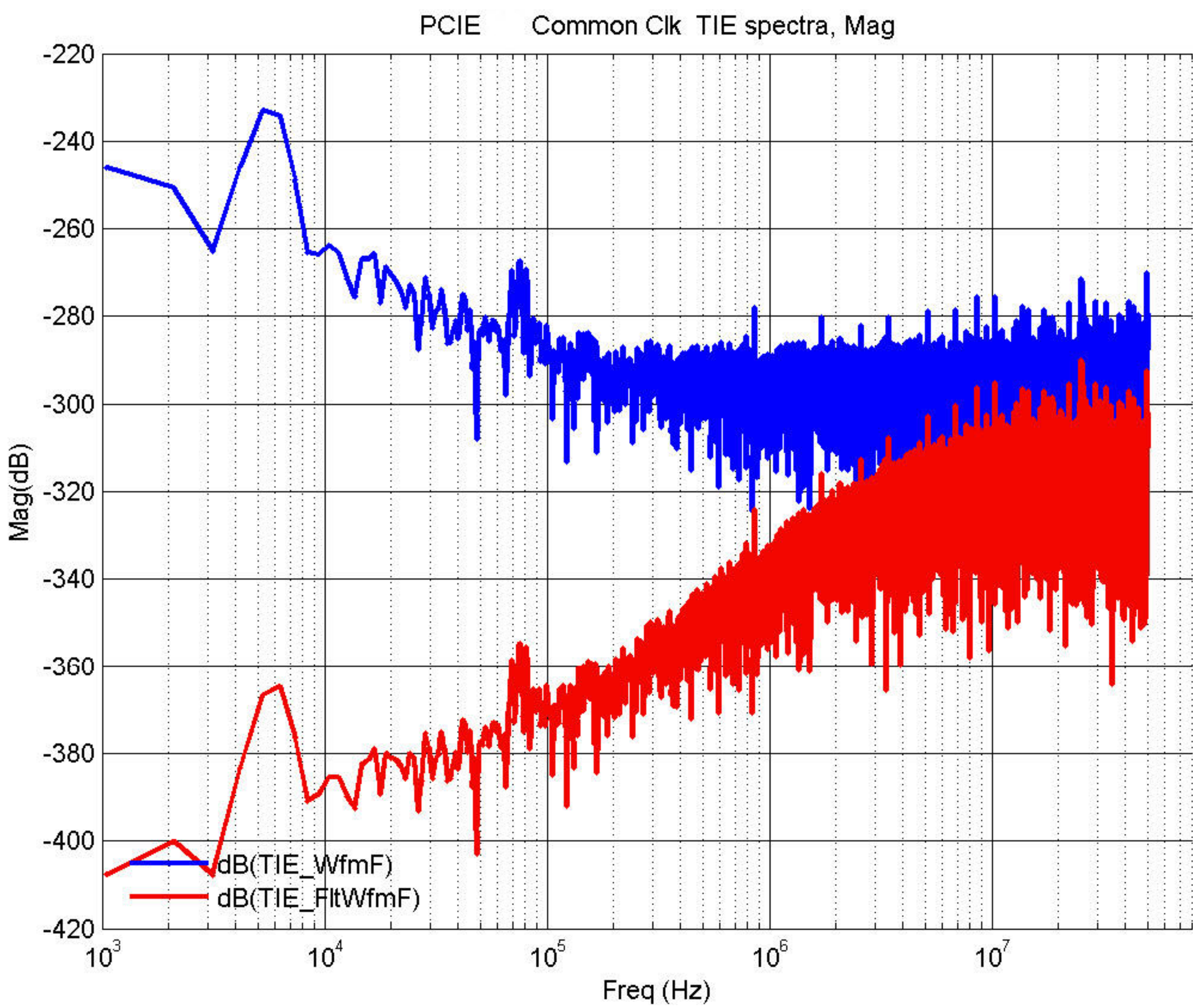


Figure 133 Reference Image for Common Clock TIE Spectra RMS Jitter Test

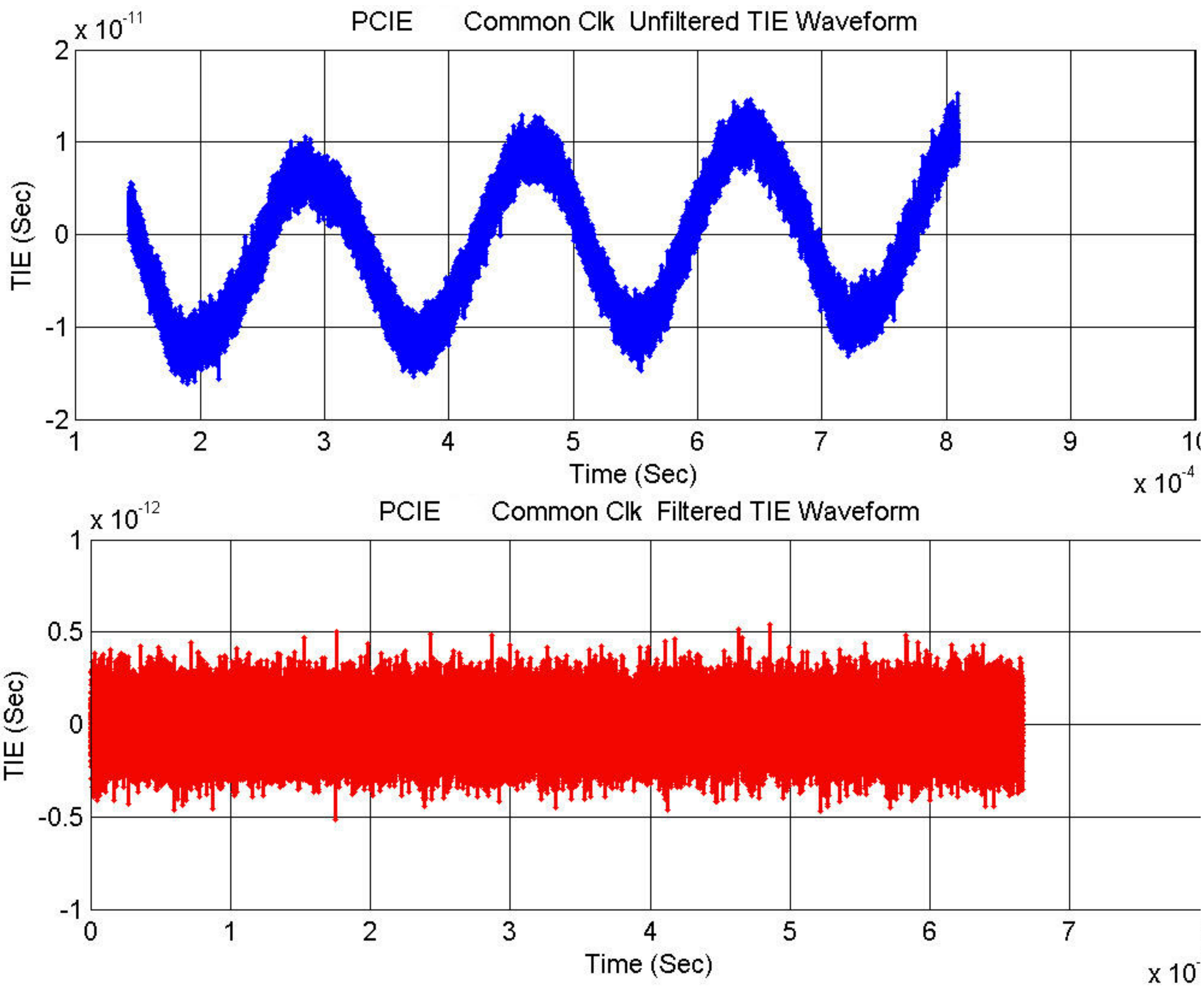


Figure 134 Reference Image for TIE Waveform RMS Jitter Test

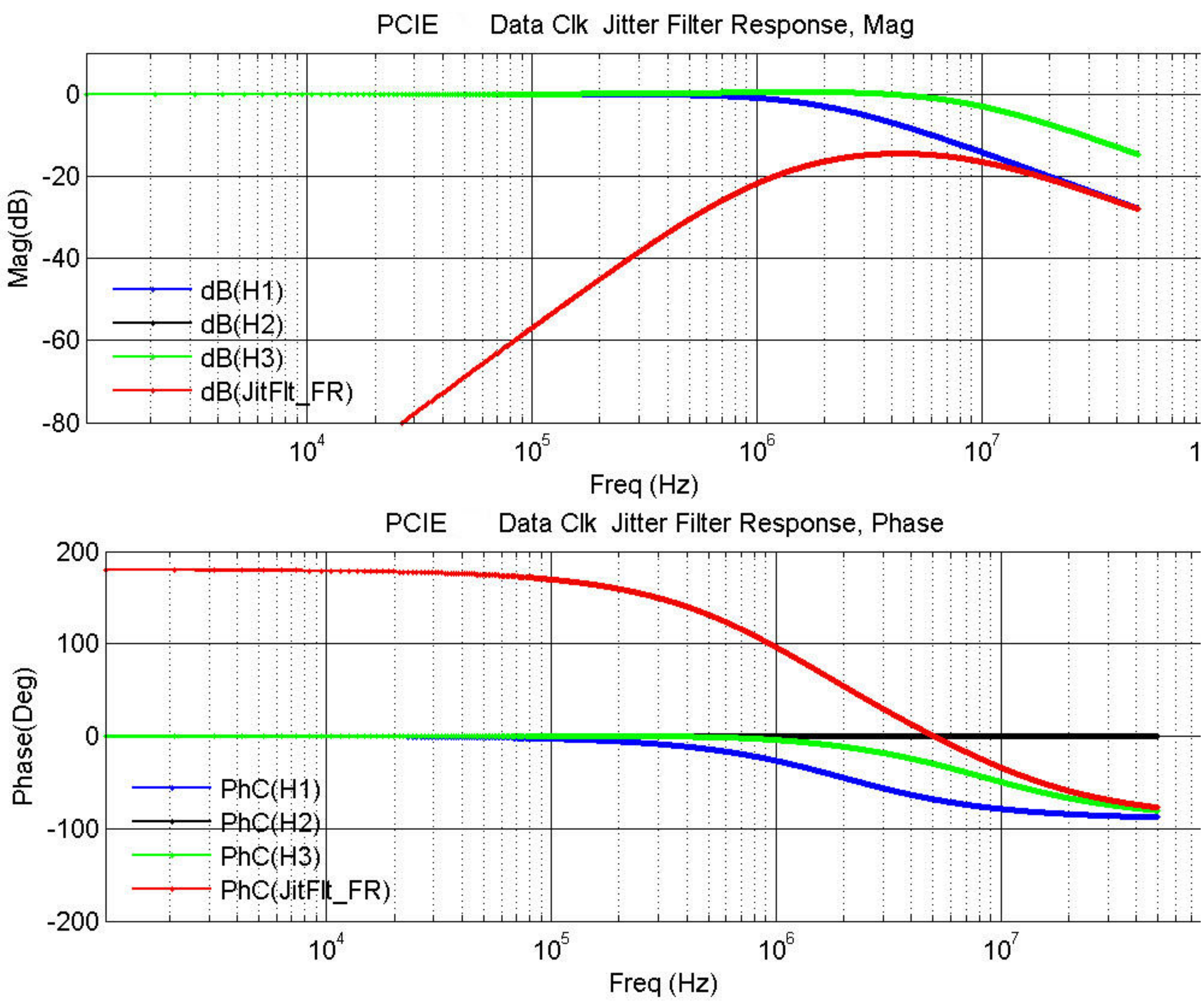


Figure 135 Reference Image for Jitter Filter Response (Data Clock) RMS Jitter Test

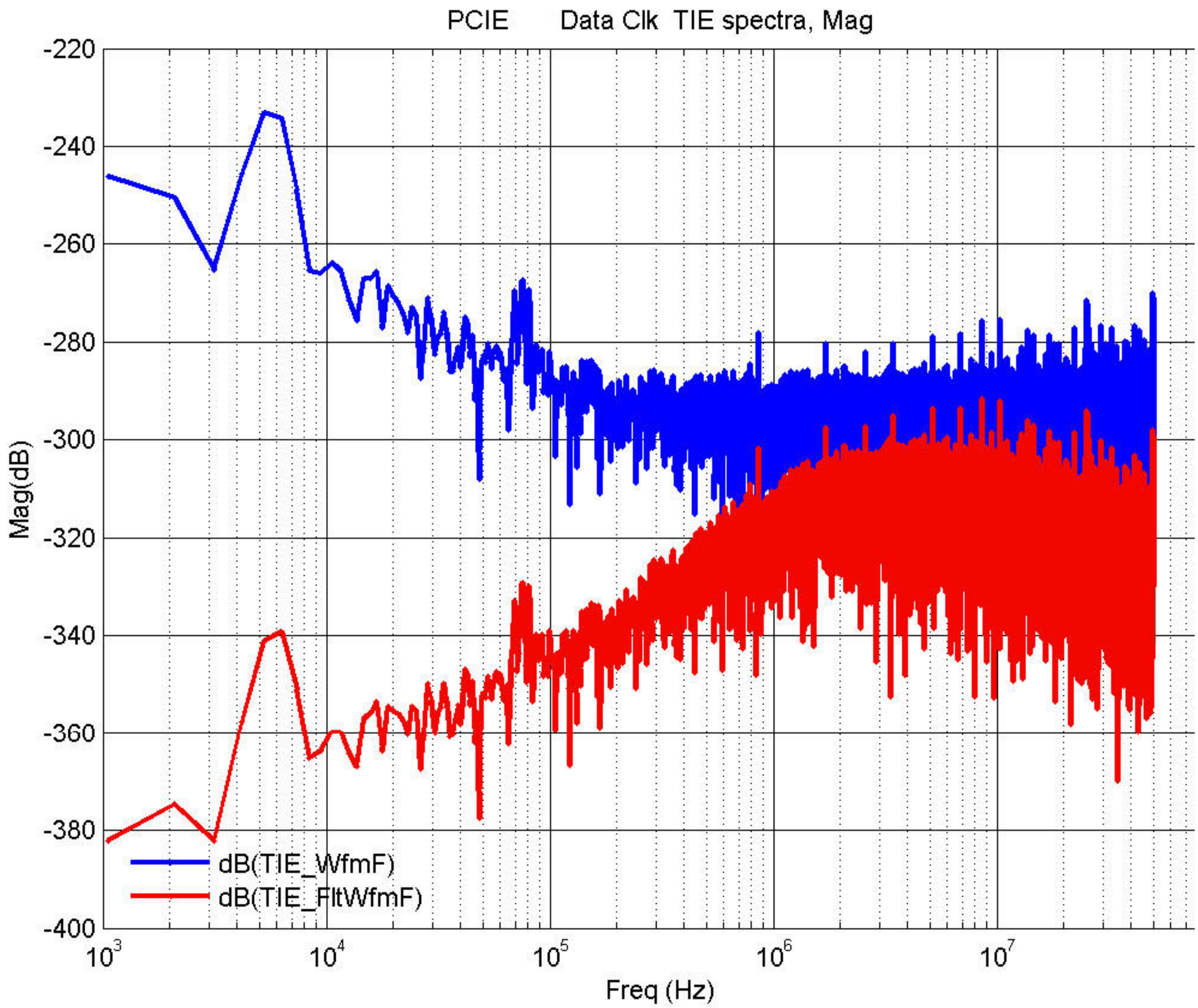


Figure 136 Reference Image for Data Clock TIE Spectra RMS Jitter Test

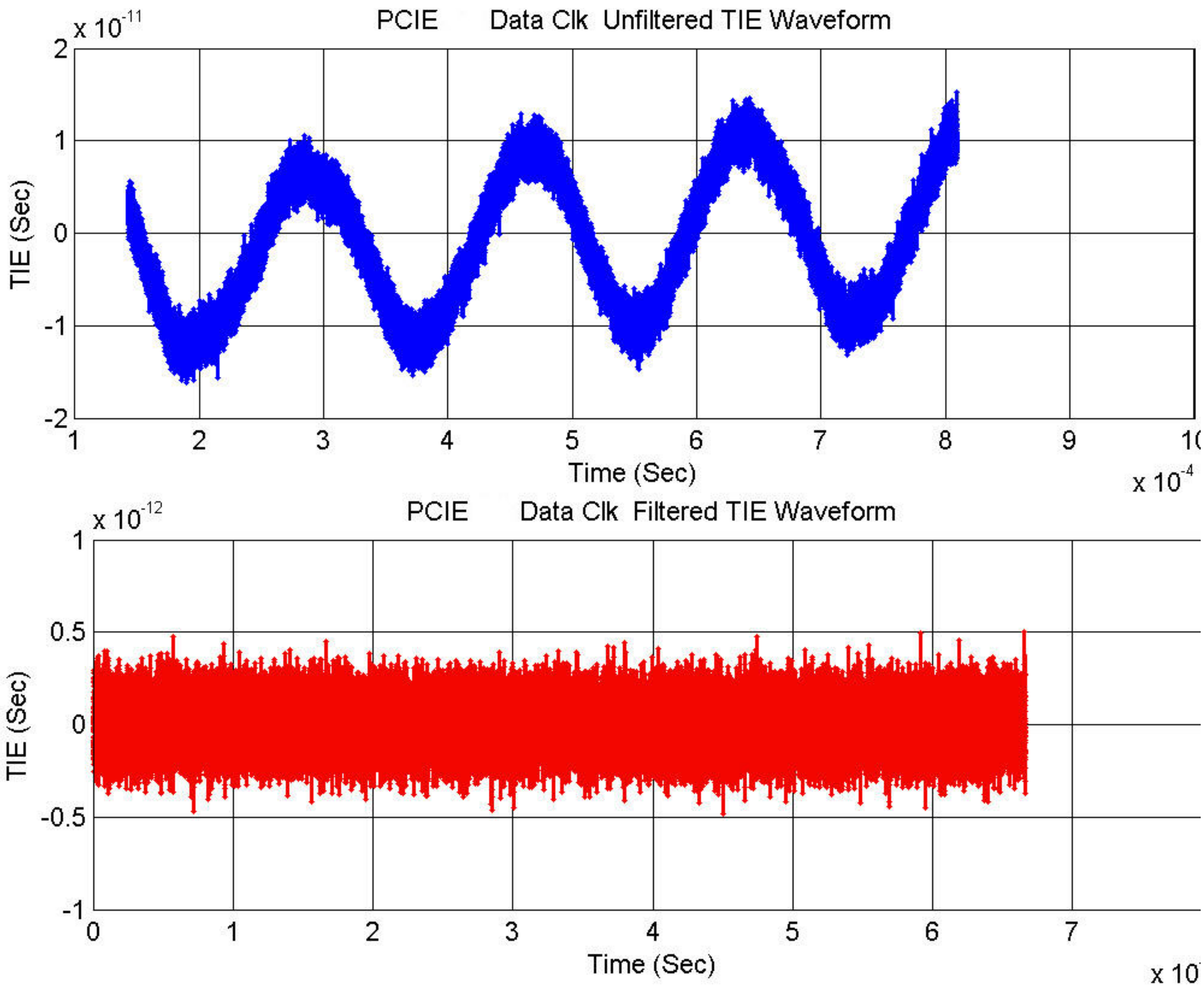


Figure 137 Reference Image for TIE Waveform RMS Jitter Test

PCI-SIG Reference Clock Jitter

This test measures PCI-SIG Reference Clock Jitter for PCIe 5.0 using Intel Clock Jitter Tool.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the PCI-SIG reference clock jitter.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Low Pass Filter**, **SSC Removal**, and **Noise Floor Deembed** option in the Clock Jitter Tool.
3. Performs compliance testing using the Clock Jitter Tool.
4. Captures the Noise Floor Signal if **Noise Floor Deembed** option is enabled.
5. Identifies overall test status.
6. Reports the overall test status, maximum phase jitter value, limits, and settings.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part VI
PCI-Express Gen5 16.0 GT/s Tests

16 Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 16.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

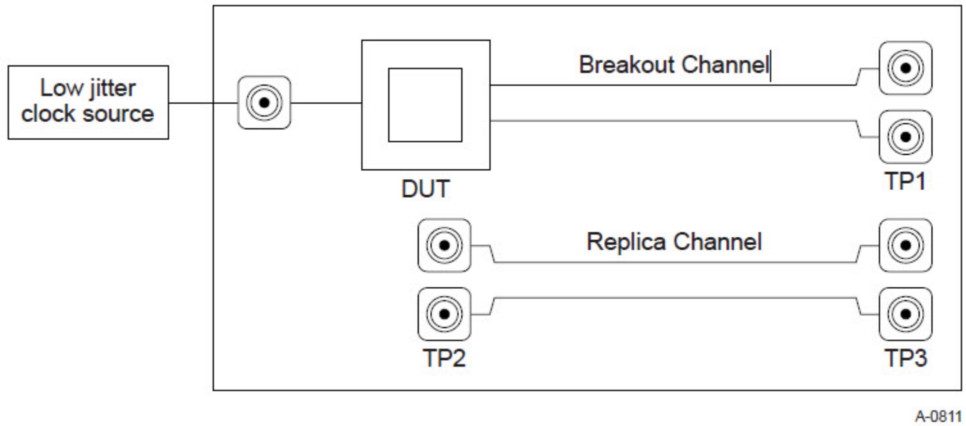


Figure 138 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 16.0 GT/s Tests > Transmitter (Tx) Tests**.

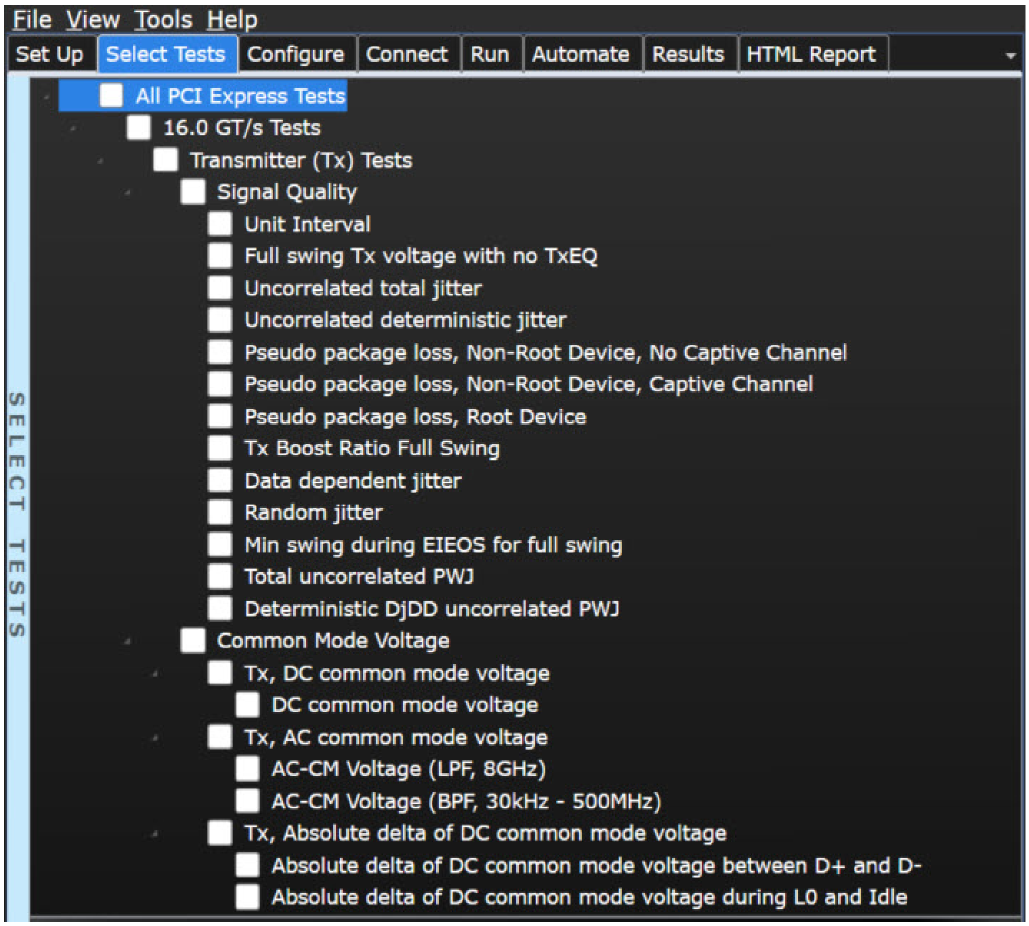


Figure 139 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

‘n’ is the index of UI in the current 2,000,000 UI clock recovery window.

‘p’ indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 132 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	62.48125 ps	62.51875 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

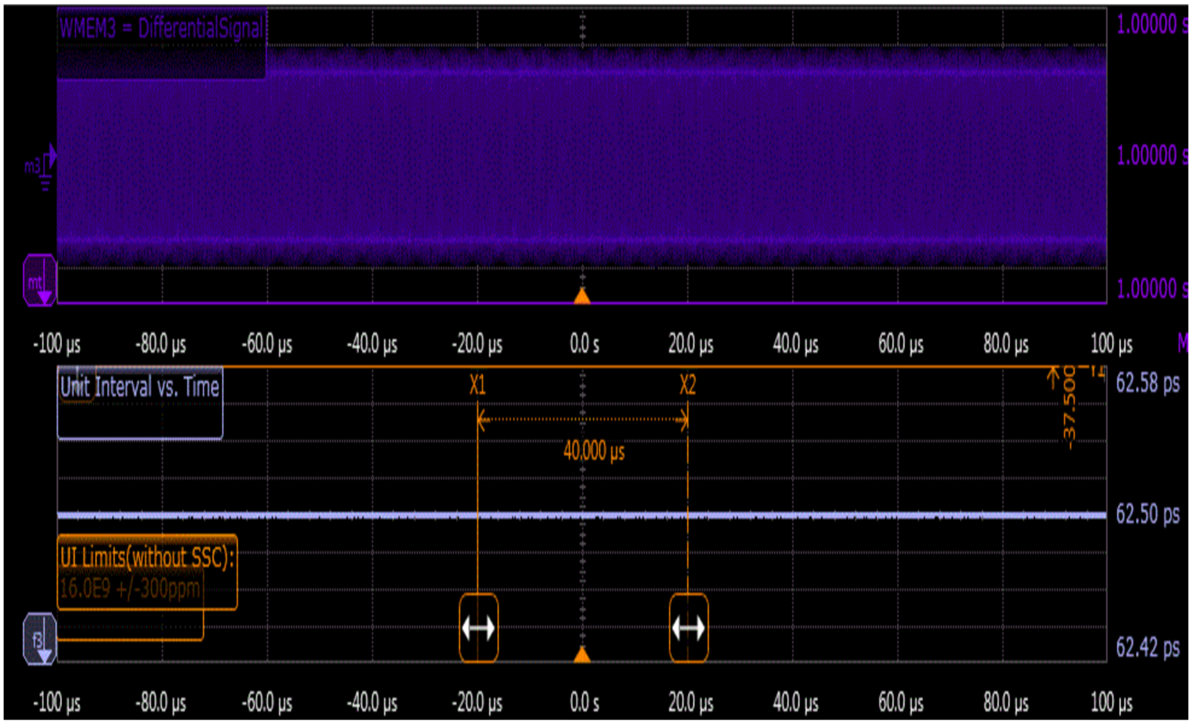


Figure 140 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 141. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP}$ is used as reference to check the compliance of the DUT.

Table 133 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$	Full swing Tx voltage with no TxEQ	800 mV	1300 mVPP

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

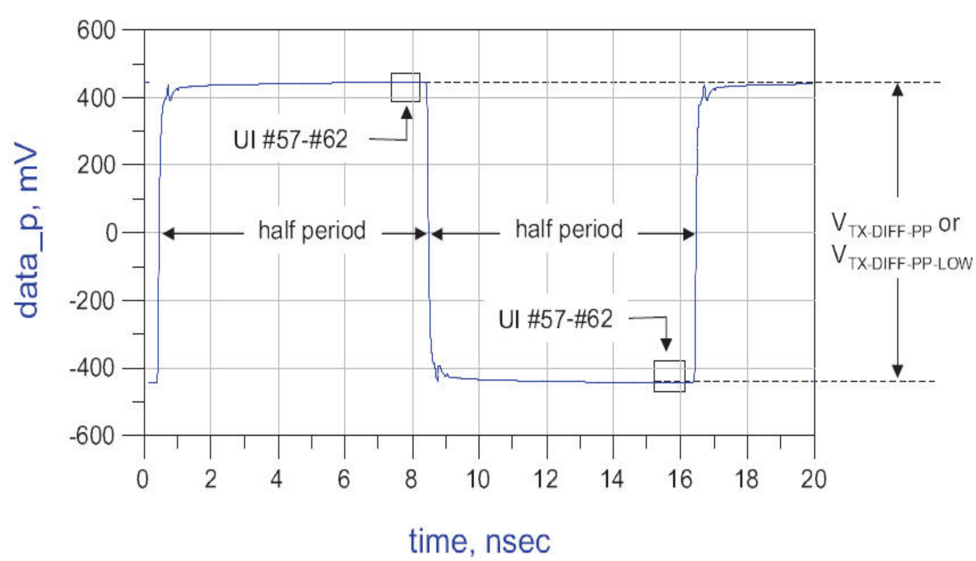


Figure 141 $V_{TX\text{-}DIFF\text{-}PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0μs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 142. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 134 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times | V_{TXD+} - V_{TXD-} |$
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

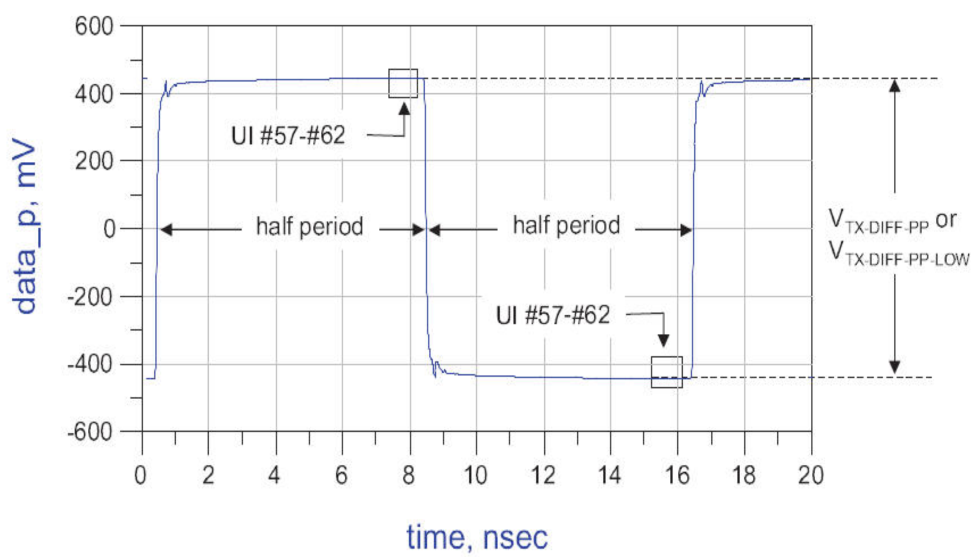


Figure 142 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14 at 16.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 135 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

VTX-EIEOS-FS and VTX-EIEOS-RS are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0 and 32.0 GT/s that ensures that these parameters are met.

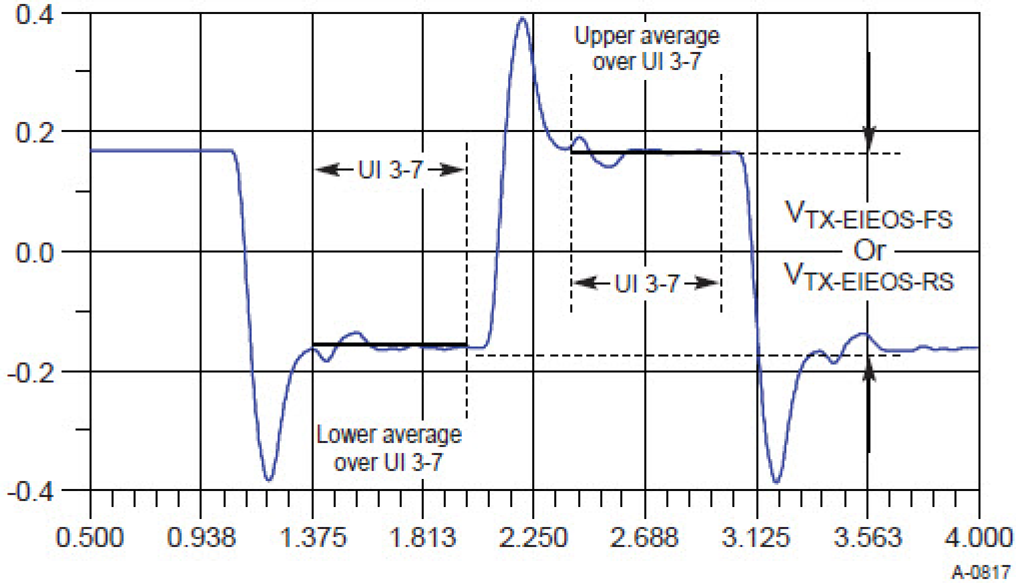


Figure 143 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Finds and updates the worst case test result values.
8. Gets the average EIEOS high voltage.
9. Gets the average EIEOS low voltage.
10. Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX\text{-}EIEOS\text{-}RS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 136 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

VTX-EIEOS-FS and VTX-EIEOS-RS are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

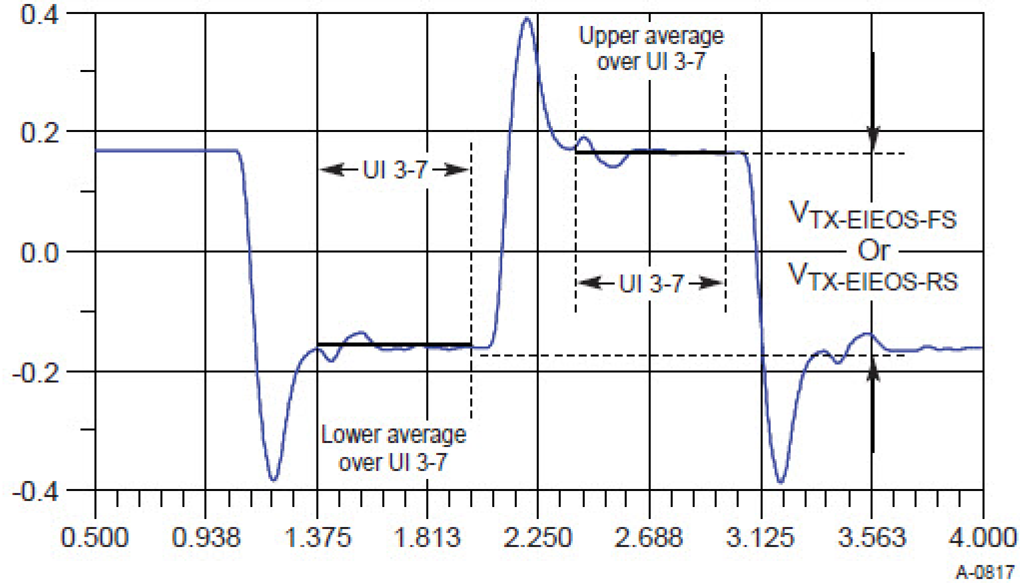


Figure 144 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Finds and updates the worst case test result values.
8. Gets the average EIEOS high voltage.
9. Gets the average EIEOS low voltage.
10. Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 137 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	11.8 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 138 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	6.25 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak uncorrelated deterministic jitter value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 139 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	12.5 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).b
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX\text{-}UPW\text{-}DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 140 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UPW\text{-}DJDD}$	Deterministic DjDD uncorrelated PWJ	5 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, T_{TX-DDJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

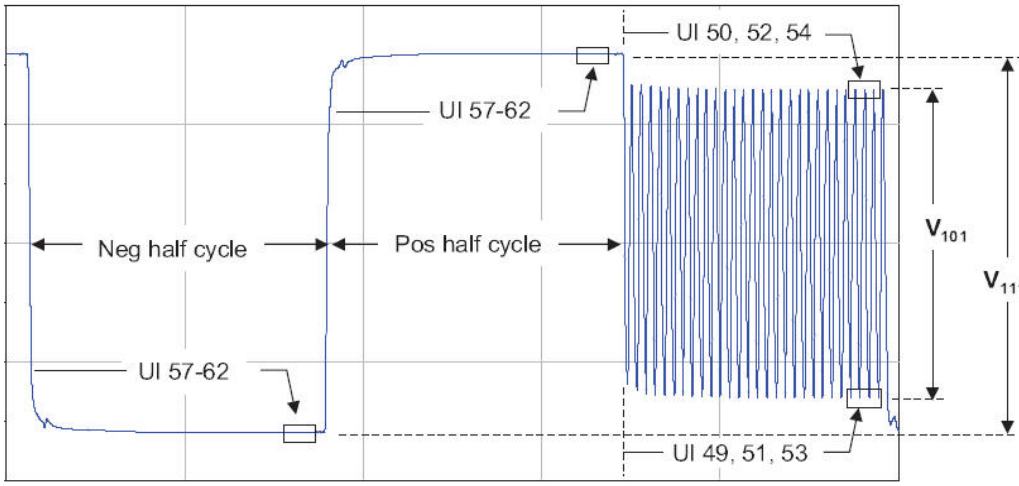
PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 141 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	5.0 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	5.0 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 145 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX\text{-}BOOST\text{-}FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

NOTE When using saved waveform option, this test will be available only when **Equalization Preset Tests** check box is selected in the **Set Up** tab.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 142 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}BOOST\text{-}FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P10.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P10 signal in *.bin format.
13 Inputs the P10 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P10.
15 Reports the measurement of Vb during preset values P10 and P4.

16 Computes the Vtx boost from the Vb and de-emphasis values.

17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 143 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 5.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 144 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	0.40 - 0.84 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 145 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

  a Enables and displays common mode measurements.

  b Loads common mode signal to waveform memory.

  c Loads and enhance dynamic range D+ signal and D- signal.

  d Enables the average common mode measurement.

  e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0 as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 8 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 146 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 147 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 8 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25$ mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 148 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX-CM-DC\ [during\ L0]} - V_{TX-CM-Idle-DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$

$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT..

Table 149 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

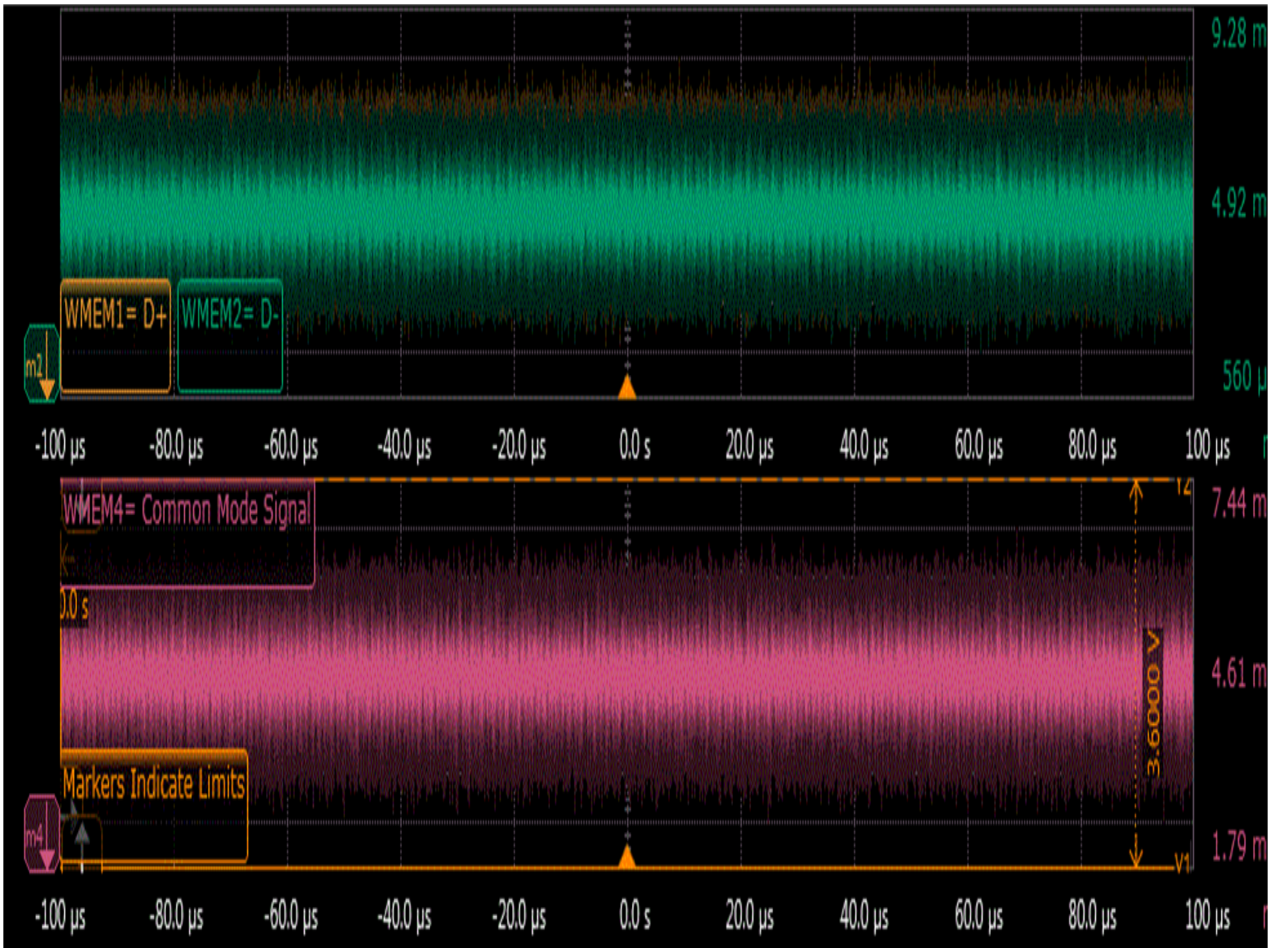


Figure 146 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 150 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 16.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 151 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 16.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 152 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 16.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 153 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a. Generates a differential plot (x_n - x_{n-1}).
   b. The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

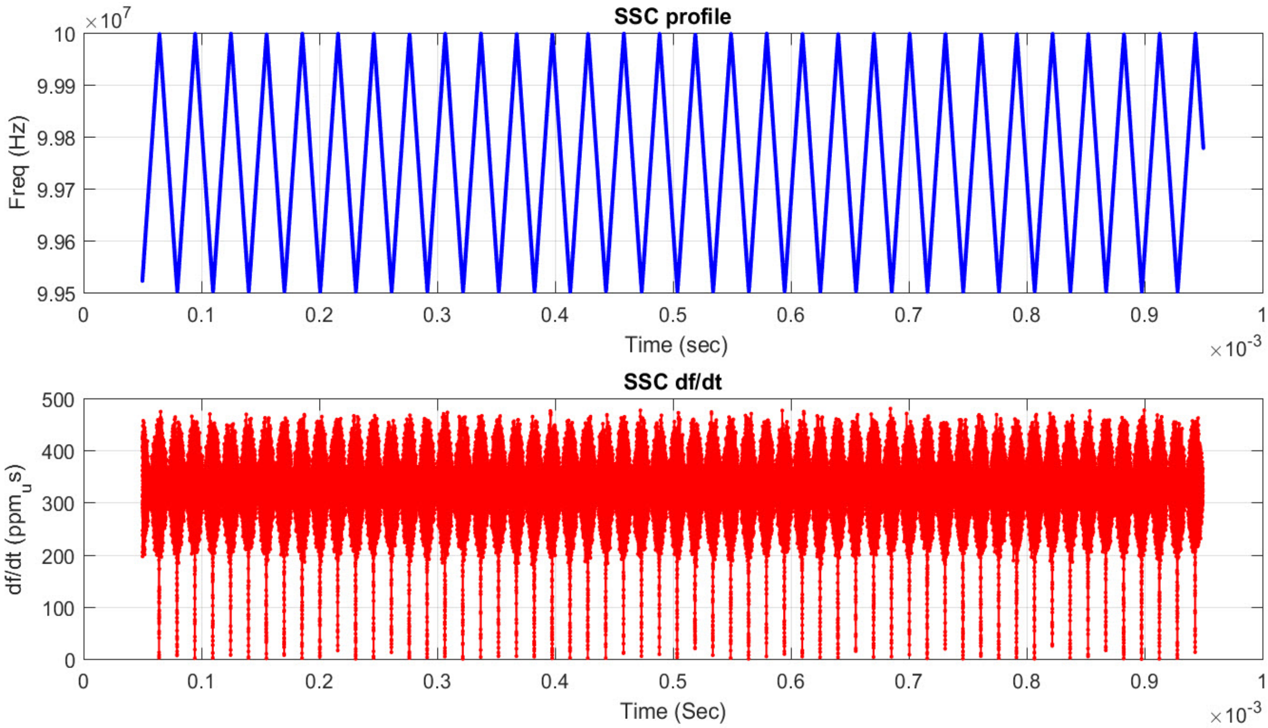


Figure 147 Maximum SSC Slew Rate

Running Equalization Presets Tests

Please refer to section: "Running Equalization Presets Tests" on page 306 in Chapter 12, "Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0".

17 CEM-EndPoint Tests, 16.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-EndPoint tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.
  Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB, and 5.0 GHz at 6.0 dB.
2 Connect cables up as follows:
  a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test).
  b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test).

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.
4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running CEM-EndPoint Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 16.0 GT/s Tests > CEM EndPoint Tests**.

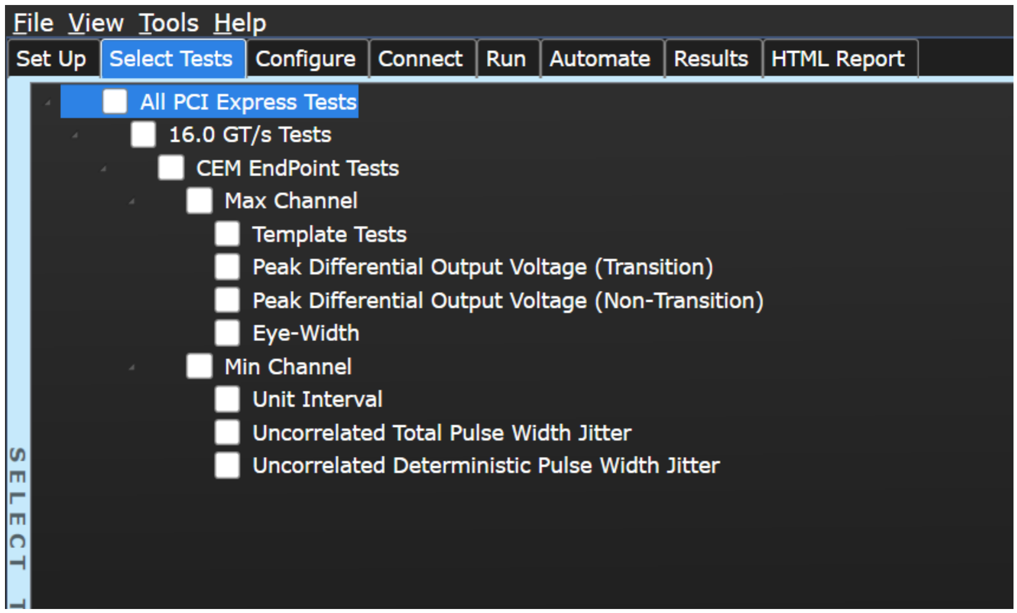


Figure 148 Selecting CEM EndPoint Tests

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.4, Table 4-15 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_{A_d}).

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.1, Figure 4-7 is used as reference to check the compliance of the DUT.

Table 154 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	23.00 mV	1300 mV	Notes 1, 2, 4
V_{TXA_d}	23.00 mV	1300 mV	Notes 1, 2, 4
T_{TXA}	24.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1. A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR-4 trace with an insertion loss of 14 dB at Nyquist, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

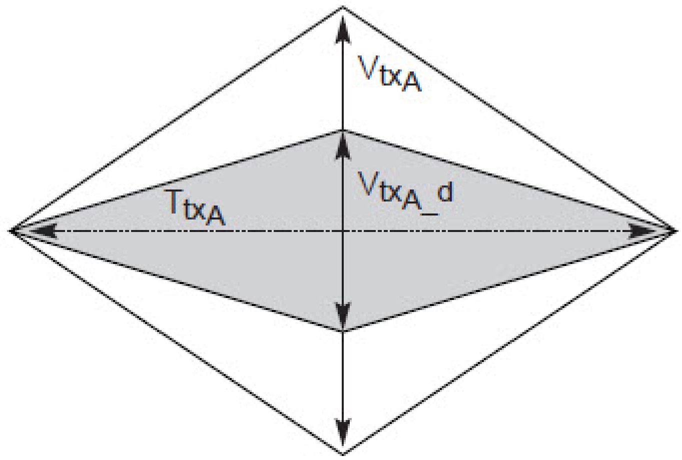


Figure 149 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs compliance testing using the SigTestWrapper.dll file.
   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

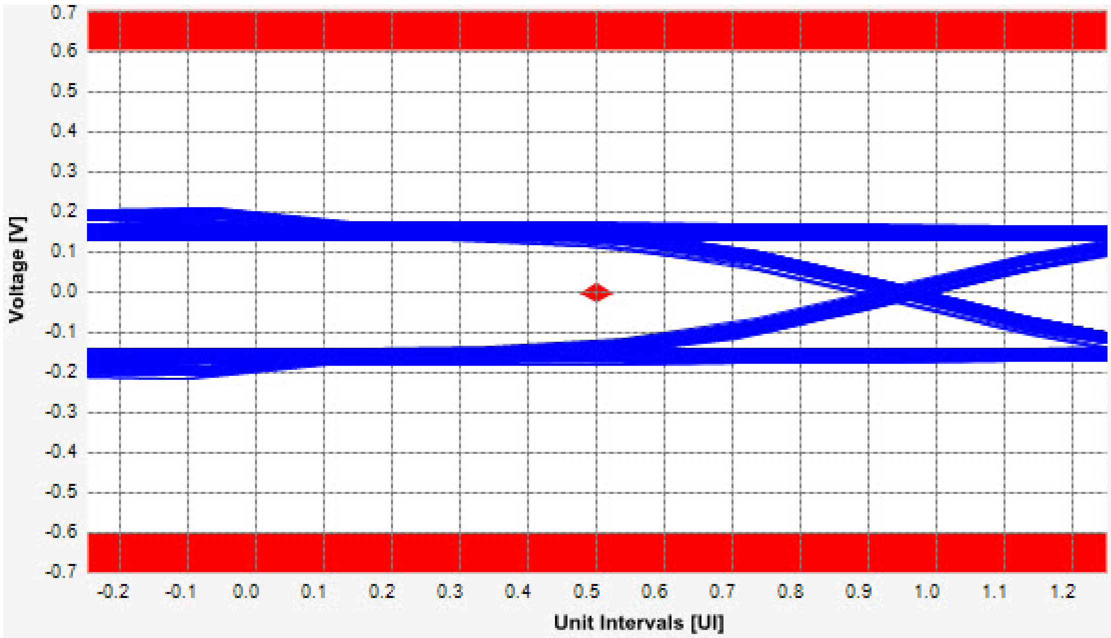


Figure 150 Reference Image for Template (Transition) Test

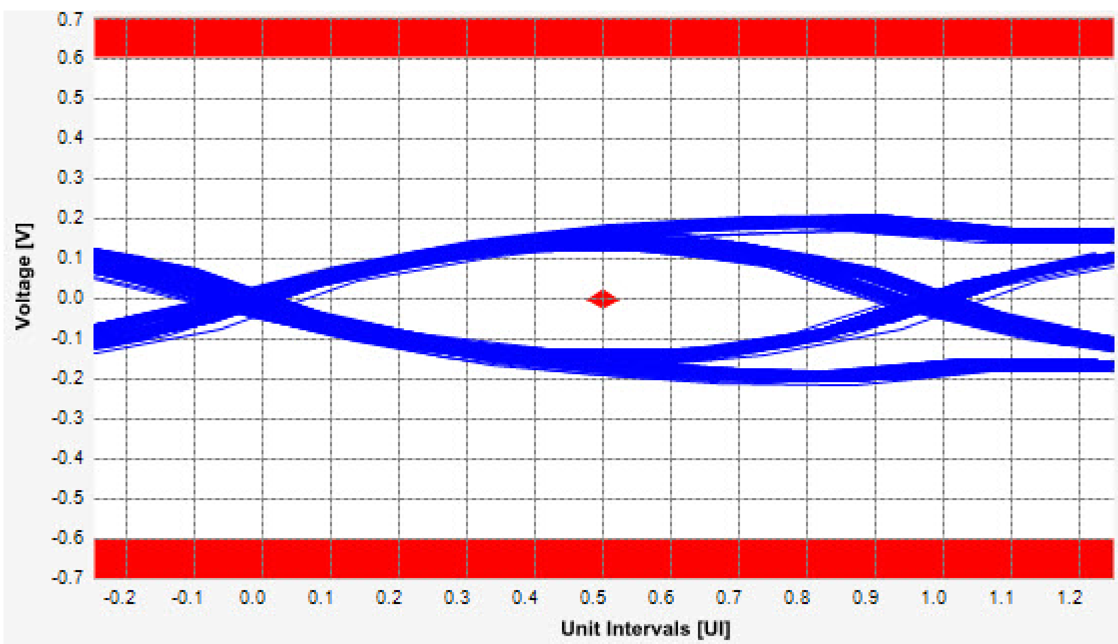


Figure 151 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.4 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.4, Table 4-15 is used as reference to check the compliance of the DUT.

Table 155 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	23.00 mV	1300 mV	Notes 1, 2, 4
V_{TXA_d}	23.00 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR-4 trace with an insertion loss of 14 dB at Nyquist, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

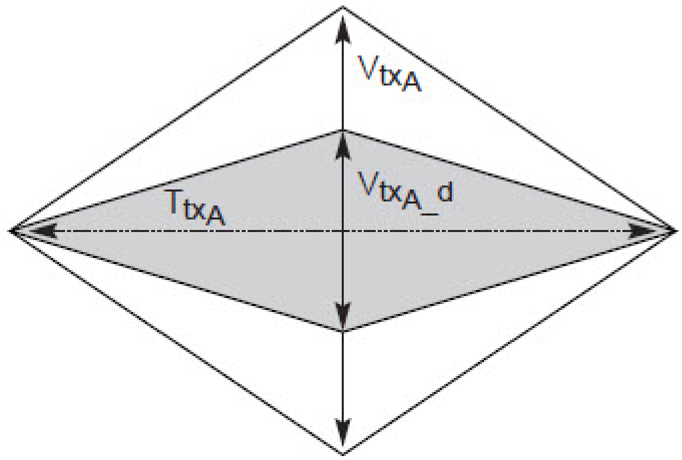


Figure 152 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 16.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

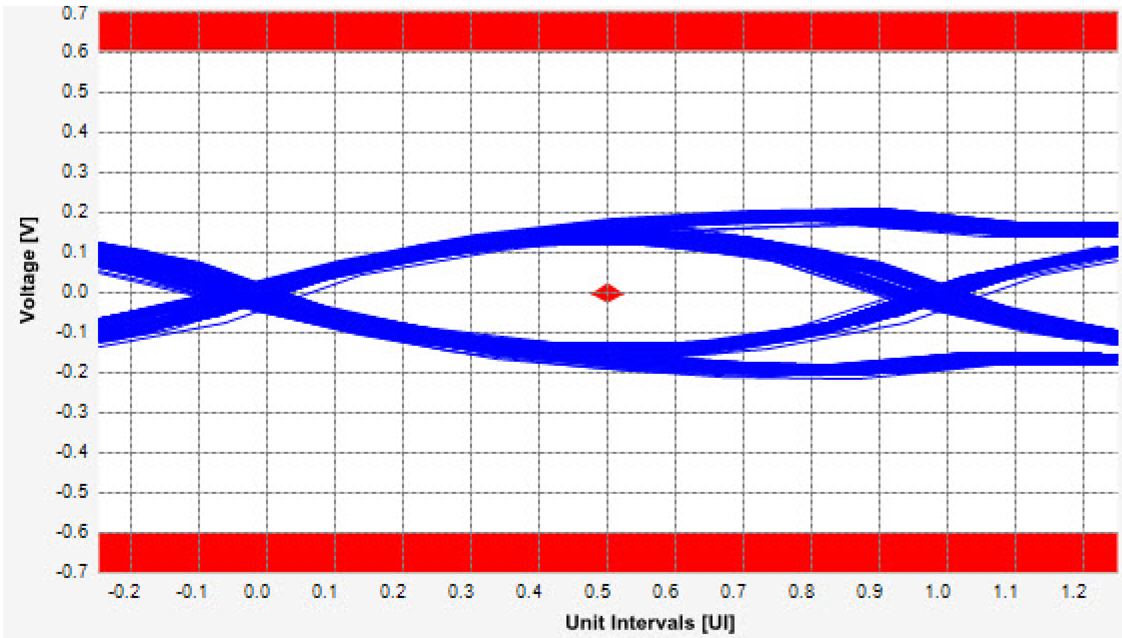


Figure 153 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.4, Table 4-15 is used as reference to check the compliance of the DUT.

Table 156 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	23.00 mV	1300 mV	Notes 1, 2, 4
V_{TXA_d}	23.00 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1. A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR-4 trace with an insertion loss of 14 dB at Nyquist, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

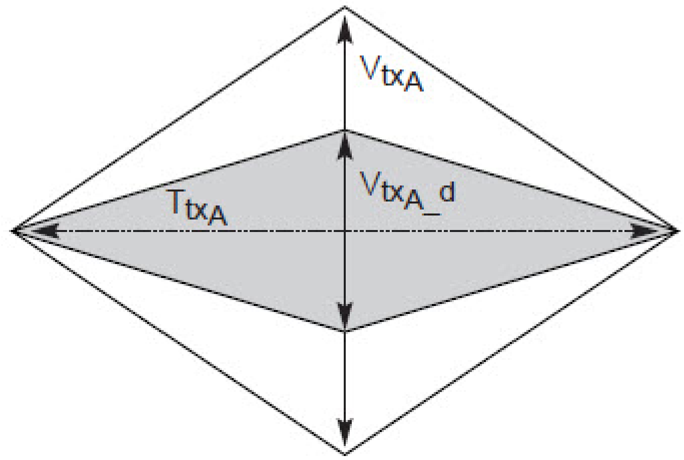


Figure 154 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 16.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

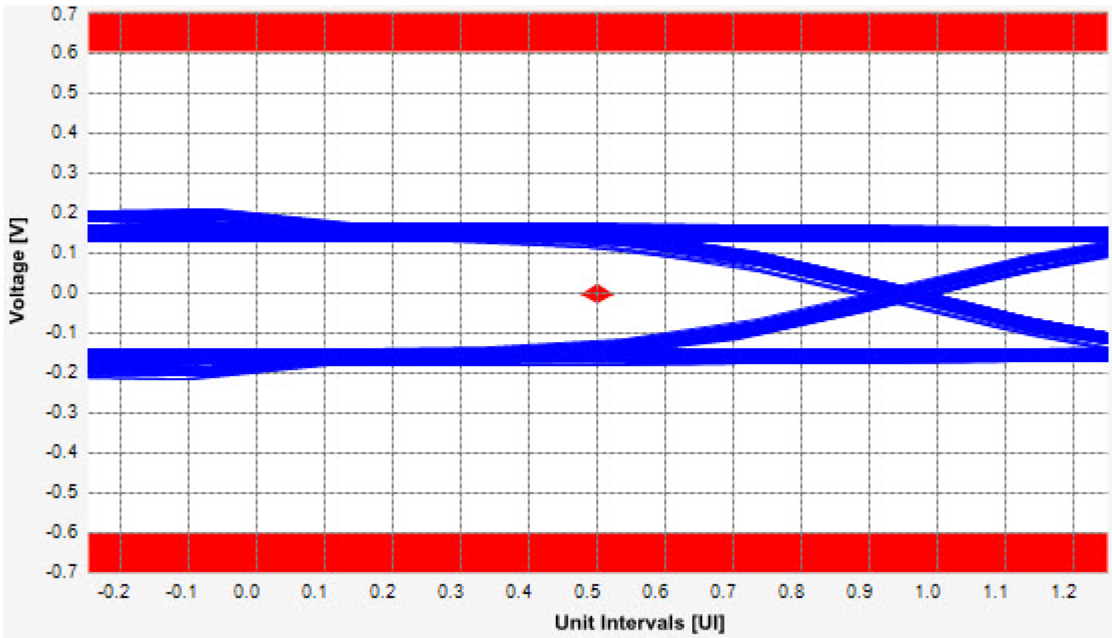


Figure 155 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.4, Table 4-15 is used as reference to check the compliance of the DUT.

Table 157 Template Test Details

Symbol	Min	Max	Comments
T_{TXA}	24.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.7 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}), V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least 2×10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω FR-4 trace with an insertion loss of 14 dB at Nyquist, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

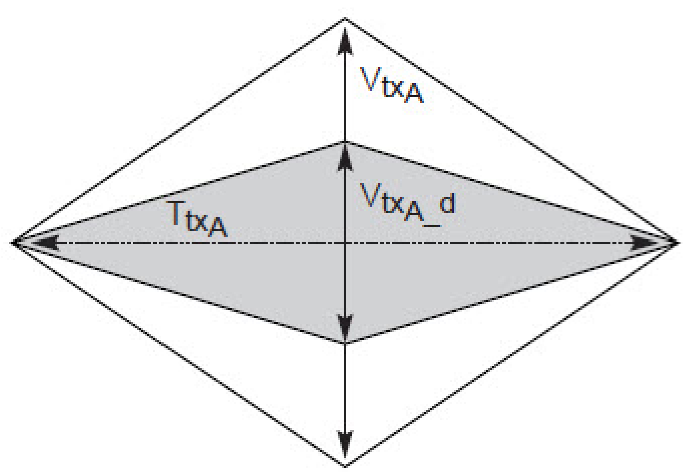


Figure 156 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> **This test requires the template test with the following specifications:**
>
> **Device: PCIE 5.0**
>
> **Data Rate: 16.0 GT/s**

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The worst case recovered TX UI is reported here. The UI range is not specified for this test point. It is provided here as informative data only.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 158 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	62.4813 ps	62.5188 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

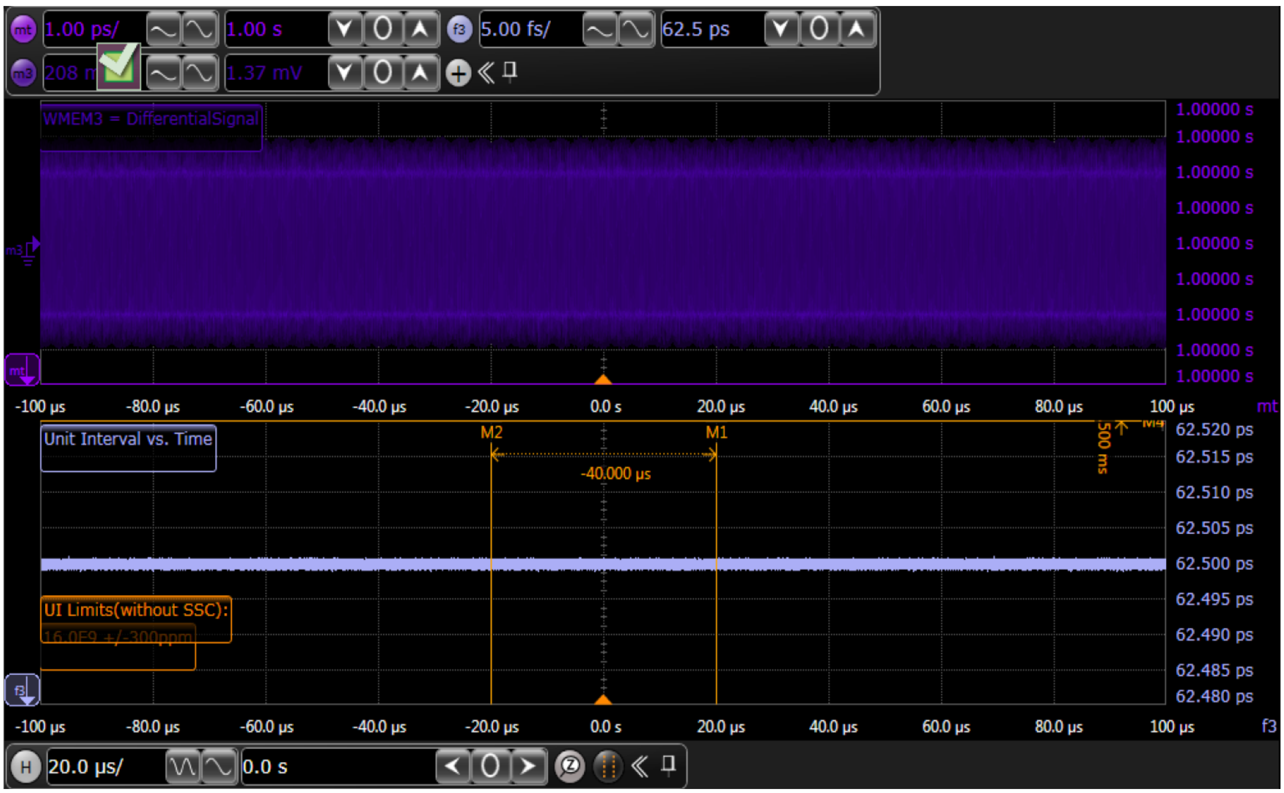


Figure 157 Reference Image for Unit Interval Test

Uncorrelated Total PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range. This test required PWJ clock pattern.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 4.8.6, Table 4-17 is used as reference to check the compliance of the DUT.

Table 159 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	12.5 ps PP at BER 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.6 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P10 + two toggles.
3 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the random jitter value.
   f Reports the uncorrelated total pulse width jitter value.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Pulse Width Jitter Test (16.0 GT/s) (Information Only)

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.6, Table 4-17 is used as reference to check the compliance of the DUT.

Table 160 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	5 ps PP at BER 10^{-12}

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.6 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

  a Gets input test waveform data from scope.

  b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

  c Performs the transmitter compliance test function using the SigTest tools.

  d Gets compliance test results from SigTest tools.

  e Reports the peak deterministic DjDD uncorrelated PWJ value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

18 CEM-RootComplex Tests, 16.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-RootComplex tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

NOTE

When SMP probing and two channels are used, channel-to-channel de-skew is required (see "Channel-to-Channel De-skew" on page 1223).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running CEM-RootComplex Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 16.0 GT/s Tests > CEM RootComplex Tests**.

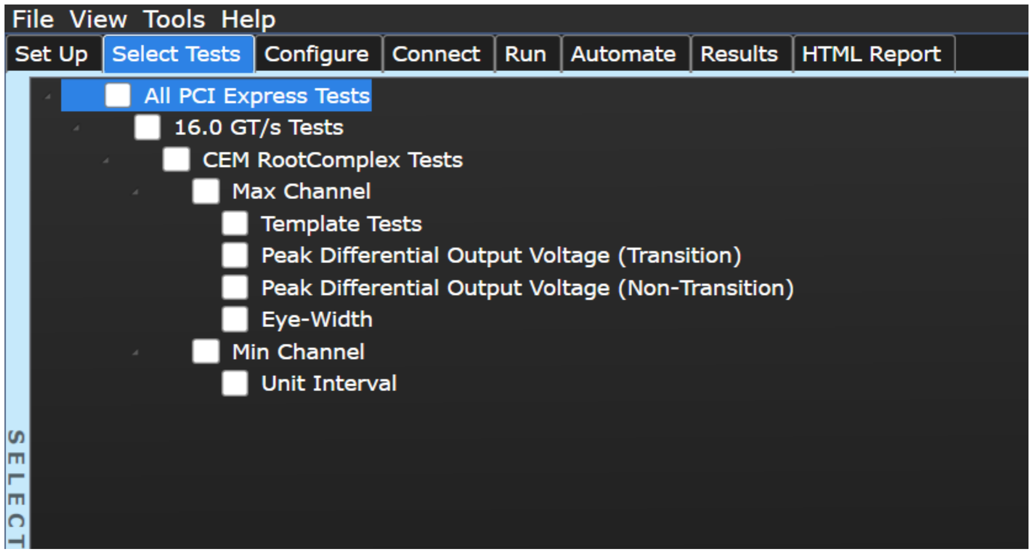


Figure 158 Selecting System Board (Tx) Tests

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.16 as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.13, Figure 4-9 is used as reference to check the compliance of the DUT.

Table 161 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	19 mV	1300 mV	Notes 1, 2, 4
V_{TXS_d}	19 mV	1300 mV	Notes 1, 2, 4
T_{TXS}	21.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

- All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.
- Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of $10^{-12.}$ The sample size for this measurement is required to be at least 2 x 10^6 UI.
- T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.
- The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ω trace, at 8.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

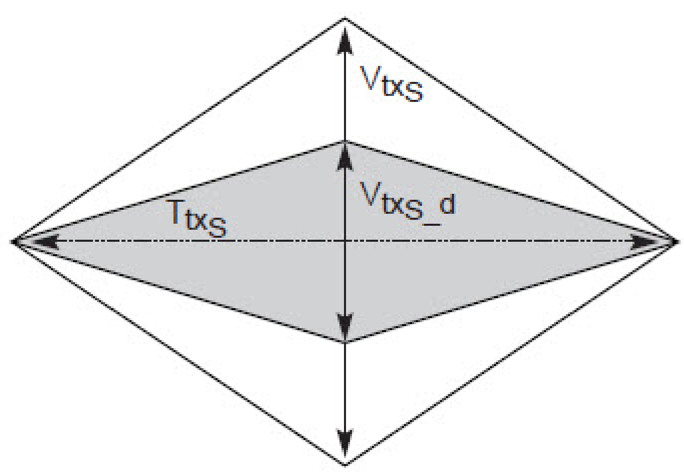


Figure 159 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

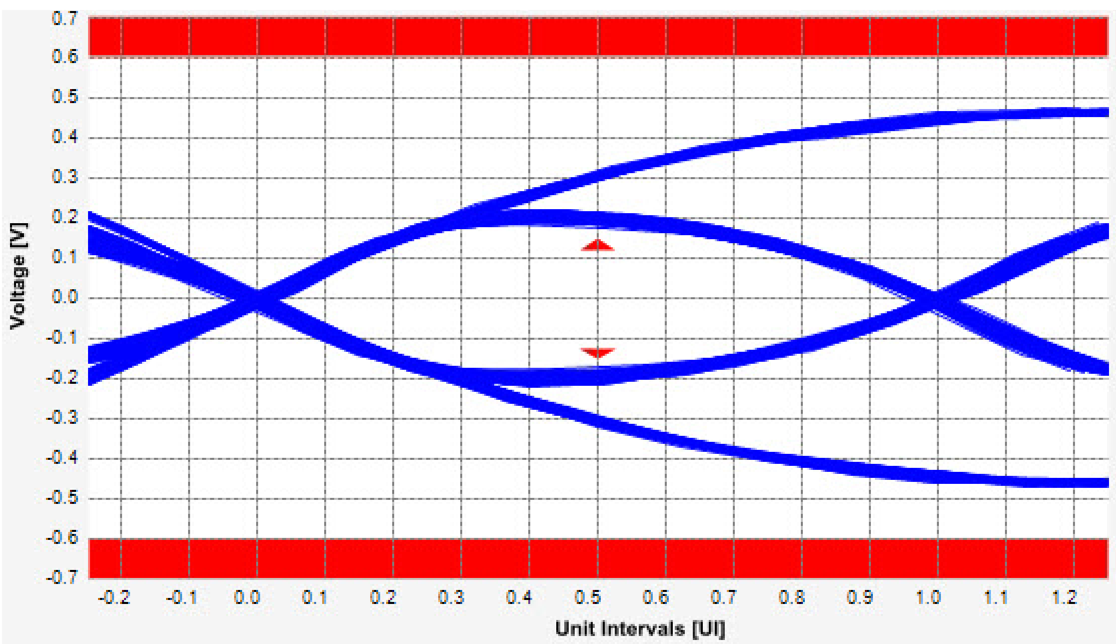


Figure 160 Reference Image for Template (Transition) Test

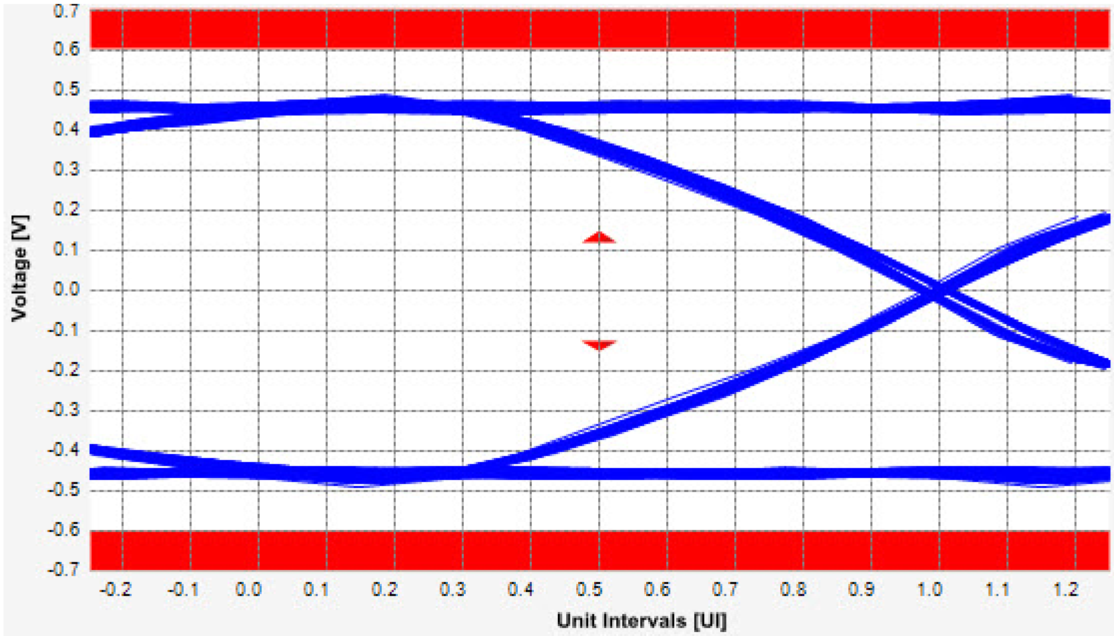


Figure 161 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements specified in section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.16, Table 4-29 is used as reference to check the compliance of the DUT.

Table 162 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	19 mV	1200 mV	Notes 1, 2, 4
V_{TXS_d}	19 mV	1200 mV	Notes 1, 2, 4
T_{TXS}	21.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of $10^{-12.}$ The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ω trace, at 8.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

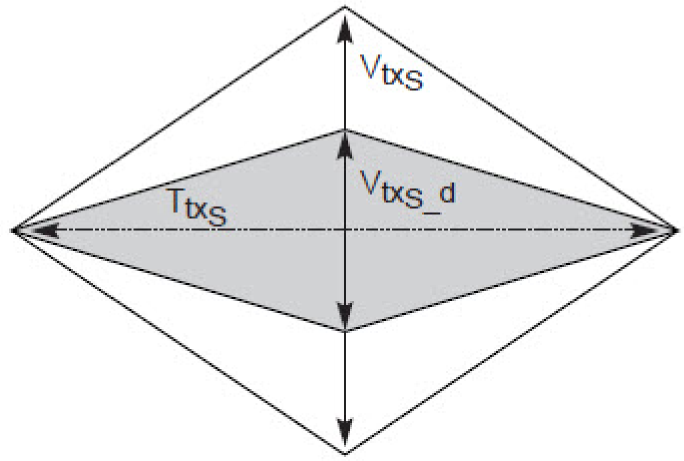


Figure 162 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
>
> Data Rate: 16.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

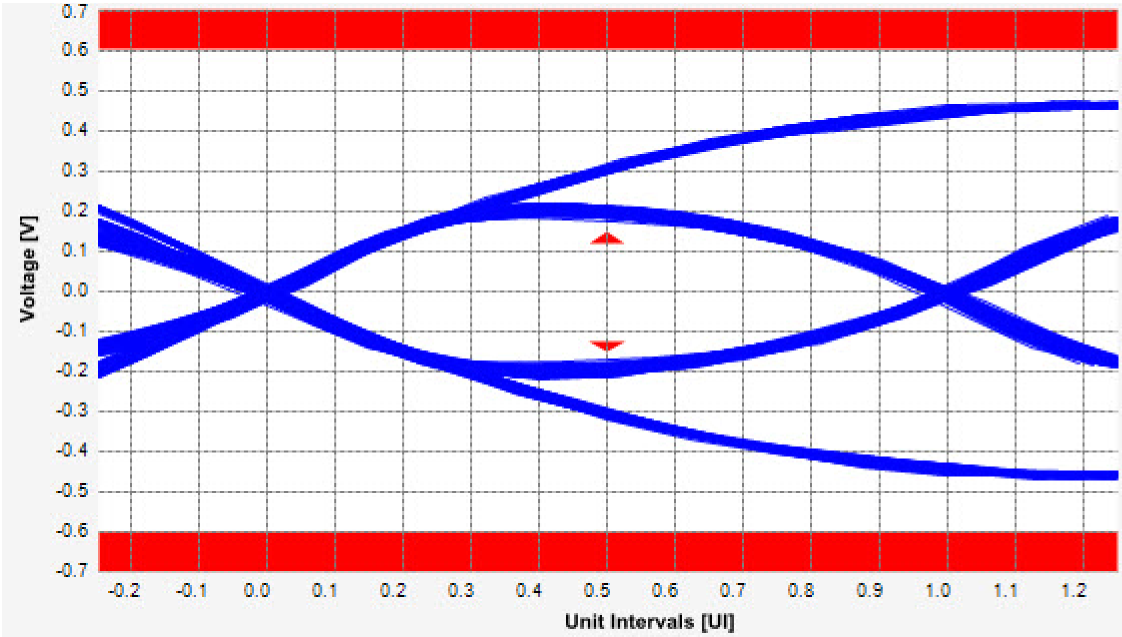


Figure 163 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye** requirements specified in section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.16, Table 4-29 is used as reference to check the compliance of the DUT.

Table 163 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	19 mV	1200 mV	Notes 1, 2, 4
V_{TXS_d}	19 mV	1200 mV	Notes 1, 2, 4
T_{TXS}	21.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of $10^{-12.}$ The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ω trace, at 8.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

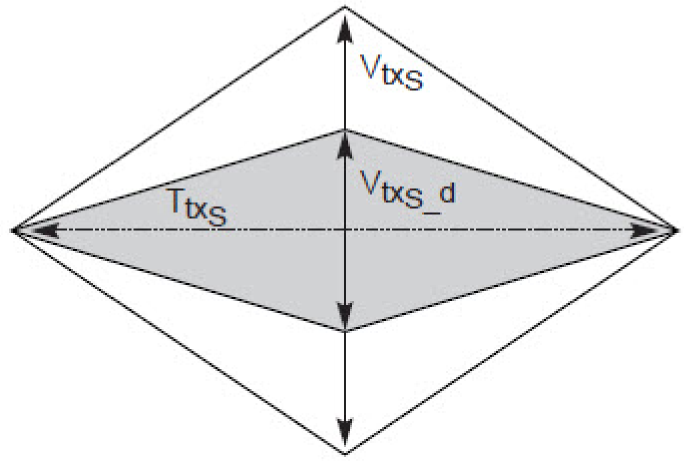


Figure 164 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> This test requires the template test with the following specifications:
>
> Device: PCIE 5.0
>
> Data Rate: 16.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the Online help.

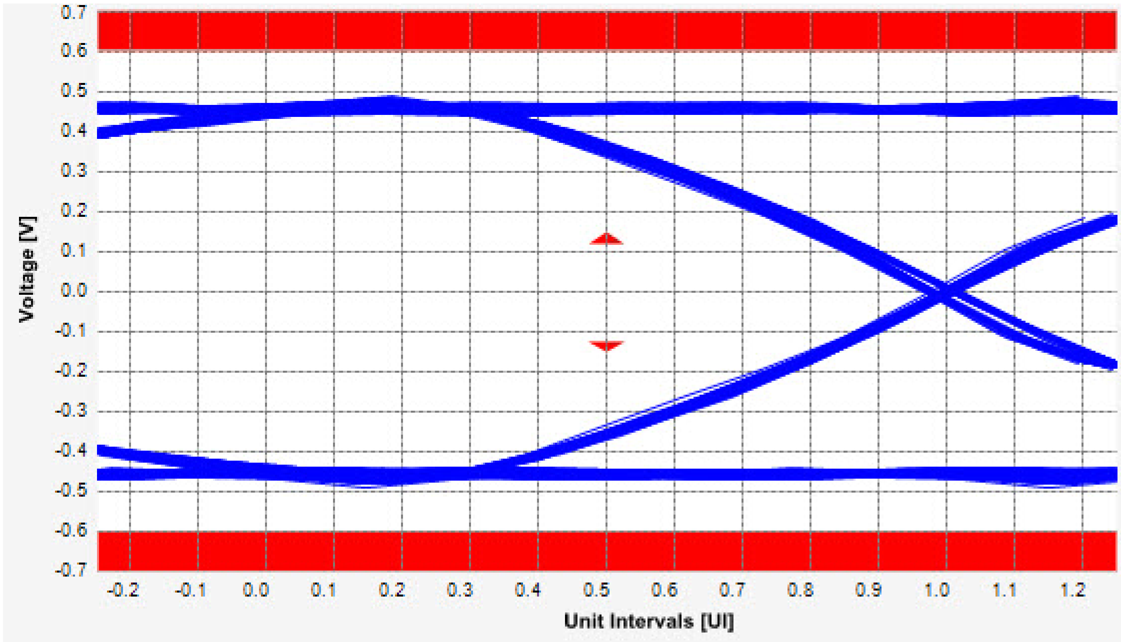


Figure 165 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

System Board must meet the **System Board Transmitter Path Compliance Eye** Requirements specified section 4.8.16 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.16, Table 4-29 is used as reference to check the compliance of the DUT.

Table 164 Template Test Details

Symbol	Min	Max	Comments
T_{TXS}	21.75 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test.

2 Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}), V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of $10^{-12.}$ The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The sample size for this measurement is required to be at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5 dB of 85 Ω trace, at 8.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 16.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

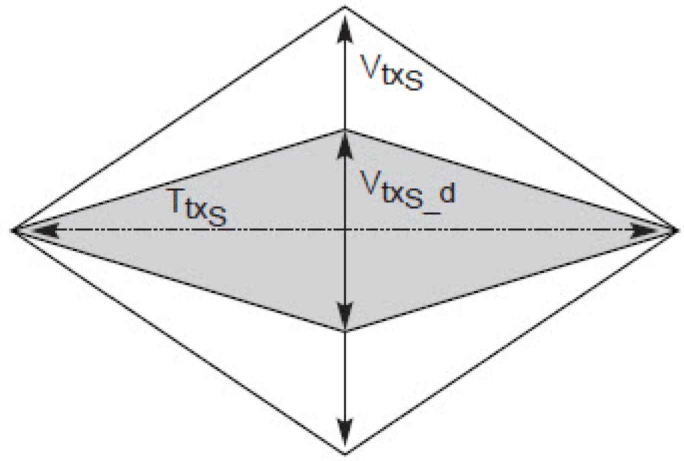


Figure 166 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** This test requires the template test with the following specifications:
> Device: PCIE 5.0
>
> Data Rate: 16.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window is as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the pth 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 165 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	62.4813 ps	62.5188 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Fits and displays all sample data on screen.
3. Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a. Selects **Unit Interval** as data measurement analysis unit.
   b. Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4. Indicates the upper and lower limit of the measured data using markers.
5. Measures the minimum, mean, and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

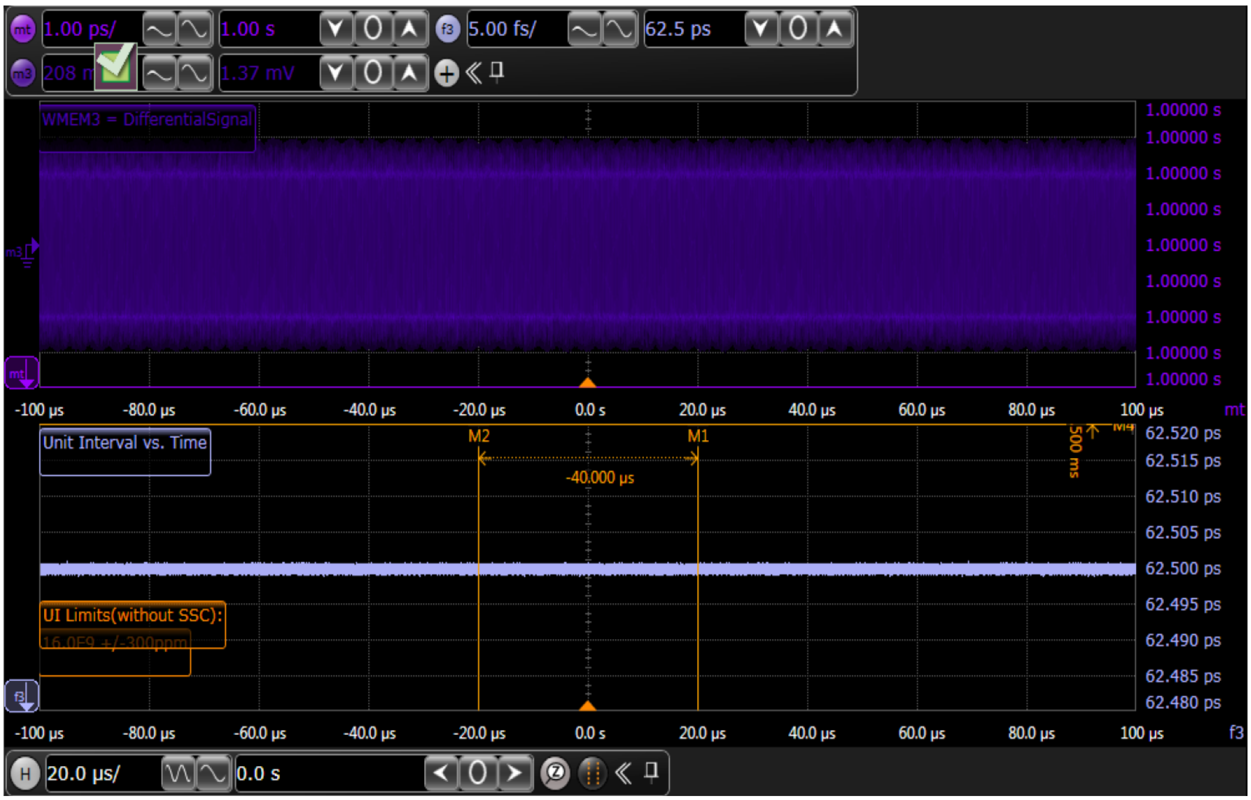


Figure 167 Reference Image for Unit Interval Test

19 Reference Clock Tests, 16.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe 5.0 Reference Clock tests at 16.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

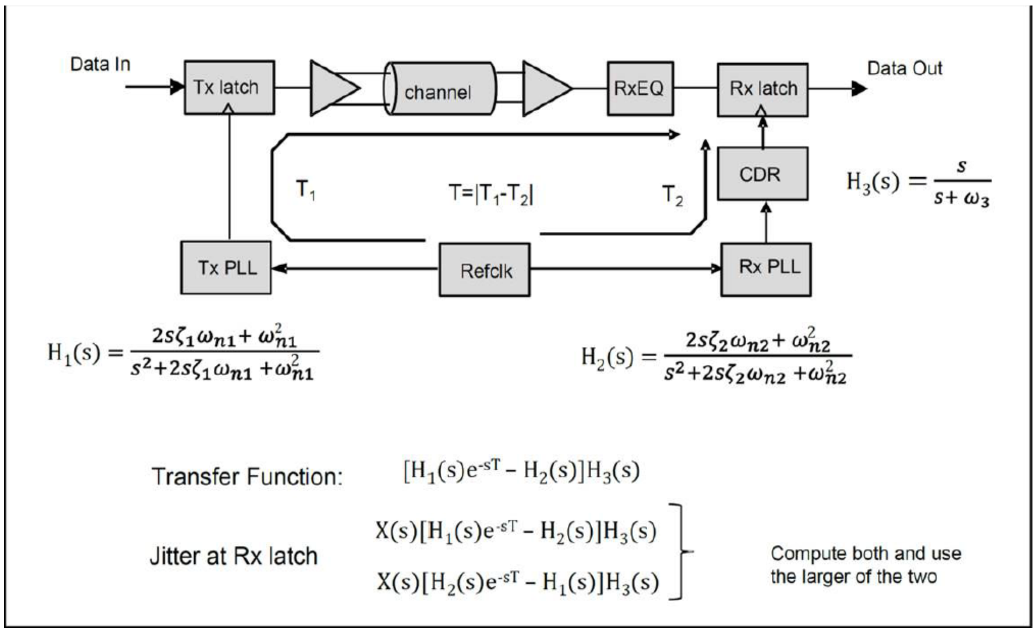
NOTE **It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.**

Reference Clock Architectures

For 16.0 GT/s, PCI-E 5.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(min) = 2.0$ MHz	ω_{n1}= 0.448 Mrad/s $\zeta_1 = 14$	ω_{n1}= 6.02 Mrad/s $\zeta_1 = 0.73$	$BW_{PLL}(min) = 2.0$ MHz	ω_{n2}= 0.448 Mrad/s $\zeta_2 = 14$	ω_{n2}= 4.62 Mrad/s $\zeta_2 = 1.15$
$BW_{PLL}(max) = 4.0$ MHz	ω_{n1}= 0.896 Mrad/s $\zeta_1 = 14$	ω_{n1}= 12.04 Mrad/s $\zeta_1 = 0.73$	$BW_{PLL}(max) = 5.0$ MHz	ω_{n2}= 1.12Mrad/s $\zeta_2 = 14$	ω_{n2}= 11.53 Mrad/s $\zeta_2 = 1.15$
$BW_{CDR}(min) = 10$ MHz, 1st order	64 combinations				8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

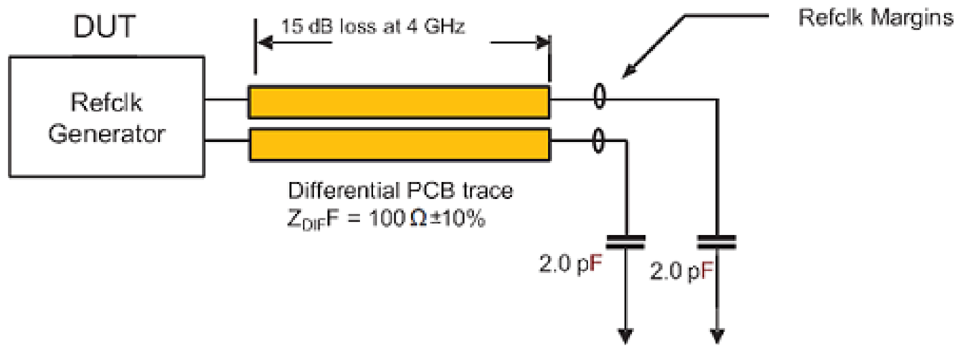


Figure 168 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 16.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

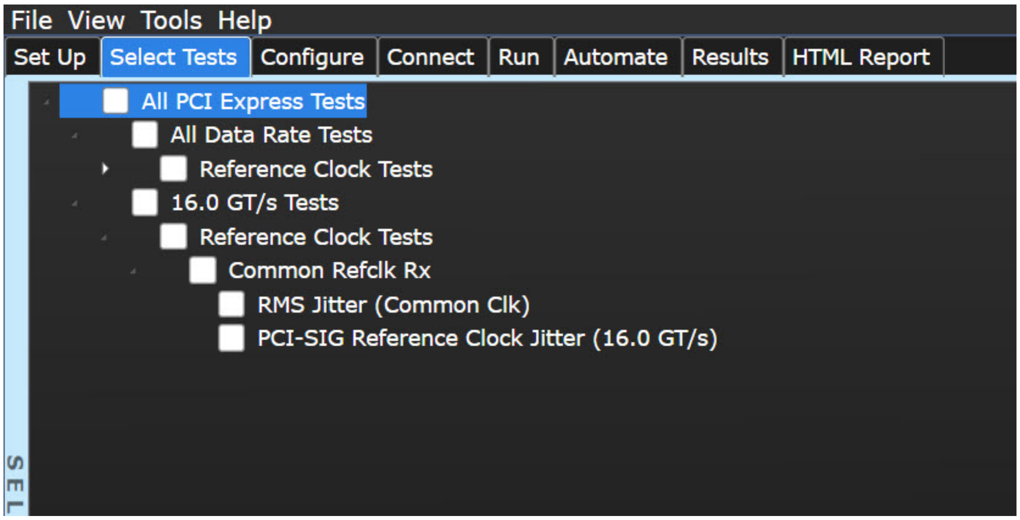


Figure 169 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 166 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.5 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.
10. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
    - *a* Converts time domain TIE data to frequency domain.
    - *b* Applies the PLL filter using parameters for common clocked architecture.
    - *c* Converts back the frequency domain TIE data to time domains.
    - *d* Computes the filtered peak-peak jitters and RMS jitter.
11. Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

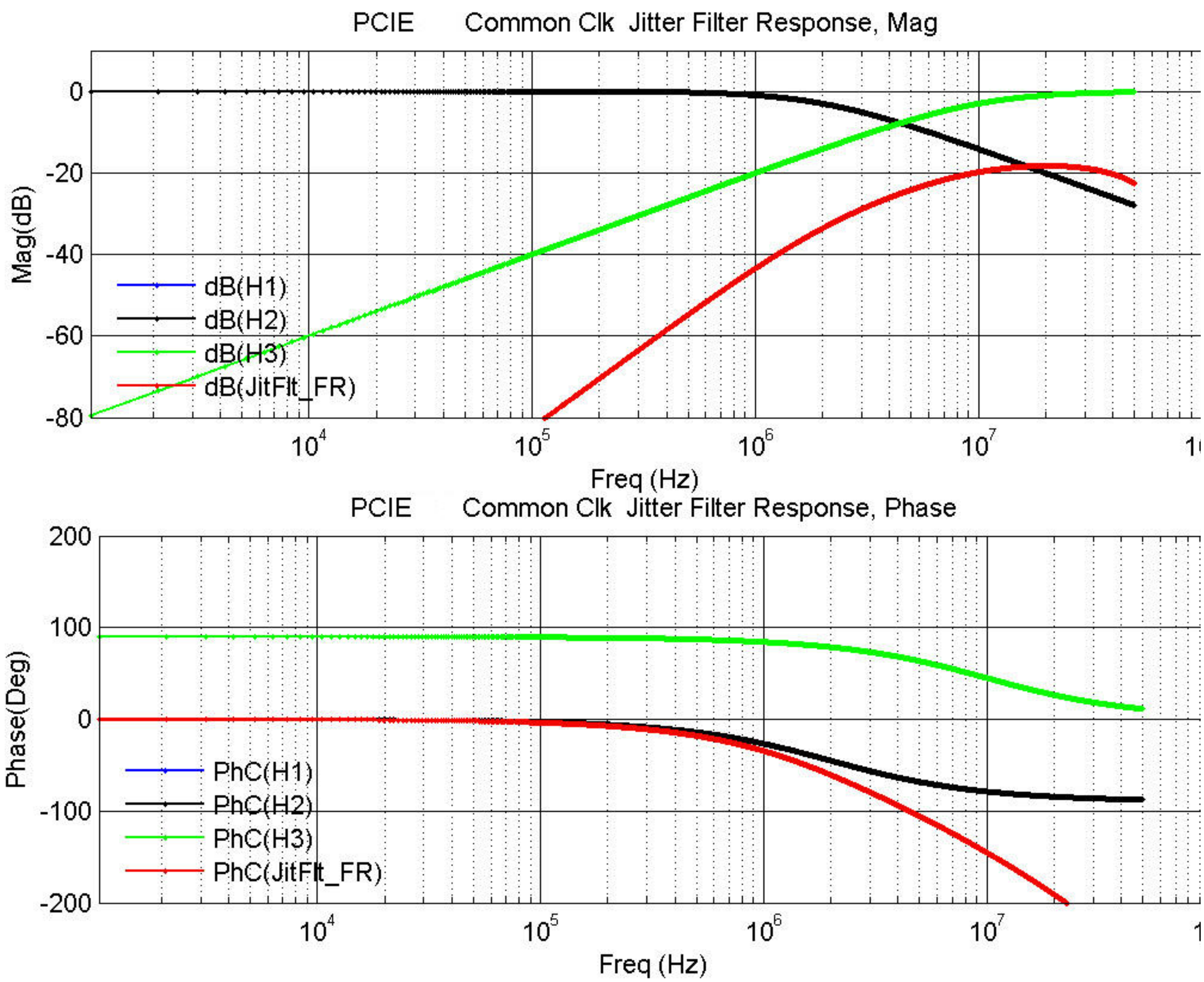


Figure 170 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

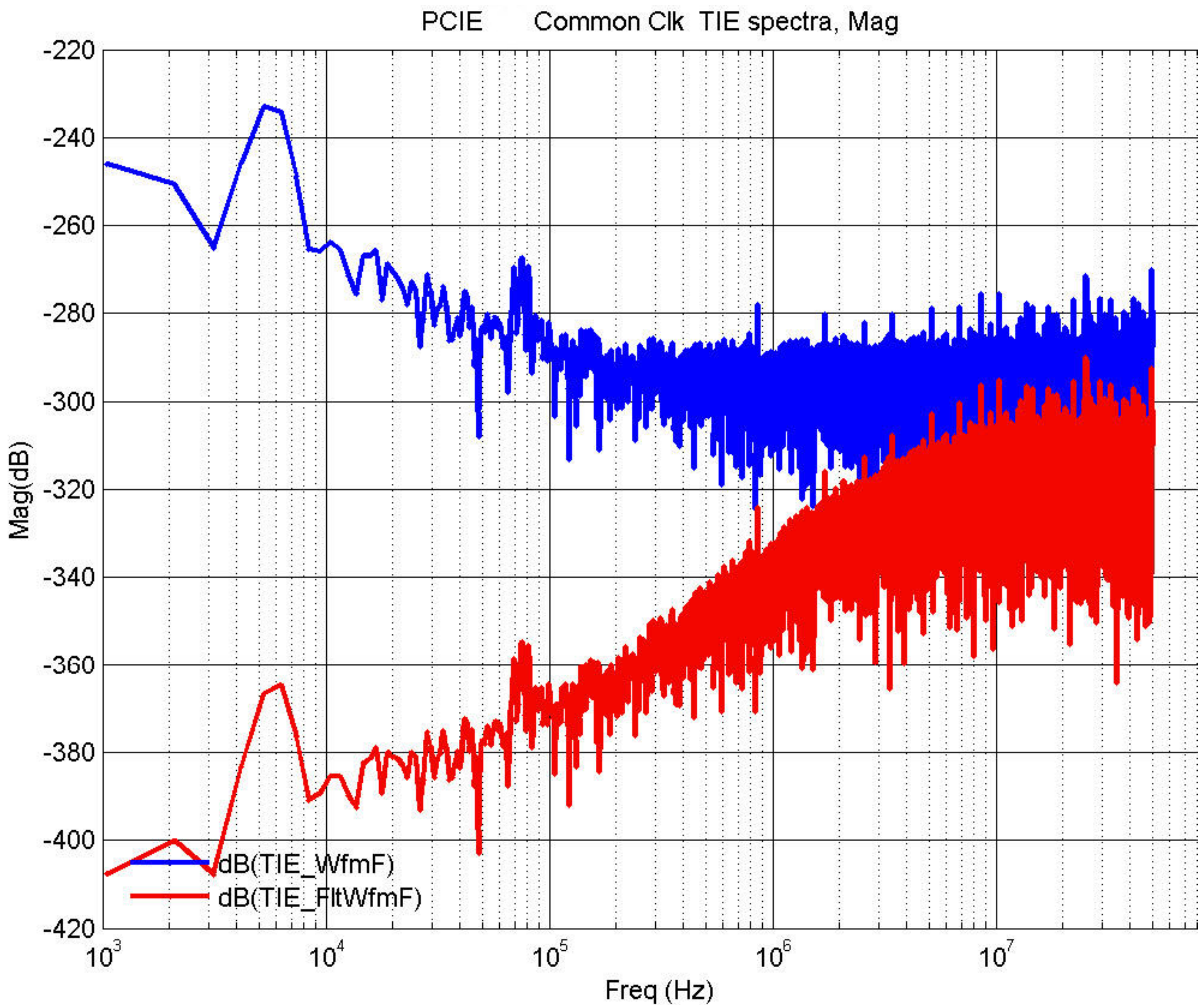


Figure 171 Reference Image for Common Clock TIE Spectra RMS Jitter Test

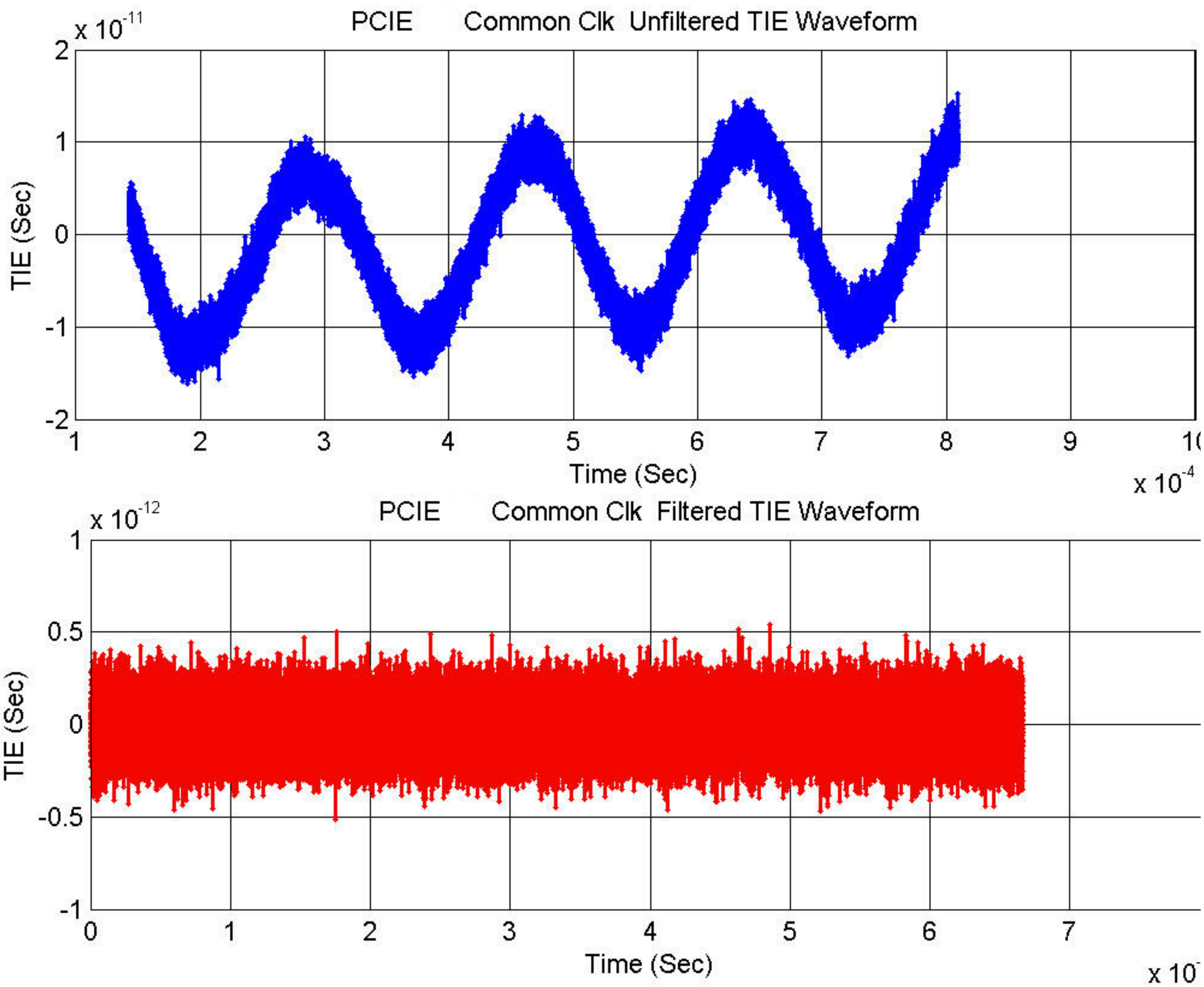


Figure 172 Reference Image for TIE Waveform RMS Jitter Test

PCI-SIG Reference Clock Jitter

This test measures PCI-SIG Reference Clock Jitter for PCIe 5.0 using Intel Clock Jitter Tool.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the PCI-SIG reference clock jitter.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Low Pass Filter**, **SSC Removal**, and **Noise Floor Deembed** option in the Clock Jitter Tool.
3. Performs compliance testing using the Clock Jitter Tool.
4. Captures the Noise Floor Signal if **Noise Floor Deembed** option is enabled.
5. Identifies overall test status.
6. Reports the overall test status, maximum phase jitter value, limits, and settings.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part VII
PCI Express Gen5 32.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

20 Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 32.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE **In case of Z-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.**

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

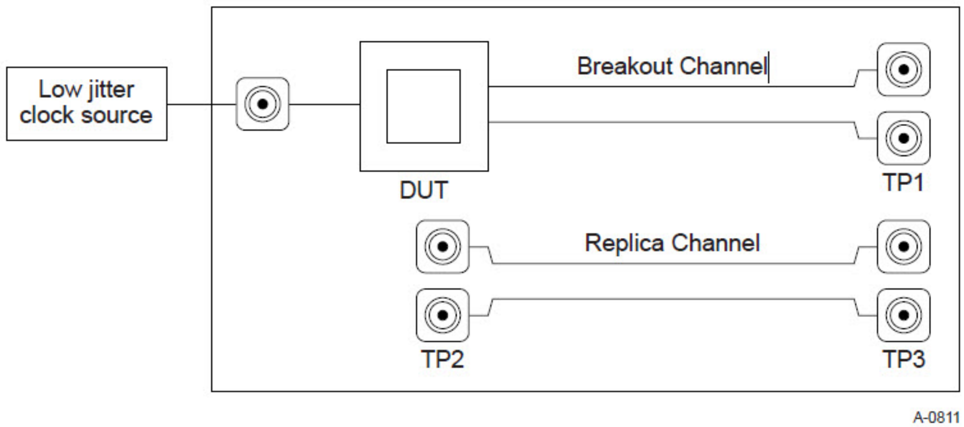


Figure 173 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 32.0 GT/s Tests > Transmitter (Tx) Tests**.

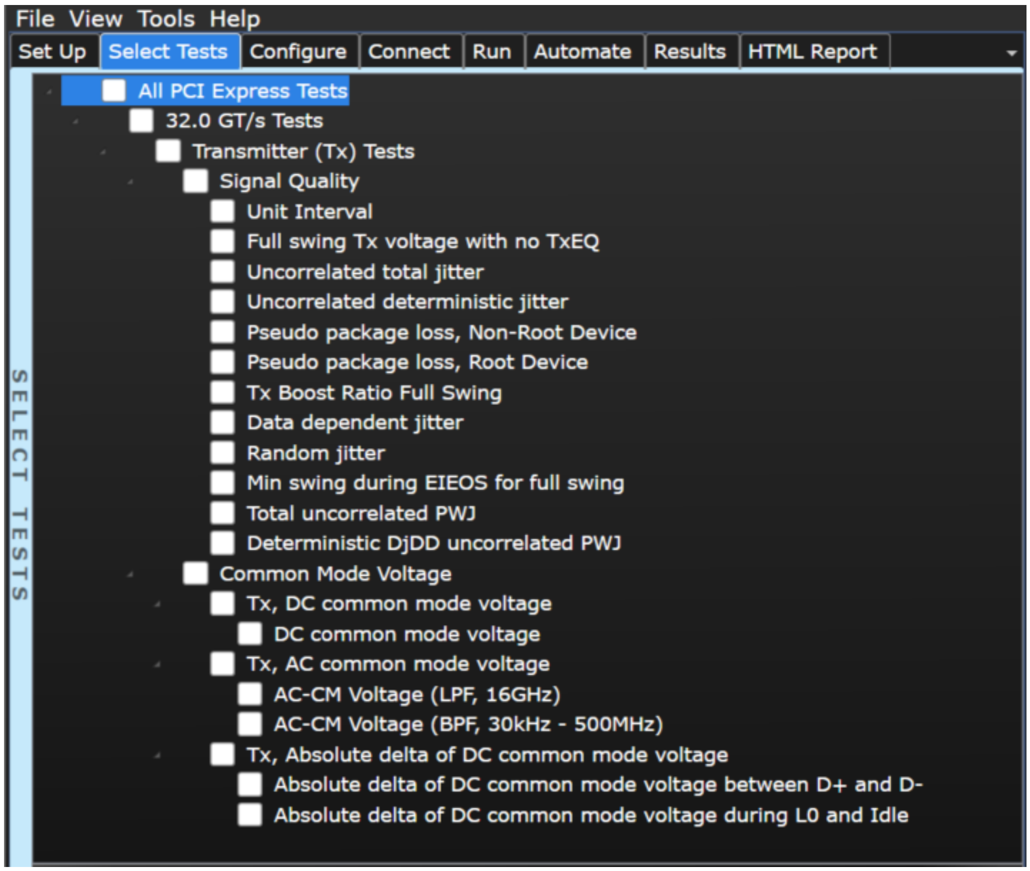


Figure 174 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 167 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.246875 ps	31.253125 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

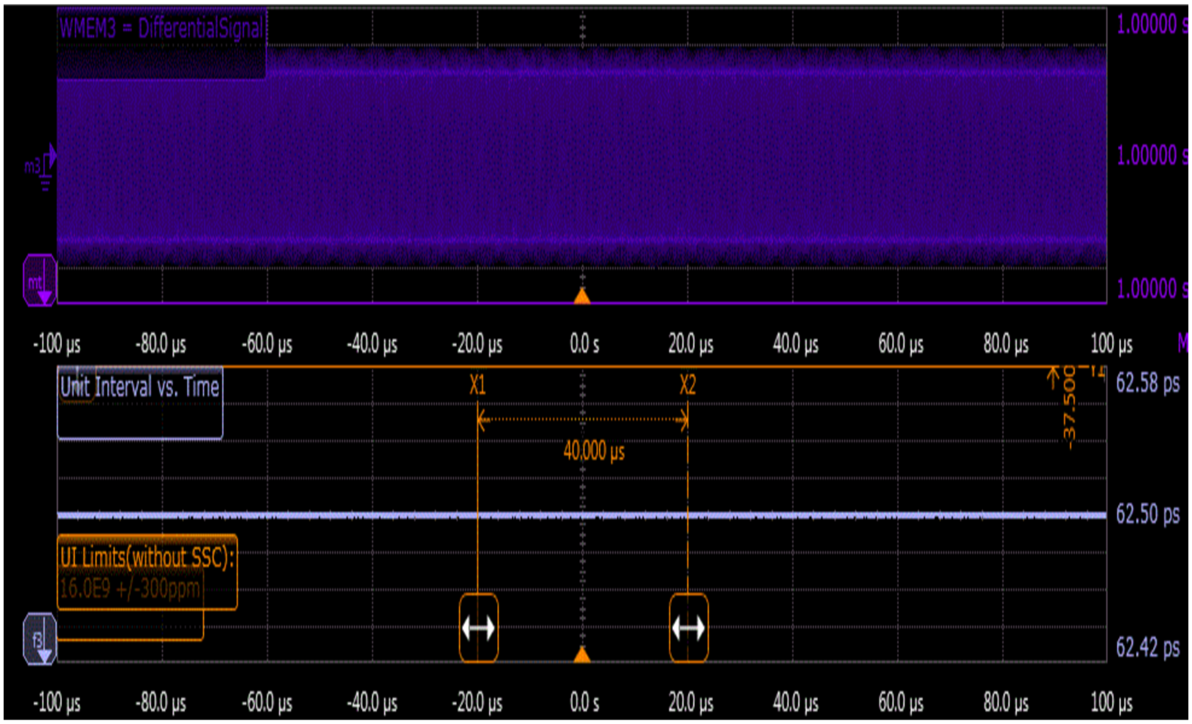


Figure 175 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 176. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP}$ is used as reference to check the compliance of the DUT.

Table 168 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DIFF\text{-}PP}$	Full swing Tx voltage with no TxEQ	800 mV	1300 mVPP

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

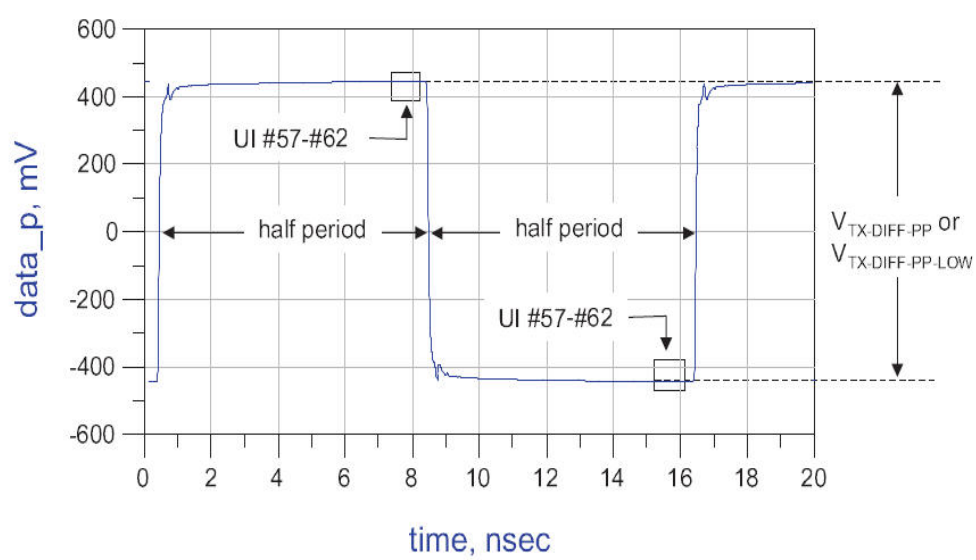


Figure 176 $V_{TX\text{-}DIFF\text{-}PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 177. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 169 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP-LOW}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times | V_{TXD+}-V_{TXD-}|$
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

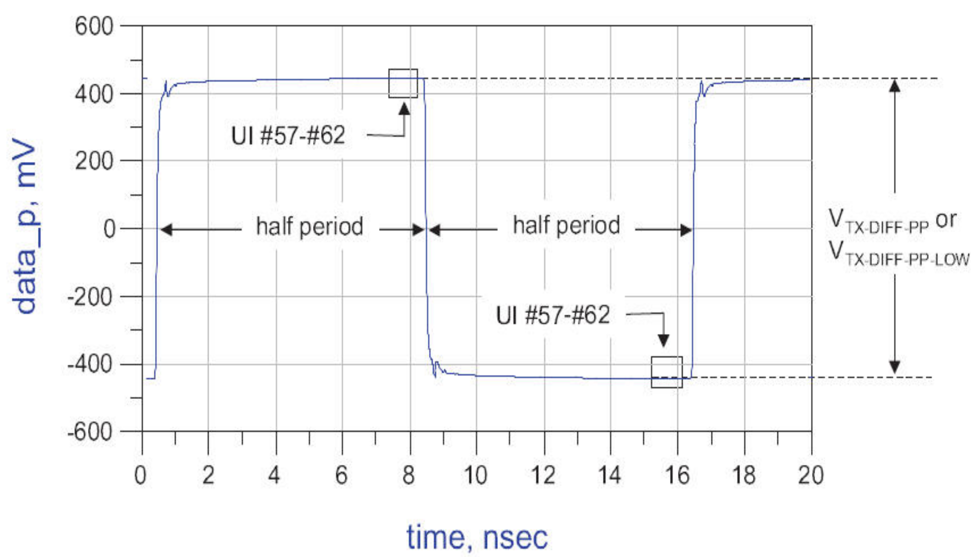


Figure 177 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

> **NOTE** Base - Transmitter Tests:
> MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 170 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 171 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	3.125 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

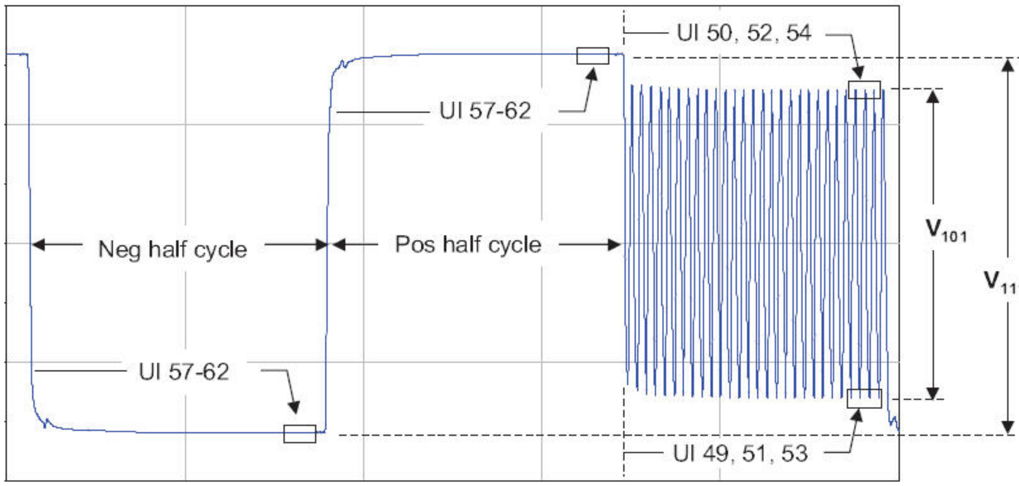
PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 172 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	8.5 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	3.7 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 178 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX-BOOST-FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 173 Tx Boost Ratio Full Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P10.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P10 signal in *.bin format.
13 Inputs the P10 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P10.
15 Reports the measurement of Vb during preset values P10 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 174 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 5.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 175 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	0.23 - 0.45 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJDD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI; at 32.0 GT/s the pattern is repeated for two consecutive blocks. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28 at 32.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages.
UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 176 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

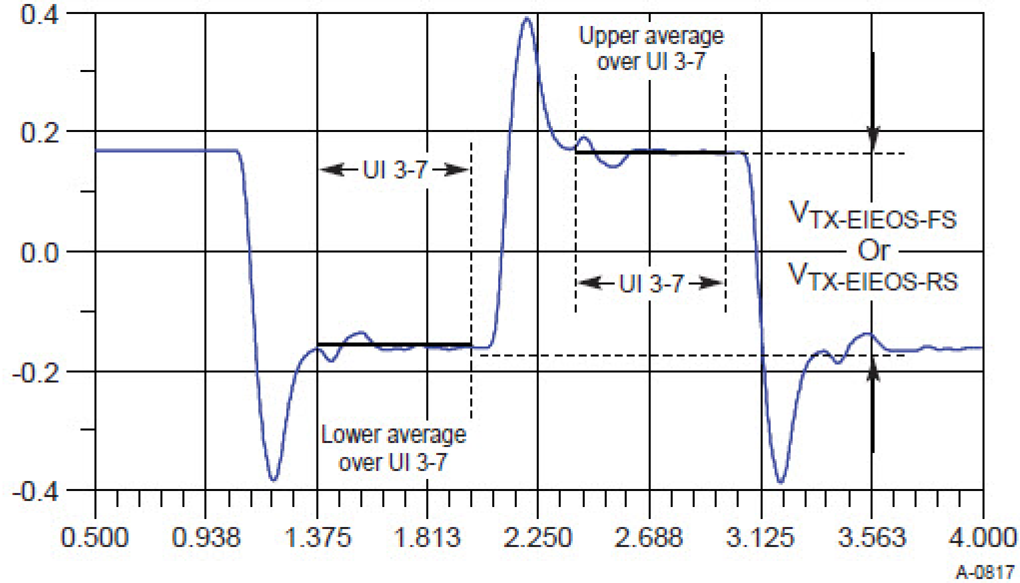


Figure 179 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 177 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

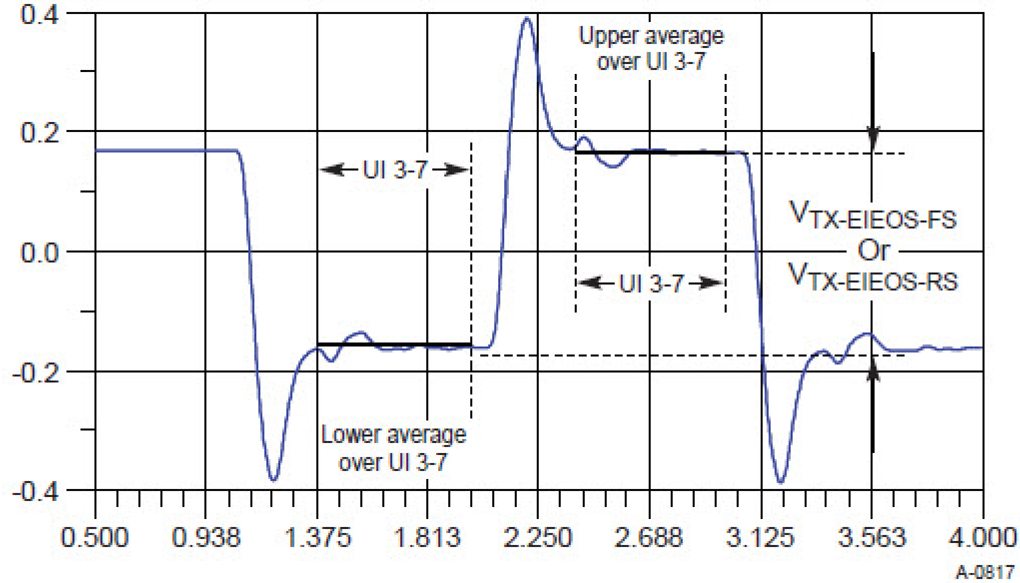


Figure 180 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 178 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.9

Table 179 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	2.5 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 180 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 32.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 181 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 32.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 182 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.33%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 32.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 183 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures memory depth and sampling rate as per the data rate..
3 Fits and displays all sample data on screen.
4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5 Analyzes measurements trend using the jitter **Meas Trend** function.
6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a Generates a differential plot (x_n - x_{n-1}).
   b The maximum slew rate corresponds to the peak of the differential plot.
7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

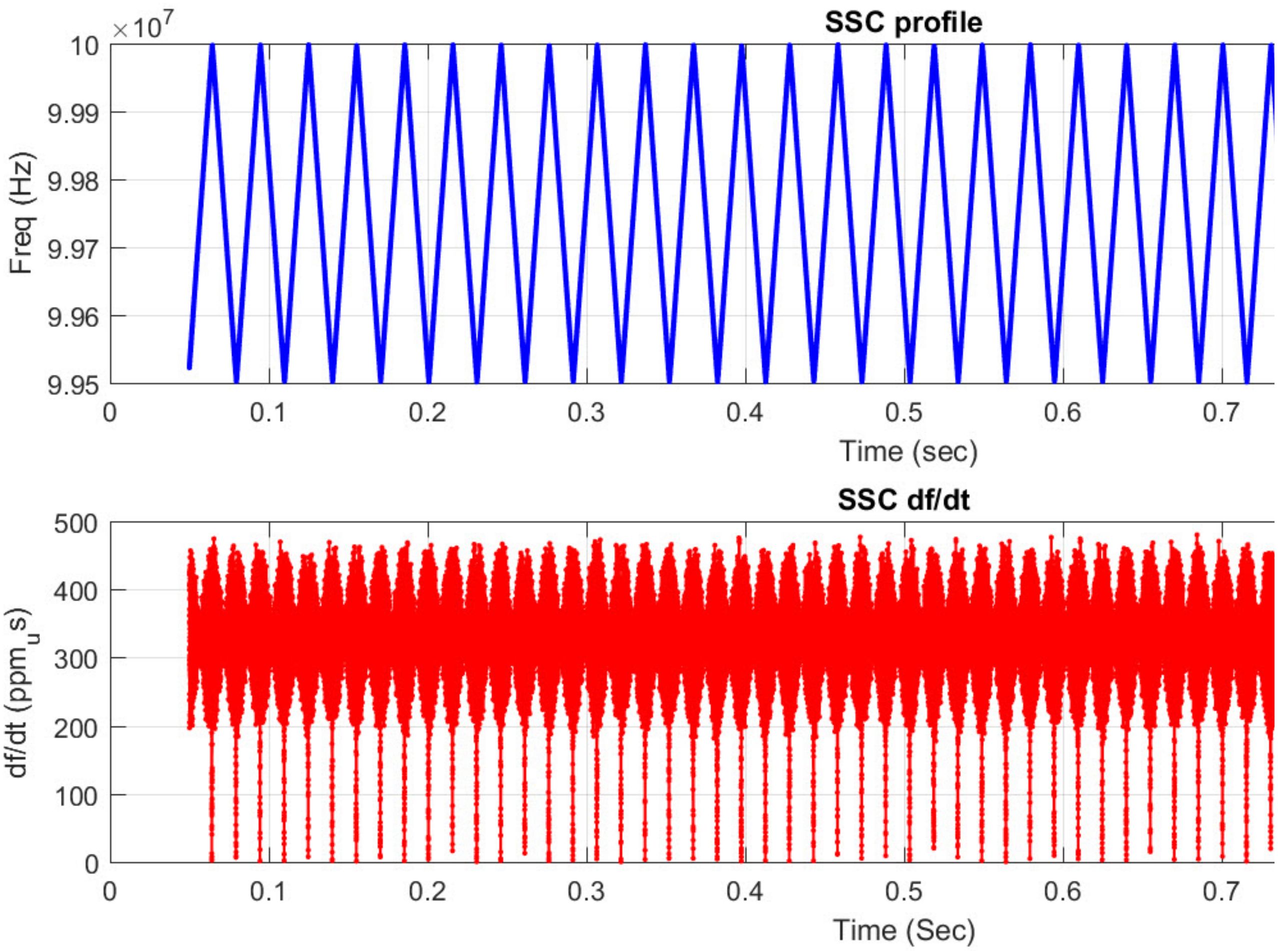


Figure 181 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 184 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage as follows:
   - *a* Enables and displays common mode measurements.
   - *b* Loads common mode signal to waveform memory.
   - *c* Loads and enhance dynamic range D+ signal and D- signal.
   - *d* Enables the average common mode measurement.
   - *e* Uses markers to indicate compliance test limit boundaries (0 V to 3.6 V).
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0 as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100 mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 16 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 185 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 186 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 16 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25\ mV$

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 187 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
- DC Common Mode Line Delta
- Average DC value of D+
- Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 188 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

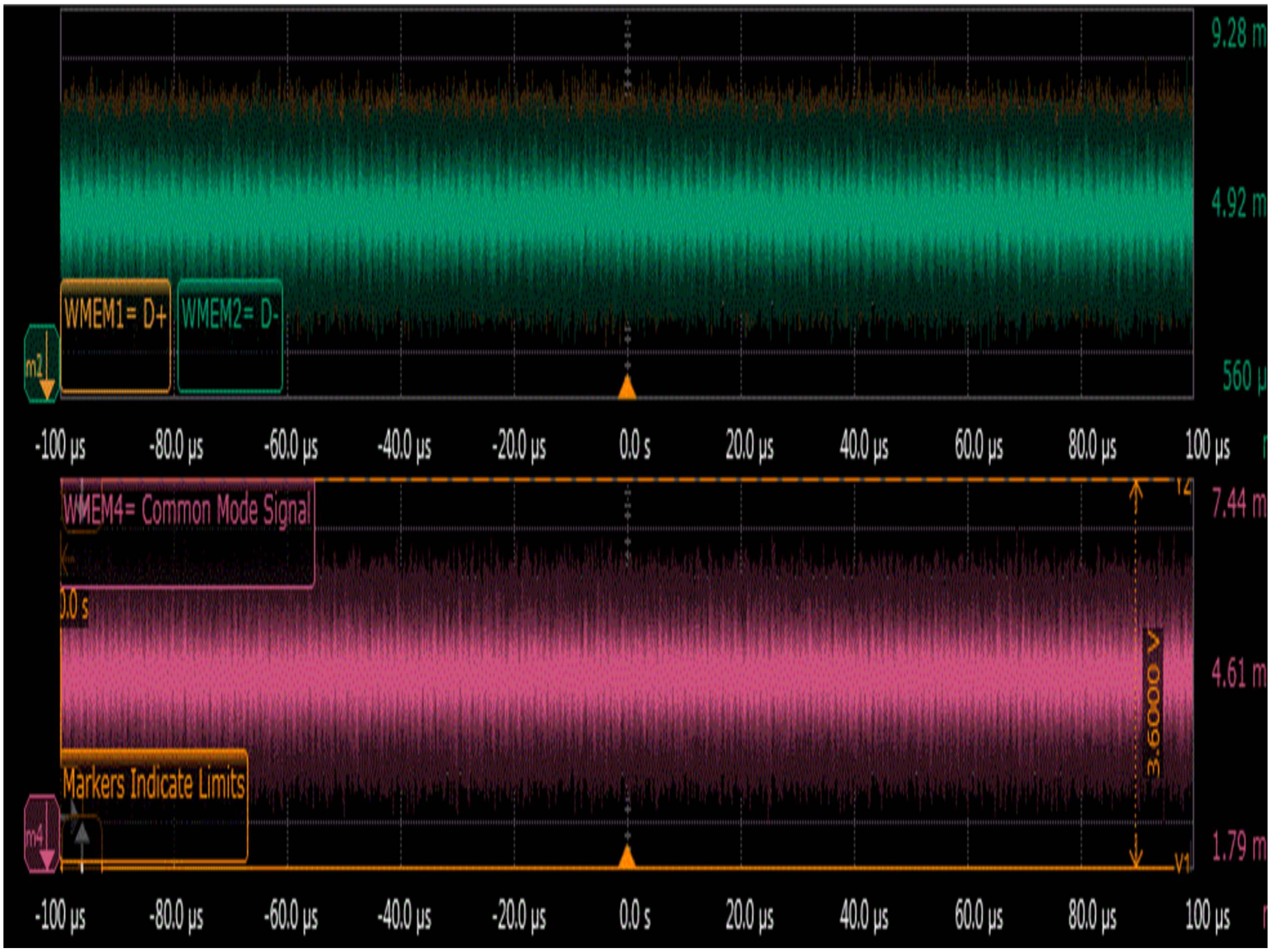


Figure 182 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to "Equalization Presets Tests".

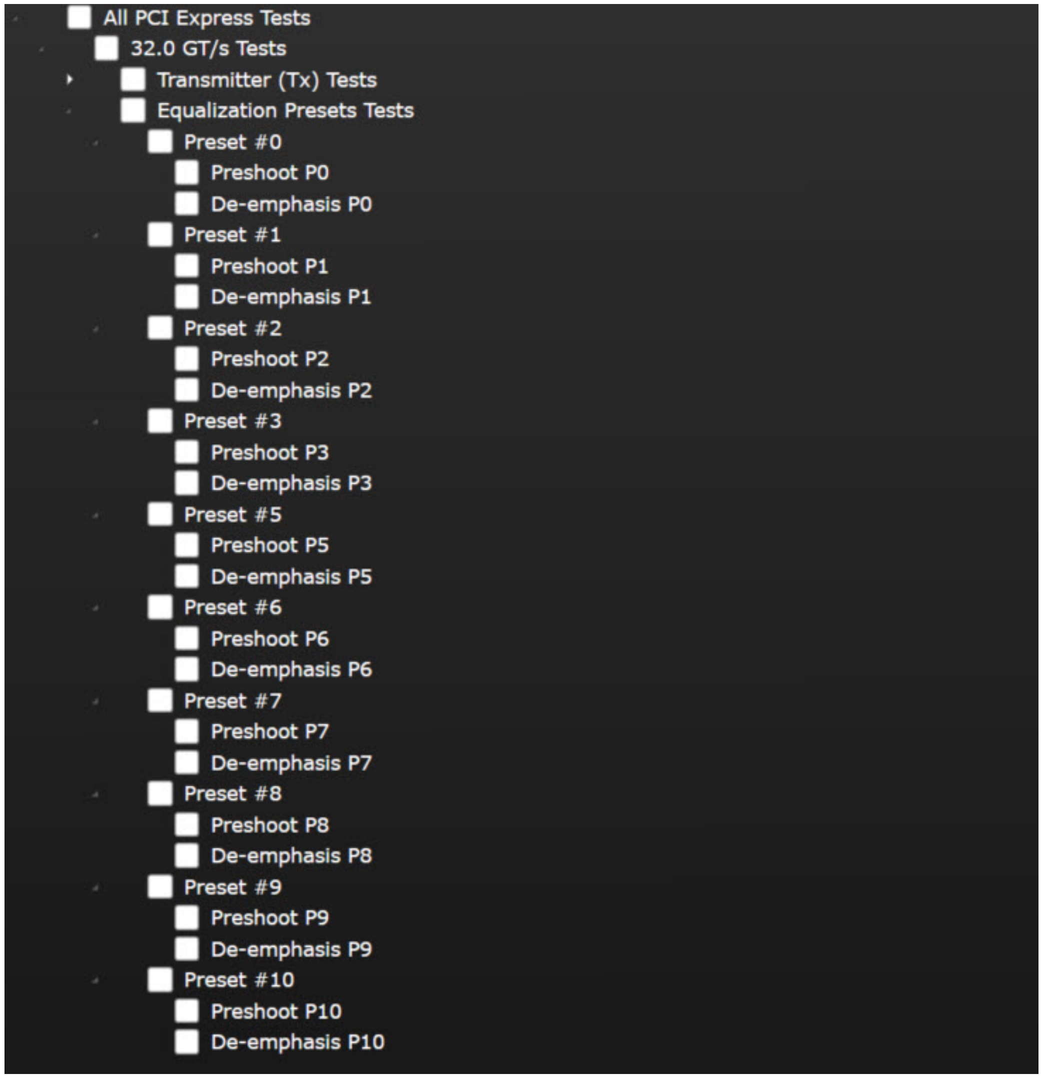


Figure 183 Selecting Equalization Presets Tests

Preset #0 Measurement (P0), Preshoot Test

This test verifies that the preshoot of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s, and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 184.

Table 189 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

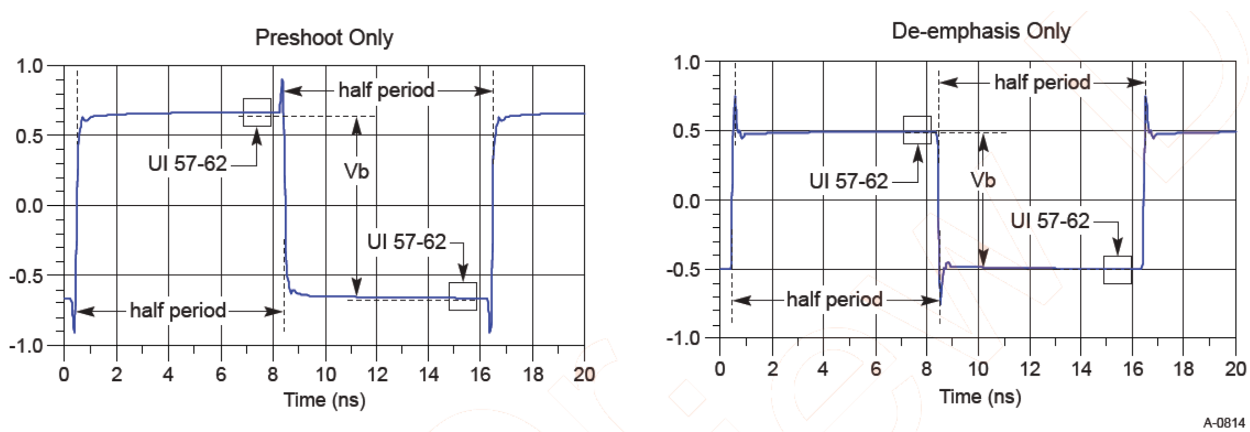


Figure 184 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 190 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	-6.0 ± 1.5 dB	0.000	–0.250	1.000	0.500	0.500

Table 191 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	-6.0 ± 2.5 dB	0.000	–0.250	1.000	0.500	0.500

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P0.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P0 signal in *.bin format.
12 Inputs the P4 and P0 saved waveforms into SigTest tool (AC calculation method).
13 Computes the preshoot at preset value P0.
14 Compares the preshoot value to the general compliance test limits (see Table 190).
15 If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 191).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #0 Measurement (P0), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 185.

Table 192 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

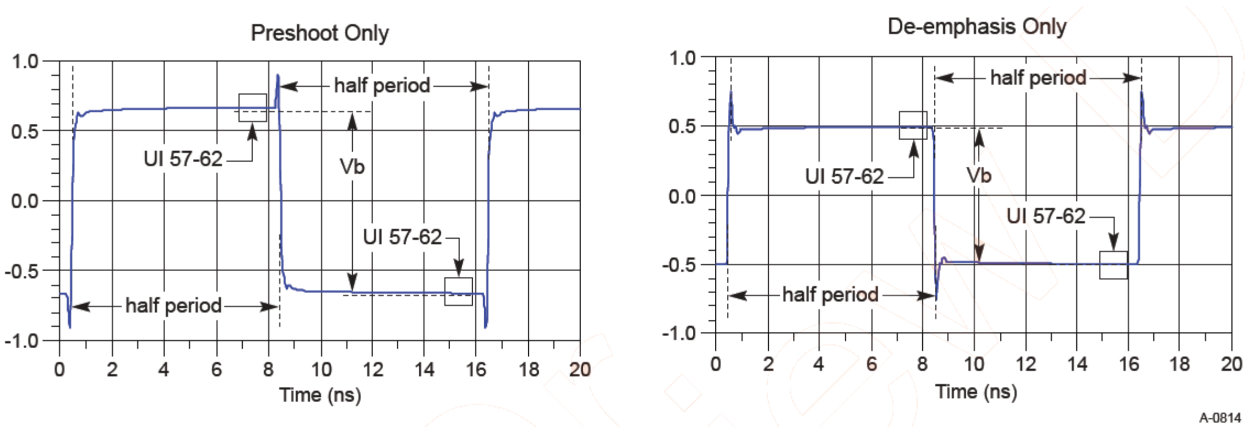


Figure 185 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 193 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	-6.0 ± 1.5 dB	0.000	–0.250	1.000	0.500	0.500

Table 194 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	-6.0 ± 2.5 dB	0.000	–0.250	1.000	0.500	0.500

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P0.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P0 signal in *.bin format.
12. Inputs the P4 and P0 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P0.
14. Compares the de-emphasis value to the general compliance test limits (see Table 193).

15 If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 194).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (P1), Preshoot Test

This test verifies that the preshoot of the preset number P1 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 184.

Table 195 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

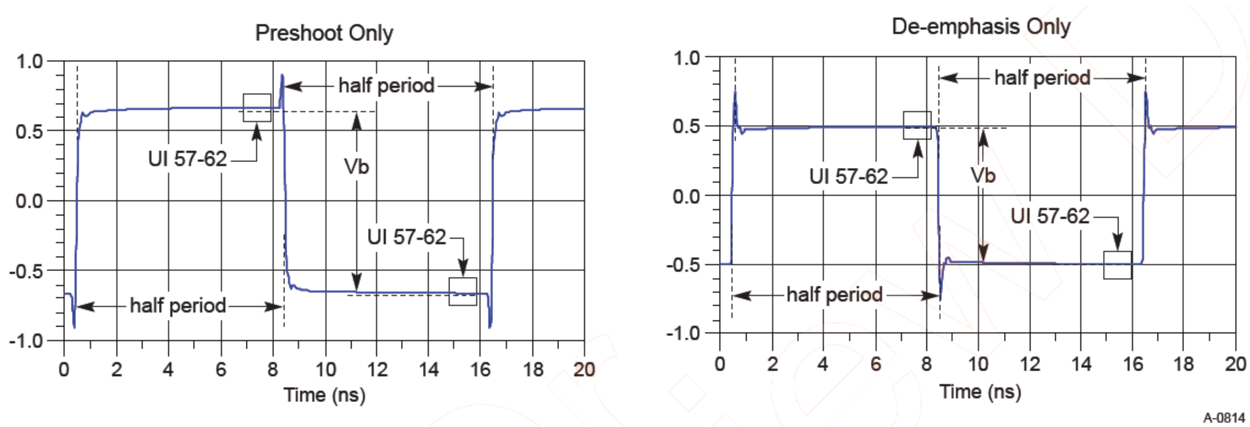


Figure 186 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 196 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	-3.5 ± 1 dB	0.000	–0.167	1.000	0.668	0.668

Table 197 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	-3.5 ± 2.0 dB	0.000	–0.167	1.000	0.668	0.668

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P1.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P1 signal in *.bin format.
12 Inputs the P4 and P1 saved waveforms into SigTest tool (AC calculation method).
13 Computes the preshoot at preset value P1.
14 Compares the preshoot value to the general compliance test limits (see Table 196).
15 If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 197).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (P1), De-emphasis Test

This test verifies that the de-emphasis of the preset number P1 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 187.

Table 198 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

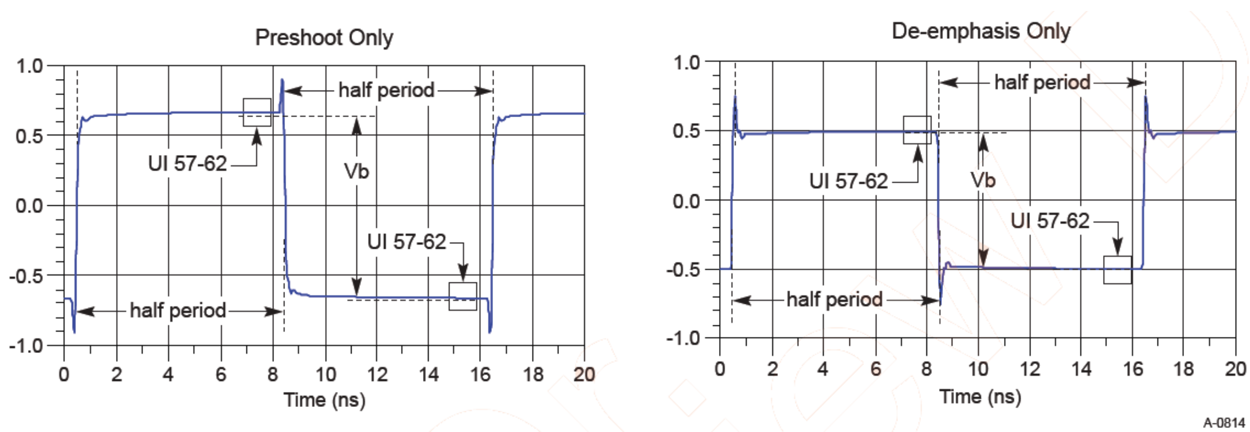


Figure 187 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 199 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	-3.5 ± 1 dB	0.000	–0.167	1.000	0.668	0.668

Table 200 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	-3.5 ± 2.0 dB	0.000	–0.167	1.000	0.668	0.668

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P1.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P1 signal in *.bin format.
12 Inputs the P4 and P1 saved waveforms into SigTest tool (AC calculation method).
13 Computes the de-emphasis at preset value P1.
14 Compares the de-emphasis value to the general compliance test limits (see Table 199).
15 If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 200).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), Preshoot Test

This test verifies that the preshoot of the preset number P2 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 184.

Table 201 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

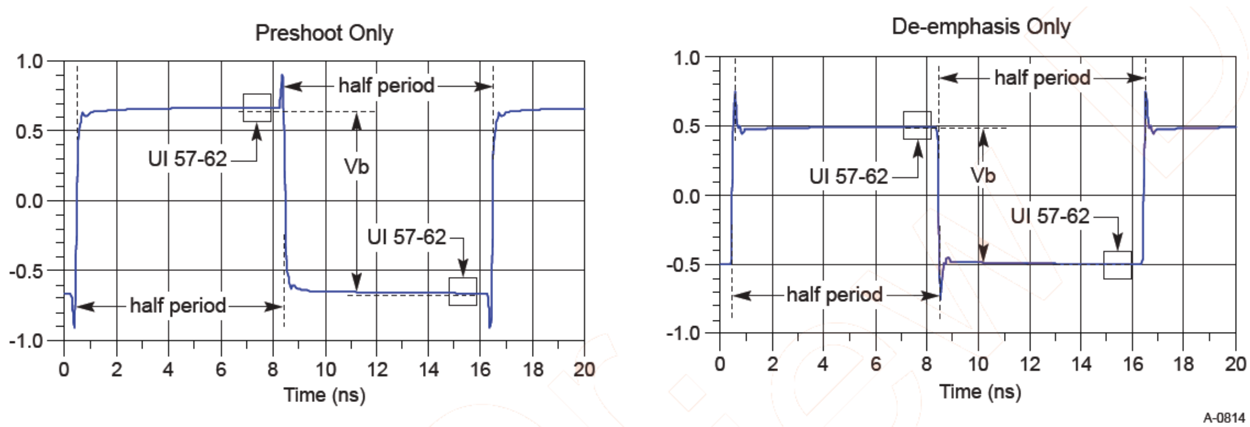


Figure 188 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 202 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	-4.4 ± 1.5 dB	0.000	–0.200	1.000	0.600	0.600

Table 203 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	-4.4 ± 2.5 dB	0.000	–0.200	1.000	0.600	0.600

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P2.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P2 signal in *.bin format.
12. Inputs the P4 and P2 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P2.
14. Compares the preshoot value to the general compliance test limits (see Table 202).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 203).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

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17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis Test

This test verifies that the de-emphasis of the preset number P2 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 189.

Table 204 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

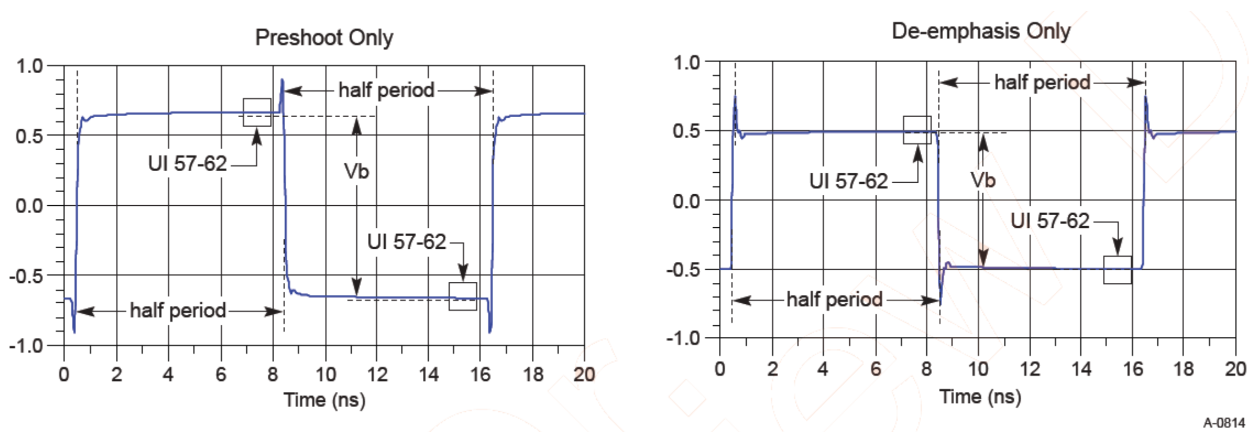

Figure 189 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 205 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	-4.4 ± 1.5 dB	0.000	–0.200	1.000	0.600	0.600

Table 206 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	-4.4 ± 2.5 dB	0.000	–0.200	1.000	0.600	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain** Scale to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P2.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P2 signal in *.bin format.
12 Inputs the P4 and P2 saved waveforms into SigTest tool (AC calculation method).
13 Computes the de-emphasis at preset value P2.
14 Compares the de-emphasis value to the general compliance test limits (see Table 205).

15 If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 206).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), Preshoot Test

This test verifies that the preshoot of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 184.

Table 207 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

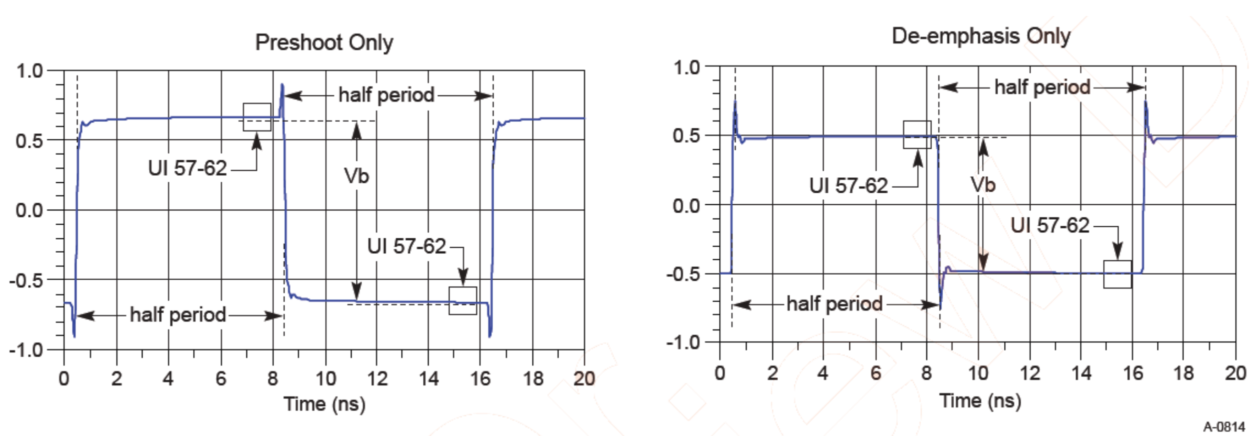

Figure 190 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 208 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750

Table 209 **Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits**

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 2.0 dB	0.000	-0.125	1.000	0.750	0.750

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P3.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P3 signal in *.bin format.
12. Inputs the P4 and P3 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P3.
14. Compares the preshoot value to the general compliance test limits (see Table 208).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 209).

NOTE

If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis Test

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 191.

Table 210 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

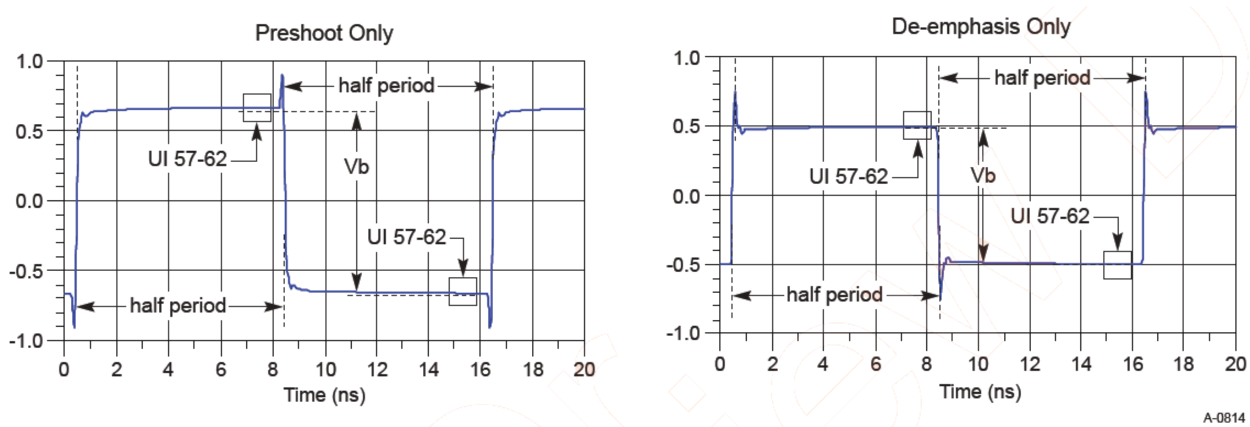

Figure 191 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 211 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750

Table 212 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 2.0 dB	0.000	-0.125	1.000	0.750	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveforms into SigTest tool (AC calculation method).
13 Computes the de-emphasis at preset value P3.
14 Compares the de-emphasis value to the general compliance test limits (see Table 211).
15 If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 212).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot Test

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 192

Table 213 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

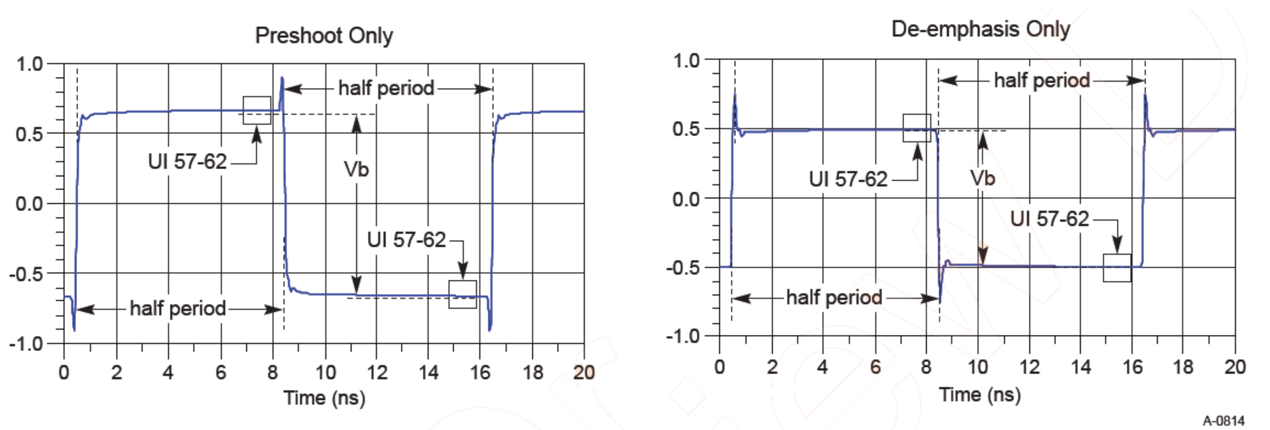

Figure 192 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 214 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Table 215 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 2.0 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P5.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P5 signal in *.bin format.
12. Inputs the P4 and P5 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P5.
14. Compares the preshoot value to the general compliance test limits (see Table 214).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 215).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), De-emphasis Test

This test verifies that the de-emphasis of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 191.

Table 216 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

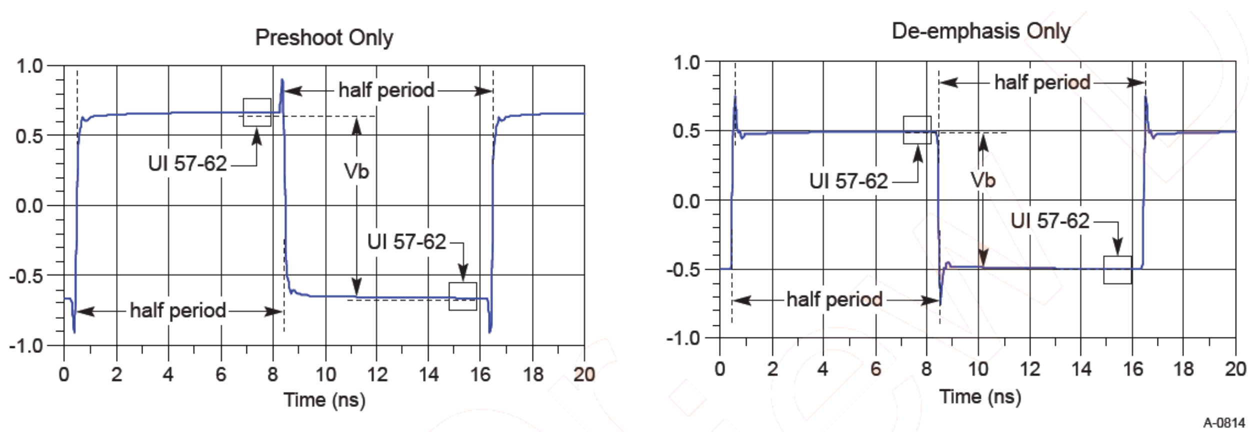

Figure 193 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 217 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Table 218 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 2.0 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P5.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P5 signal in *.bin format.
12. Inputs the P4 and P5 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P5.
14. Compares the de-emphasis value to the general compliance test limits (see Table 217).
15. If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 218).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot Test

This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 194.

Table 219 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

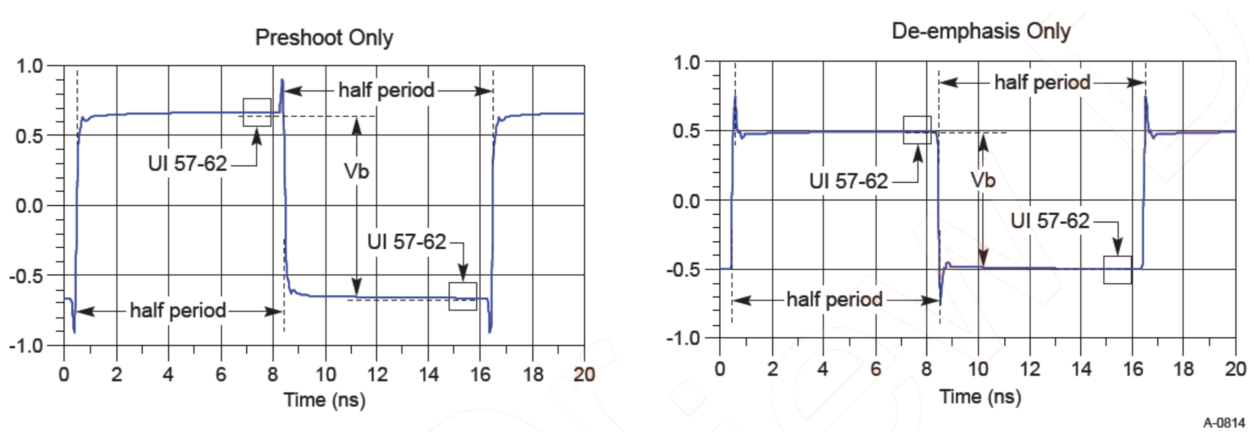

Figure 194 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 220 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Table 221 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 2.0 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P6.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P6 signal in *.bin format.
12. Inputs the P4 and P6 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P6.
14. Compares the preshoot value to the general compliance test limits (see Table 220).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits.

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

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17 If the test again fails with relaxed compliance test limits, it is marked as fail (see Table 221).

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), De-emphasis Test

This test verifies that the de-emphasis of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 191.

Table 222 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

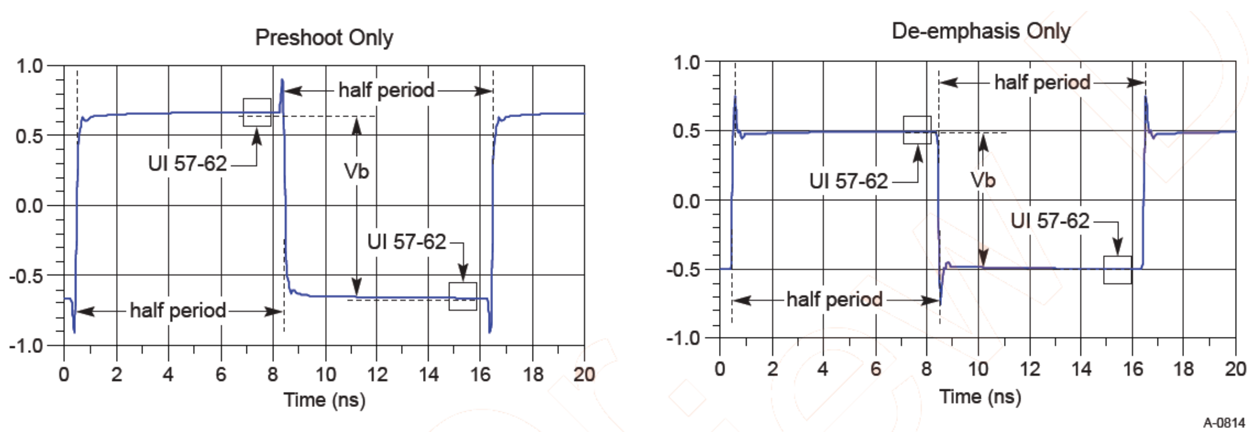


Figure 195 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 223 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Table 224 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 2.0 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P6.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P6 signal in *.bin format.
12 Inputs the P4 and P6 saved waveforms into SigTest tool (AC calculation method).
13 Computes the de-emphasis at preset value P6.
14 Compares the de-emphasis value to the general compliance test limits (see Table 223).
15 If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 224).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot Test

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 194.

Table 225 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

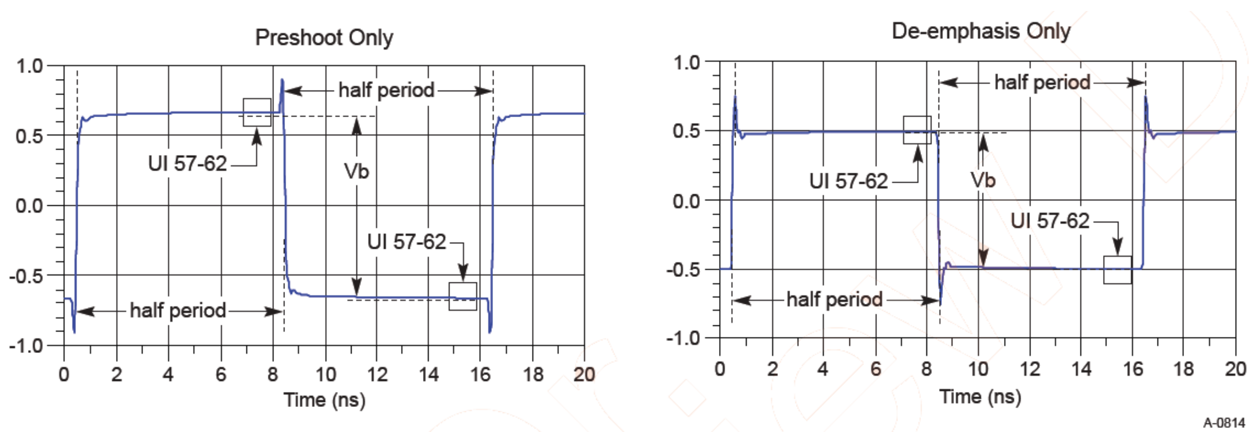


Figure 196 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 226 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600

Table 227 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 2.0 dB	-6.0 ± 2.5 dB	-0.100	-0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P2.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P2 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P2 and P7 saved waveforms into SigTest tool (AC calculation method).
13 Computes the preshoot at preset value P7.
14 Compares the preshoot value to the general compliance test limits (see Table 226).
15 If the preshoot value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 227).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis Test

This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 191.

Table 228 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

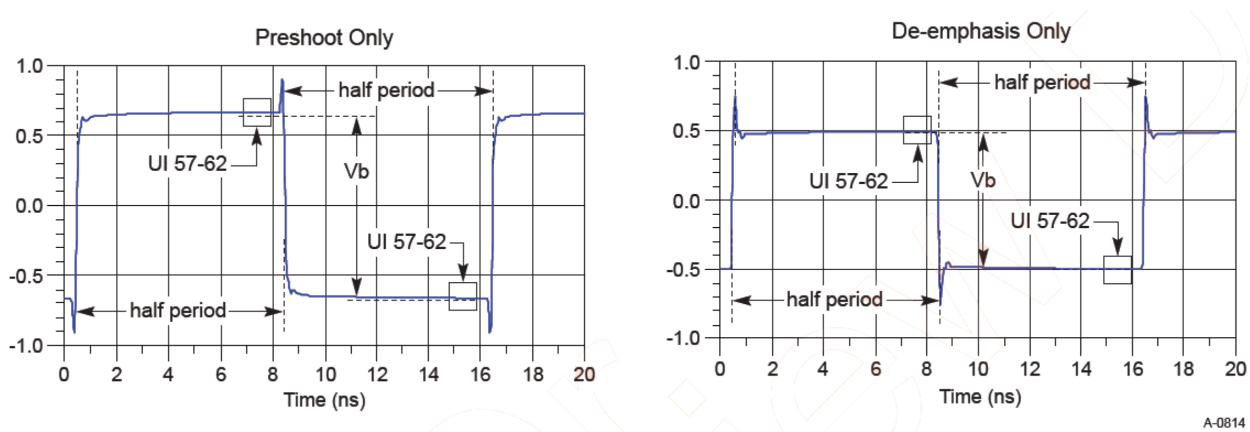


Figure 197 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 229 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600

Table 230 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 2.0 dB	-6.0 ± 2.5 dB	-0.100	-0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P5.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P5 signal into *.bin format.
7. Configures the DUT to operate in preset value #P7.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P7 signal in *.bin format.
12. Inputs the P5 and P7 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P7.
14. Compares the de-emphasis value to the general compliance test limits (see Table 229).
15. If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.

16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 230).

NOTE **If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.**

17 If the test again fails with relaxed compliance test limits, it is marked as fail.

18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.

19 If the test fails, the test is marked as fail or else pass.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot Test

This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 198.

Table 231 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

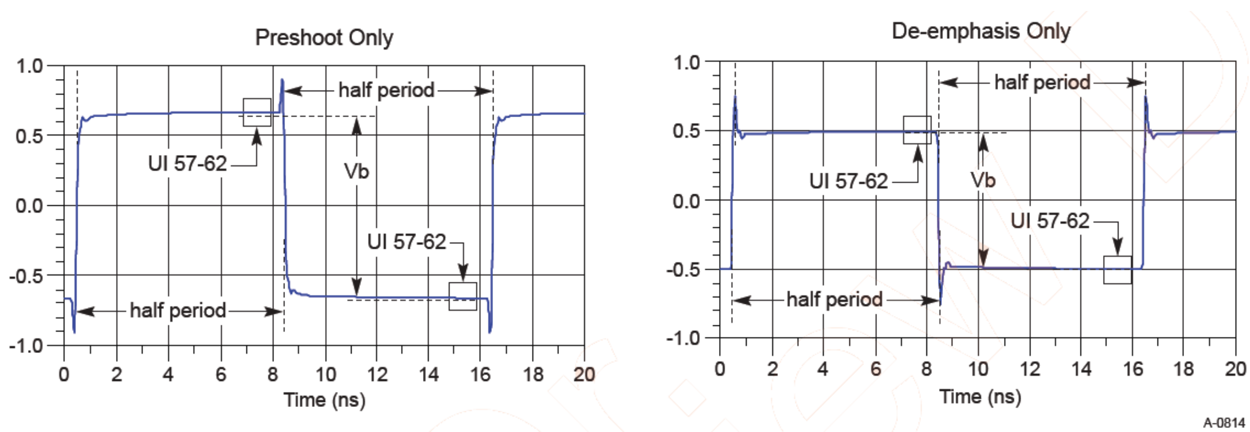


Figure 198 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 232 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750

Table 233 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 2.0 dB	-3.5 ± 2.0 dB	-0.125	-0.125	0.750	0.500	0.750

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P3.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P3 signal into *.bin format.
7. Configures the DUT to operate in preset value #P8.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P8 signal in *.bin format.
12. Inputs the P3 and P8 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P8.
14. Compares the preshoot value to the general compliance test limits (see Table 232).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.
16. If the test fails, the application compares the result with relaxed compliance test limits (see Table 233).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.
18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis Test

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 199.

Table 234 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

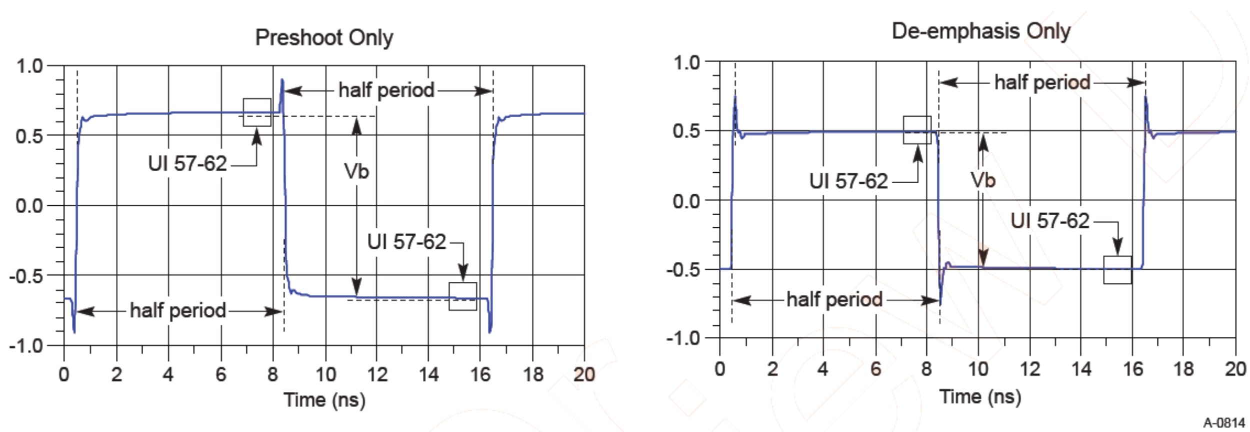


Figure 199 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 235 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Table 236 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 2.0 dB	–3.5 ± 2.0 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P6.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P6 signal into *.bin format.
7. Configures the DUT to operate in preset value #P8.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P8 signal in *.bin format.
12. Inputs the P6 and P8 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P8.
14. Compares the de-emphasis value to the general compliance test limits (see Table 235).
15. If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.
16. If the test fails, the application compares the result with relaxed compliance test limits (see Table 236).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17. If the test again fails with relaxed compliance test limits, it is marked as fail.
18. If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19. If the test fails, the test is marked as fail or else pass.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot Test

This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 200.

Table 237 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

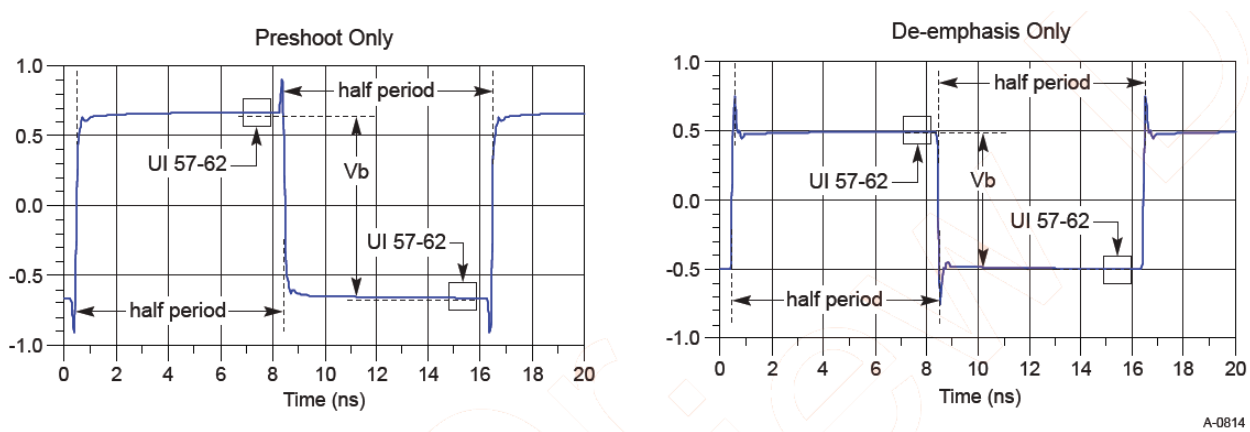


Figure 200 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 238 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Table 239 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 2.0 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P9.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P9 signal in *.bin format.
12. Inputs the P4 and P9 saved waveforms into SigTest tool (AC calculation method).
13. Computes the preshoot at preset value P9.
14. Compares the preshoot value to the general compliance test limits (see Table 238).
15. If the preshoot value is within the general compliance test limits, the test result is marked as pass.
16. If the test fails, the application compares the result with relaxed compliance test limits (see Table 239).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17. If the test again fails with relaxed compliance test limits, it is marked as fail.
18. If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19. If the test fails, the test is marked as fail or else pass.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), De-emphasis Test

This test verifies that the de-emphasis of the preset number P9 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 199.

Table 240 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

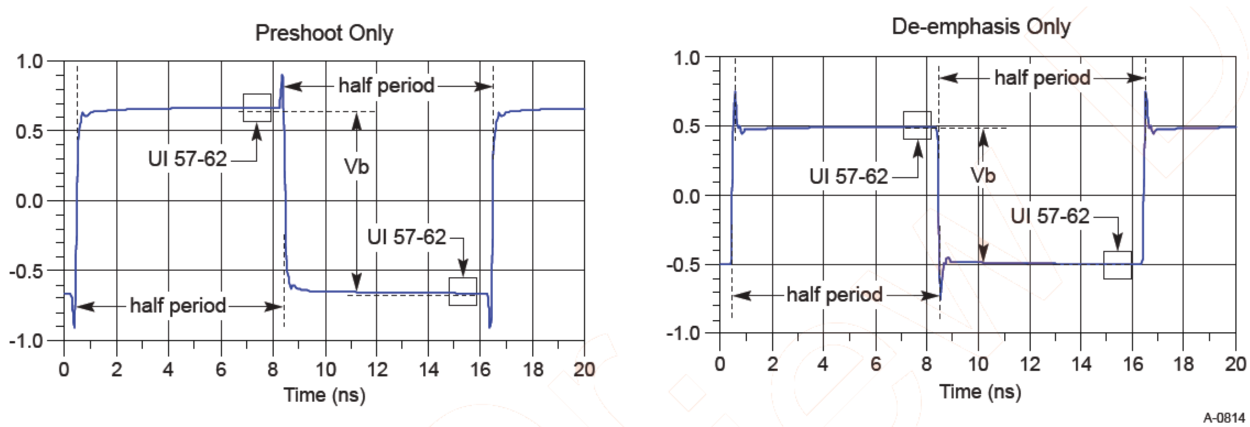


Figure 201 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 241 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Table 242 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 2.0 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P9.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P9 signal in *.bin format.
12. Inputs the P4 and P9 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P9.
14. Compares the de-emphasis value to the general compliance test limits (see Table 241).
15. If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.
16. If the test fails, the application compares the result with relaxed compliance test limits (see Table 242).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17. If the test again fails with relaxed compliance test limits, it is marked as fail.
18. If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19. If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), Preshoot Test

This test verifies that the preshoot of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 200.

Table 243 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

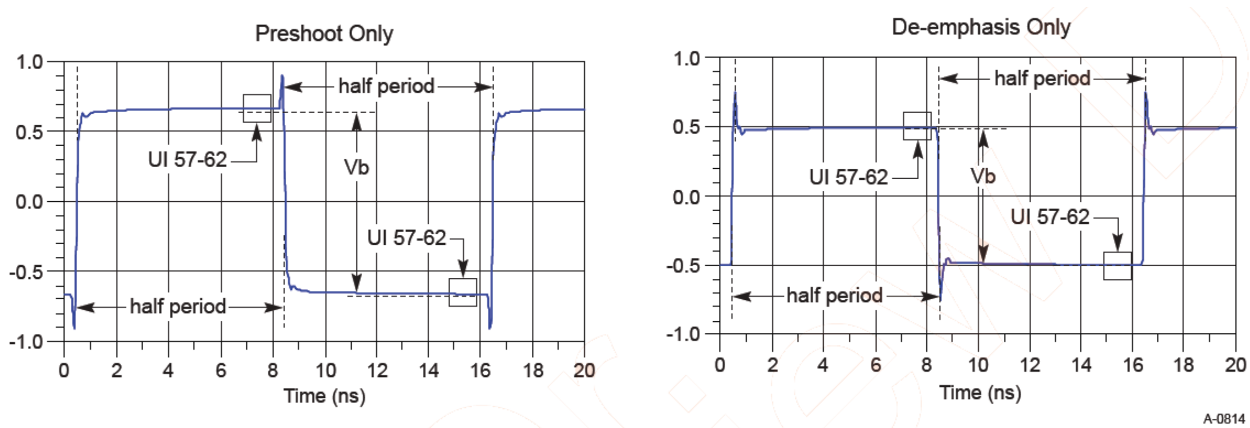


Figure 202 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 244 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	Note 2	0.000	Note 2	1.000	Note 2	Note 2

Note 2 (PCIe Base Spec):
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training.P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Table 245 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	Note 2*	0.000	Note 2	1.000	Note 2	Note 2

Note 2 (PCIe Base Spec):
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training.P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

* “Note2” limits already contain a tolerance of $\pm$ 1dB, and in case of relaxed limits an additional $\pm$ 1dB of tolerance is included.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P10.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P10 saved waveforms into SigTest tool (AC calculation method).
13 Computes the preshoot at preset value P10.
14 Compares the preshoot value to the general compliance test limits (see Table 244).
15 If the preshoot value is within the general compliance test limits, the test result is marked as pass.
16 If the test fails, the application compares the result with relaxed compliance test limits (see Table 245).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17 If the test again fails with relaxed compliance test limits, it is marked as fail.
18 If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19 If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis Test

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 203.

Table 246 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

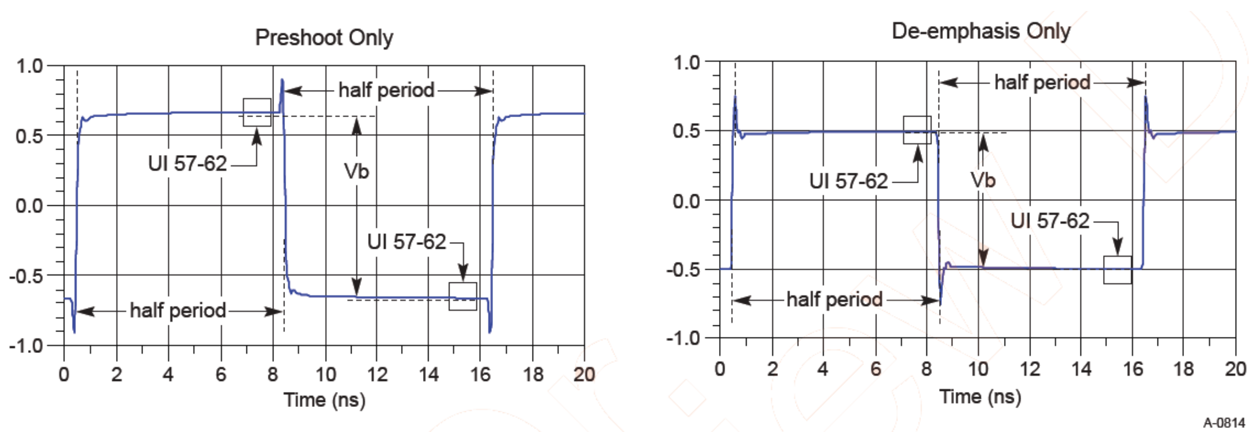


Figure 203 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 247 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	Note 2	0.000	Note 2	1.000	Note 2	Note 2

Note 2 (PCIe Base Spec):
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training.P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Table 248 Tx Preset Ratios and Corresponding Coefficient Values - Relaxed Limits

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	Note 2*	0.000	Note 2	1.000	Note 2	Note 2

Note 2 (PCIe Base Spec):
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training.P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

* “Note2” limits already contain a tolerance of ± 1dB, and in case of relaxed limits an additional ± 1dB of tolerance is included.

Test Definition Notes from the Specification

P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P10.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P10 signal in *.bin format.
12. Inputs the P4 and P10 saved waveforms into SigTest tool (AC calculation method).
13. Computes the de-emphasis at preset value P10.
14. Compares the de-emphasis value to the general compliance test limits (see Table 247).
15. If the de-emphasis value is within the general compliance test limits, the test result is marked as pass.
16. If the test fails, the application compares the result with relaxed compliance test limits (see Table 248).

NOTE If any preset measurement fails at this step with compliance test limits, all presets must be re-evaluated as mentioned in Step 17-19.

17. If the test again fails with relaxed compliance test limits, it is marked as fail.
18. If the test passes, the application performs the measurement again using SigTest tool (DC calculation method), and compares the result with general compliance test limits.
19. If the test fails, the test is marked as fail or else pass.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

21 CEM-EndPoint Tests, 32.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-EndPoint tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE In case of Z-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

Probing the Link for CEM-EndPoint Compliance

Connecting the Compliance Base Board for CEM-EndPoint Testing

There are multiple pairs of MMPX connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB, and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test).

When probing and two channels are used, channel-to-channel deskew may be required (see "Channel-to-Channel De-skew" on page 1223).

For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

NOTE

When probing and two channels are used, channel-to-channel de-skew may be required (see "Channel-to-Channel De-skew" on page 1223).

For more information on the probe amplifier and differential probe heads, see Appendix C, "InfiniiMax Probing Options," starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running CEM-EndPoint Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 32.0 GT/s Tests > CEM EndPoint Tests**.

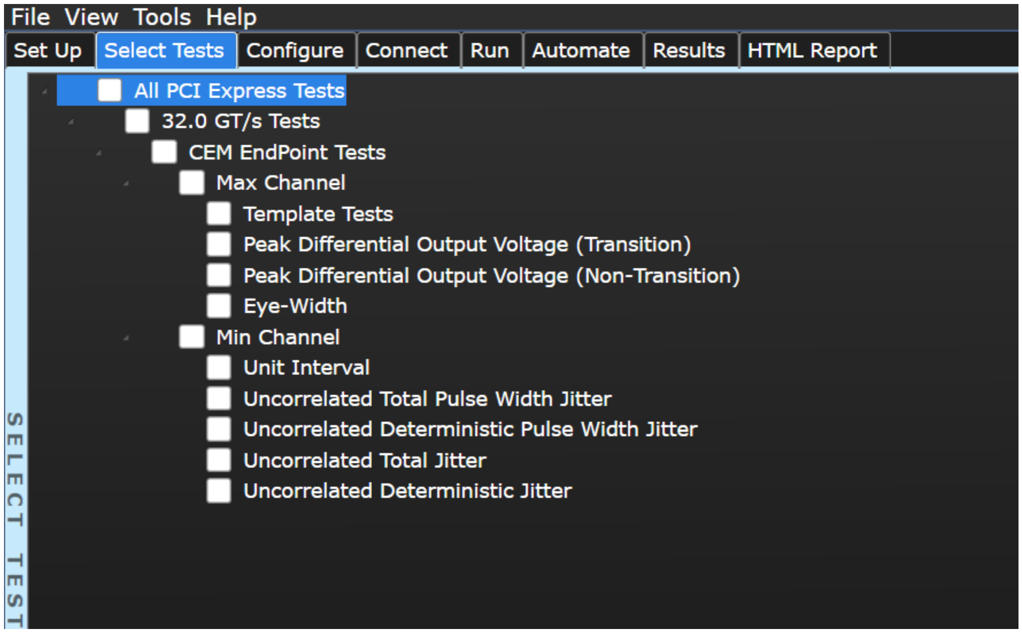


Figure 204 Selecting CEM EndPoint Tests

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM). This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{txA_d}).

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.1, Figure 4-7 is used as reference to check the compliance of the DUT.

Table 249 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	22 mV	1300 mV	Notes 1, 2, 4
T_{TXA}	10.625 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for system board crosstalk that is not present during measurement.

2 V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least $2x10^{6}$ UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 18 dB at 16 Hz, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 32.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

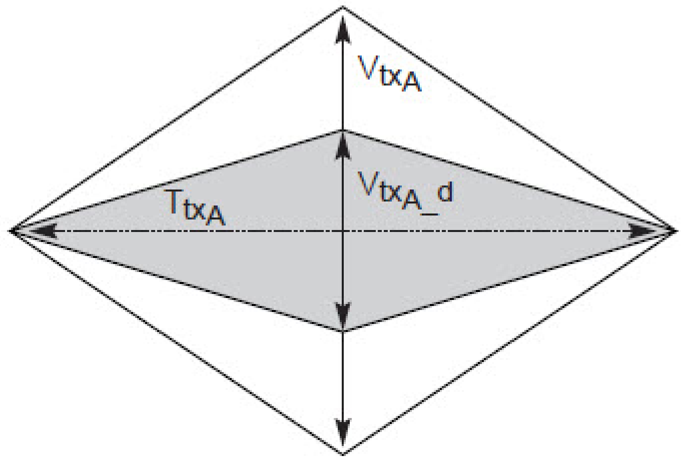


Figure 205 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs compliance testing using the SigTestWrapper.dll file.
   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

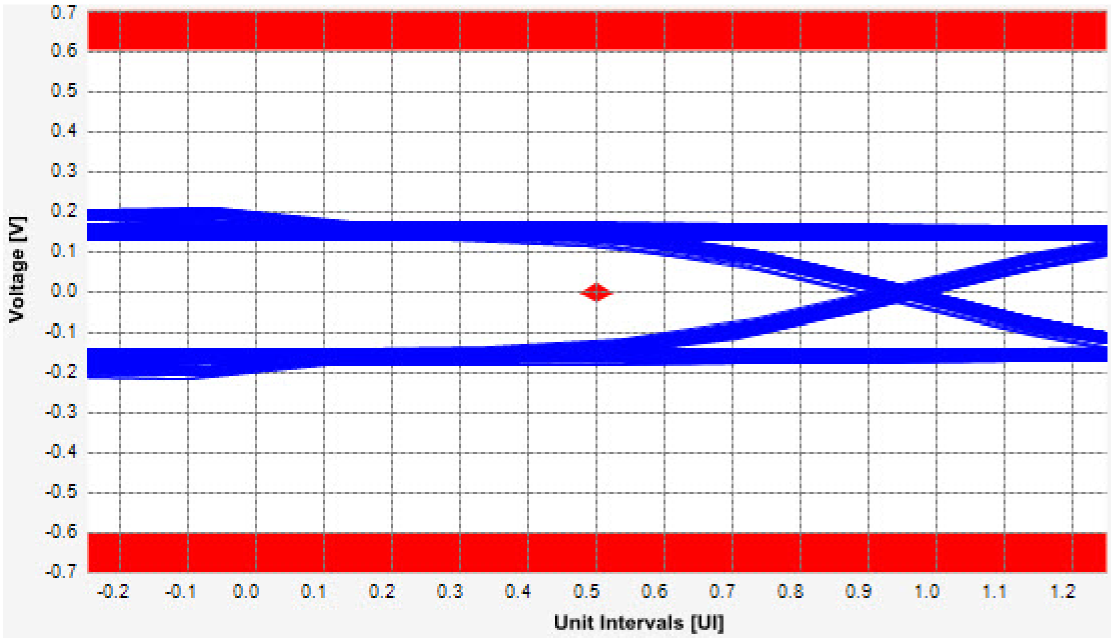


Figure 206 Reference Image for Template (Transition) Test

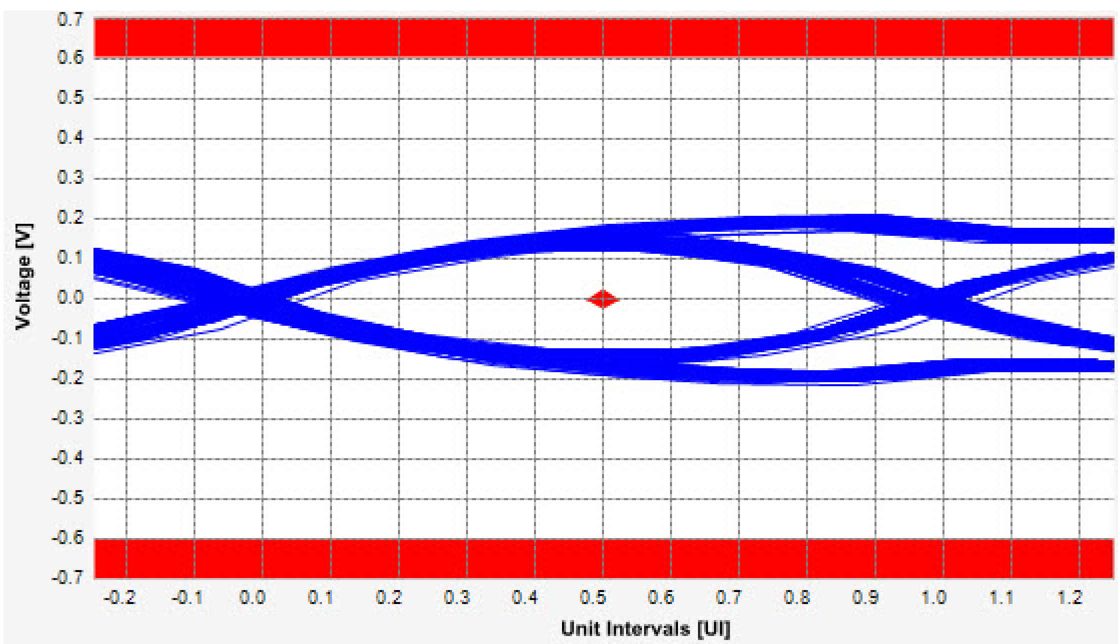


Figure 207 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.5, Table 4-16 is used as reference to check the compliance of the DUT.

Table 250 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	22 mV	1300 mV	Notes 1, 2, 4
T_{TXA}	10.625 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for system board crosstalk that is not present during measurement.

2 V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least $2x10^6$ UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 18 dB at 16 Hz, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 32.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

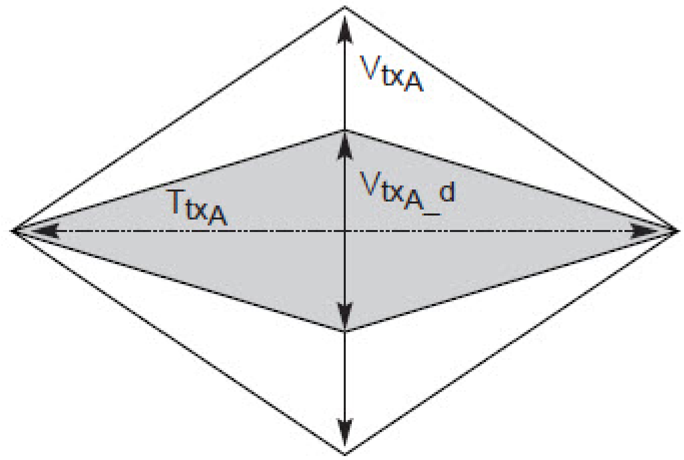


Figure 208 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> This test requires the template test with the following specifications:
>
> Device: PCIE 5.0
>
> Data Rate: 32.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

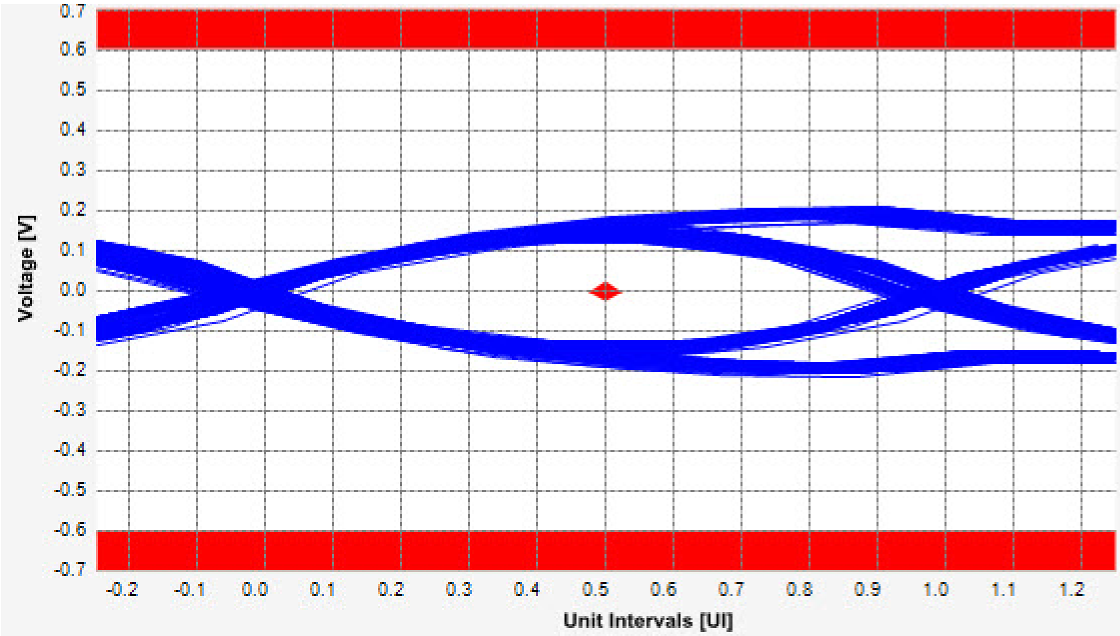


Figure 209 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test (Information Only)

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}), Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.5, Table 4-16 is used as reference to check the compliance of the DUT.

Table 251 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	22 mV	1300 mV	Notes 1, 2, 4
T_{TXA}	10.625 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for system board crosstalk that is not present during measurement.

2 V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least $2x10^6$ UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 18 dB at 16 Hz, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 32.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

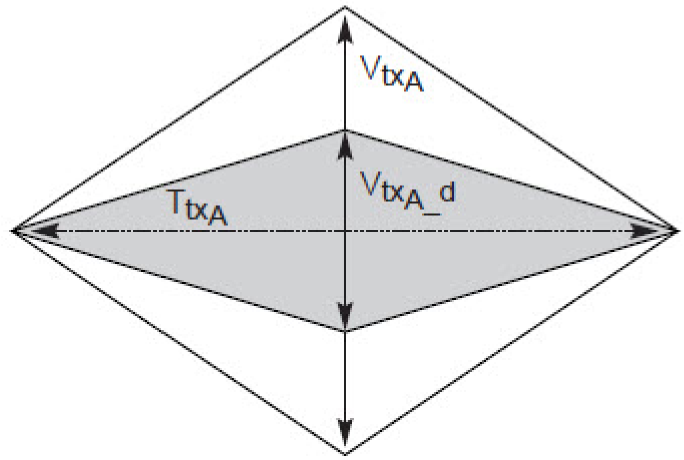


Figure 210 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 32.0 GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (non transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

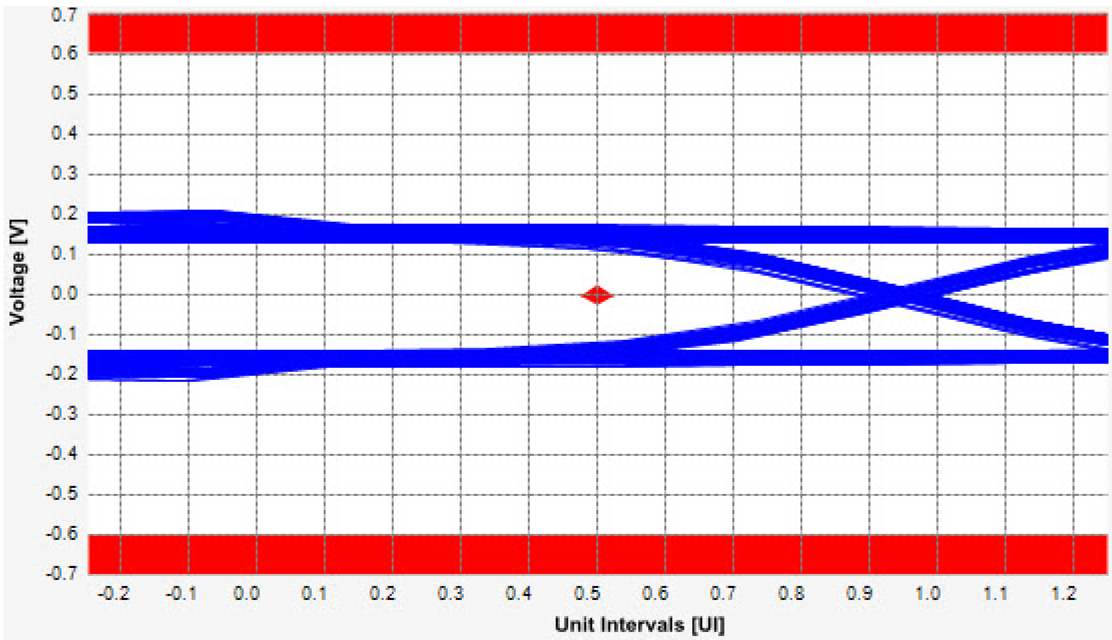


Figure 211 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.5, Table 4-16 is used as reference to check the compliance of the DUT.

Table 252 Template Test Details

Symbol	Min	Max	Comments
V_{TXA}	22 mV	1300 mV	Notes 1, 2, 4
T_{TXA}	10.625 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 A worst-case reference clock with 0.25 ps RMS jitter at the receiver of the Add-in Card is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for system board crosstalk that is not present during measurement.

2 V_{TXA} is the minimum differential peak-peak output voltage. The voltage measurements are done at a BER of 10^{-12}.

3 T_{TXA} is the minimum eye width. The sample size for this measurement is required to be at least $2x10^6$ UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXA}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 85 Ω trace with an insertion loss of 18 dB at 16 Hz, followed by a root reference package all behind a standard PCI Express connector. This channel shall be referenced as the 32.0 GT/s Add-in Card Test Channel. S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

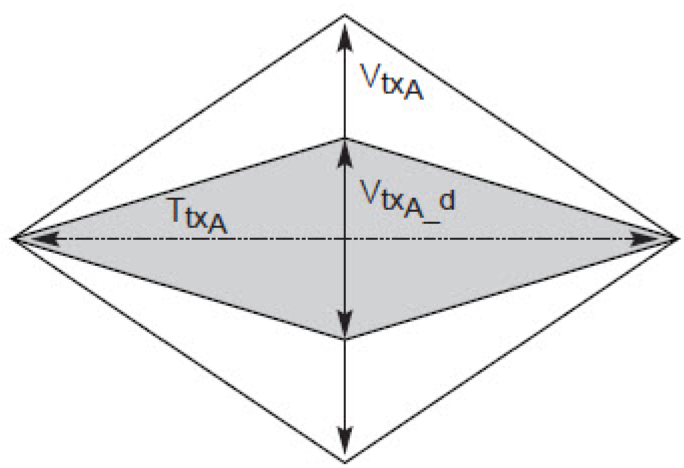


Figure 212 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE 5.0

Data Rate: 32.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The worst case recovered TX UI is reported here. The UI range is not specified for this test point. It is provided here as informative data only.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 253 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.2469 ps	31.2531

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

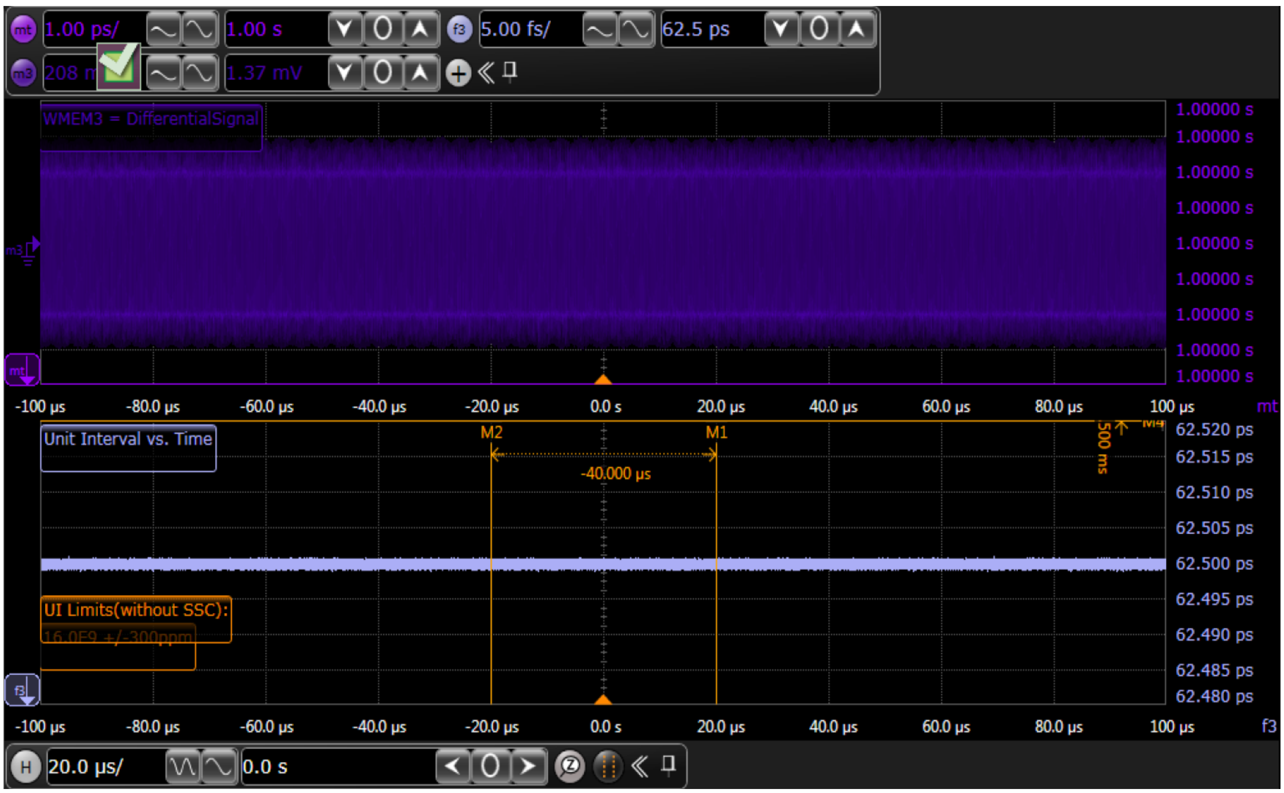


Figure 213 Reference Image for Unit Interval Test

Uncorrelated Total Pulse Width Jitter (PWJ) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.3.2, Note 11 is used as reference to check the compliance of the DUT.

Table 254 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	6.25 ps

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P10 + two toggles at lane 0.
3 Performs actual compliance testing using the SigTest tools.
  a Gets input test waveform data from scope.
  b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
  c Performs the transmitter compliance test function using the SigTest tools.
  d Gets compliance test results from SigTest tools.
  e Reports the uncorrelated total pulse width jitter value.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Pulse Width Jitter Test (32.0 GT/s)

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.3.2, Note 11 is used as reference to check the compliance of the DUT.

Table 255 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	2.5 ps

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTest tools.

a Gets input test waveform data from scope.

b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).

c Performs the transmitter compliance test function using the SigTest tools.

d Gets compliance test results from SigTest tools.

e Reports the uncorrelated deterministic DjDD PWJ value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test (32.0 GT/s)

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.3.2, Note 11 is used as reference to check the compliance of the DUT.

Table 256 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Uncorrelated total jitter	6.25 ps

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
  a Gets input test waveform data from scope.
  b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
  c Performs the transmitter compliance test function using the SigTest tools.
  d Gets compliance test results from SigTest tools.
  e Reports the uncorrelated total jitter value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test (32.0 GT/s)

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.3.2, Note 11 is used as reference to check the compliance of the DUT.

Table 257 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Uncorrelated Deterministic Jitter	3.125 ps

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the uncorrelated deterministic jitter value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

22 CEM-RootComplex Tests, 32.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe5.0 CEM-RootComplex tests using Keysight Z-Series or UXR Series Infiniium oscilloscope (13 GHz – 33 GHz), 1169A/B probes, and the PCI Express Compliance Test Application.

NOTE In case of Z-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

KEYSIGHT TECHNOLOGIES

Probing the Link for CEM-RootComplex Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of MMPX connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

   b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

NOTE

When probing and two channels are used, channel-to-channel de-skew may be required (see “Channel-to-Channel De-skew" on page 1223).

For more information on the probe amplifier and differential probe heads, see Appendix C, “InfiniiMax Probing Options,” starting on page 1231.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running CEM-RootComplex Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 32.0 GT/s Tests > CEM RootComplex Tests**.

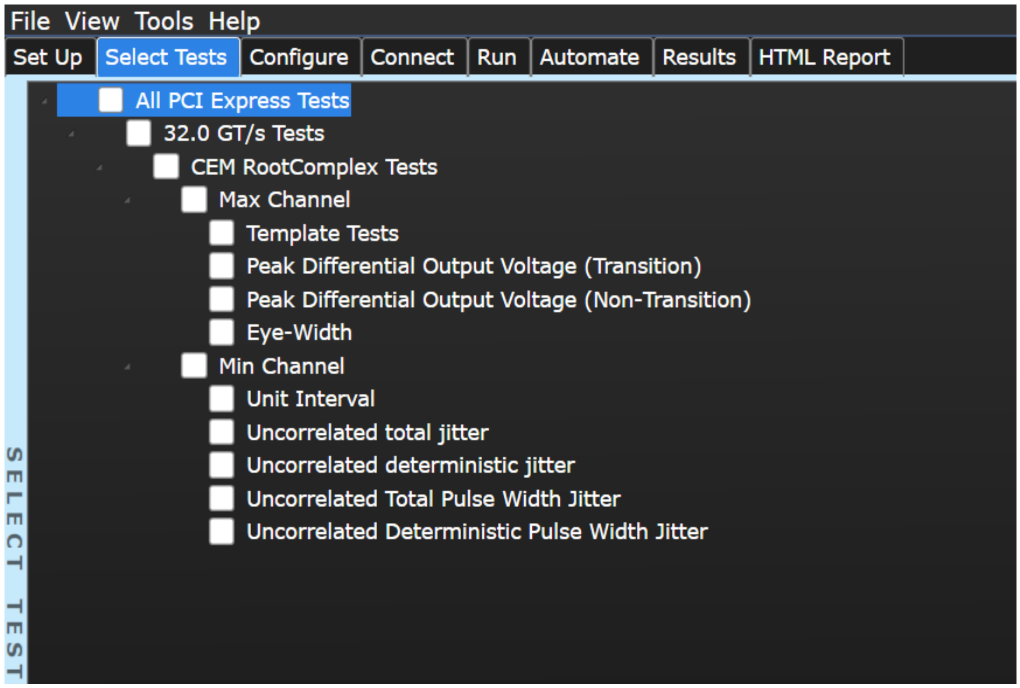


Figure 214 Selecting System Board (Tx) Tests

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window is as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

‘n’ is the index of UI in the current 3500 UI clock recovery window.

‘p’ indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 258 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.2469 ps	31.2531

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

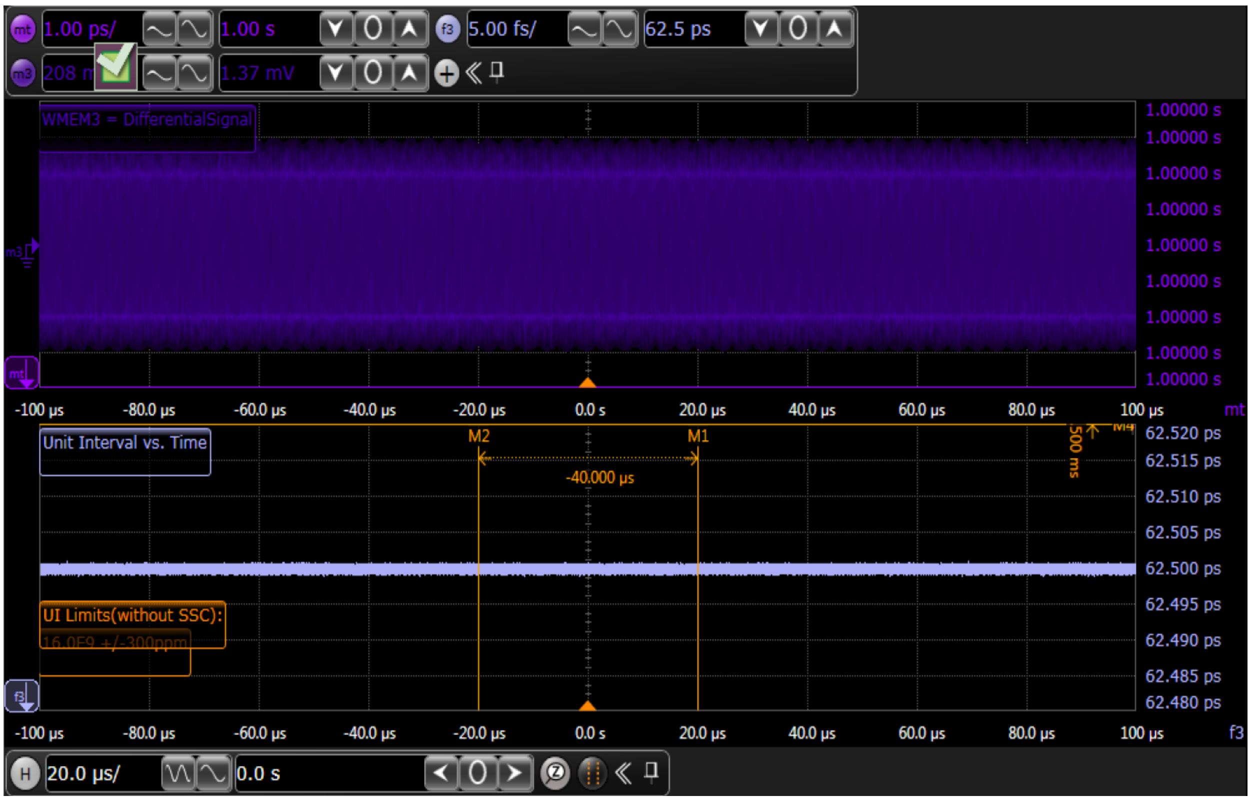


Figure 215 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 5.0, Section 4.8.17 as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Version 1.0, Section 4.8.13, Figure 4-9 is used as reference to check the compliance of the DUT.

Table 259 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	17.5 mV	1300 mV	Notes 1, 2, 4
T_{TXS}	9.688 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for Add-in Card crosstalk that is not present during measurement.

2 V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5.8 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

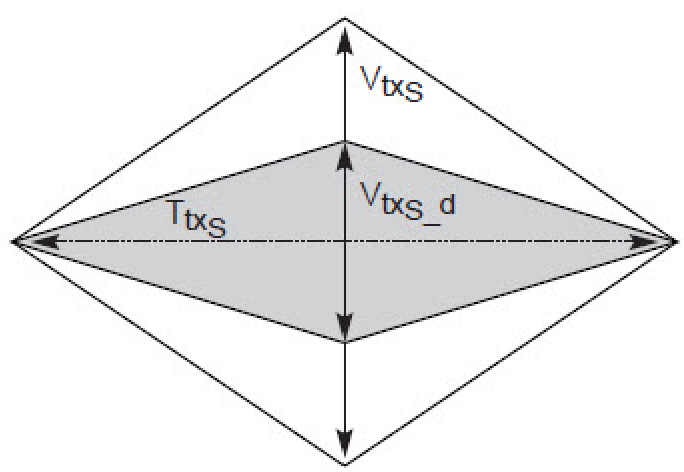


Figure 216 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

  a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

  b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 5.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

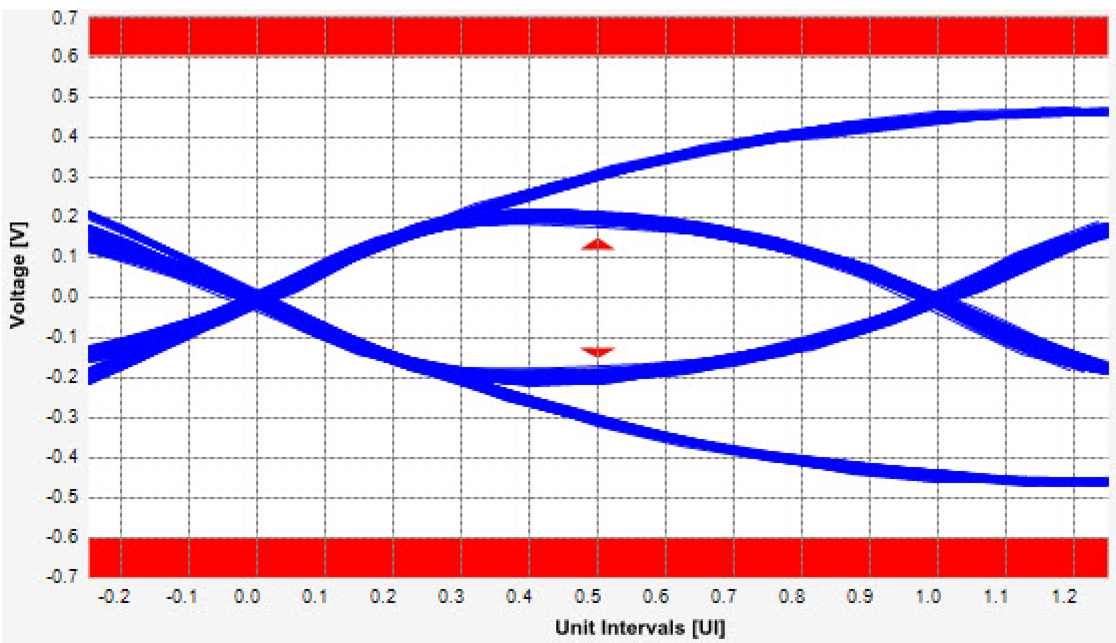


Figure 217 Reference Image for Template (Transition) Test

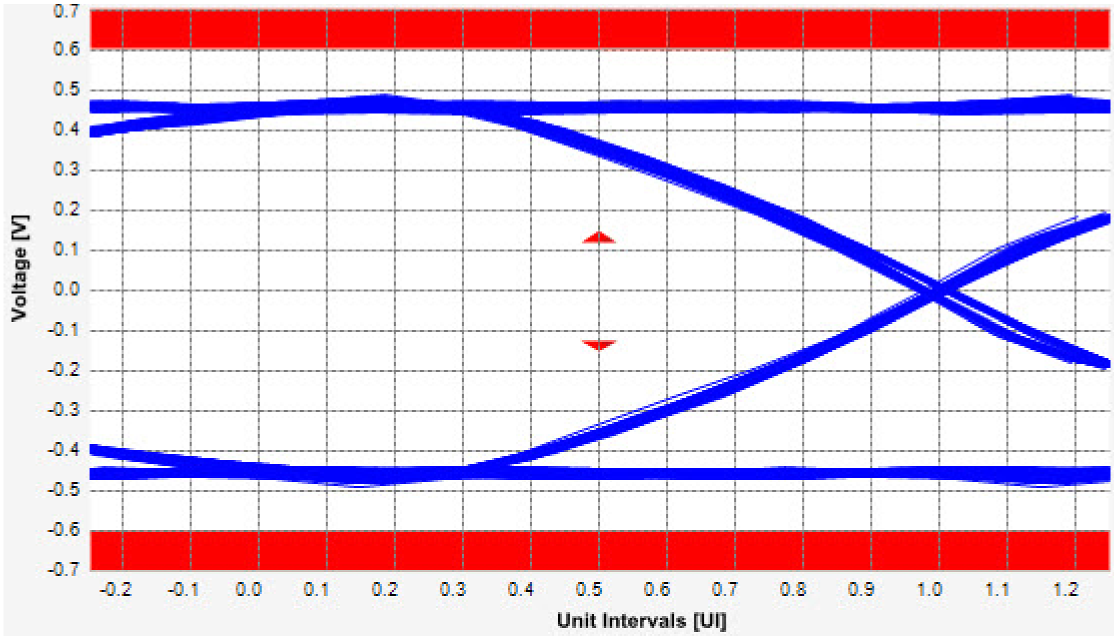


Figure 218 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test (Information Only)

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements specified in section 4.8.17 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.17, Table 4-30 is used as reference to check the compliance of the DUT.

Table 260 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	17.5 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for Add-in Card crosstalk that is not present during measurement.

2 V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5.8 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

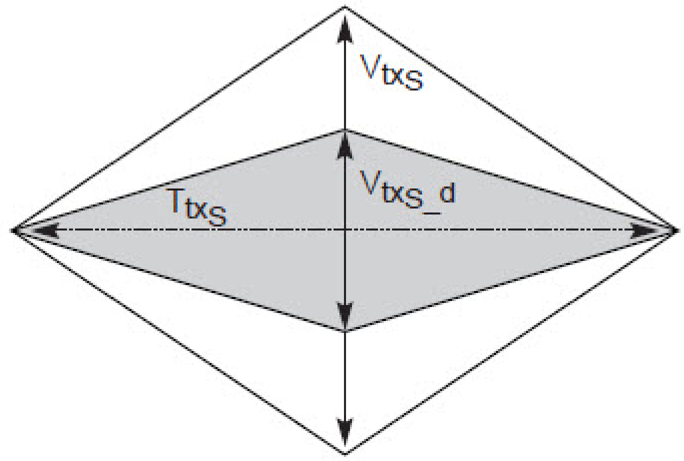


Figure 219 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:
Device: PCIE 5.0

Data Rate: 32.0 GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3 Finds the peak differential output voltage (transition) mean value from the center of UI.
4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

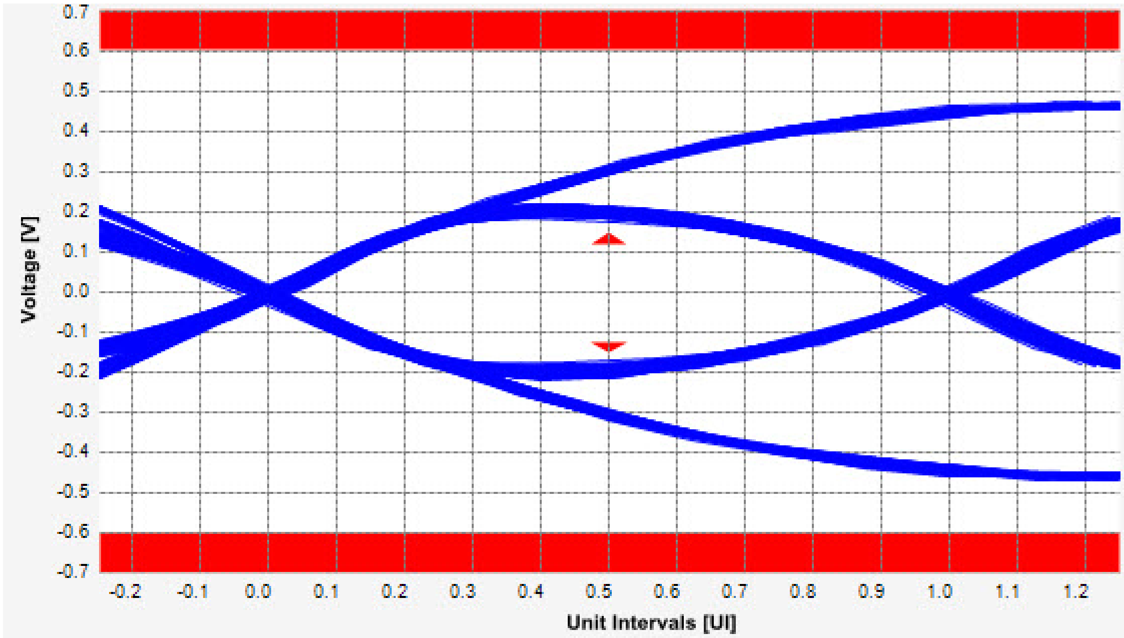


Figure 220 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test (Information Only)

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

System Board must meet the **System Board Transmitter Path Compliance Eye** requirements specified in section 4.8.17 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.17, Table 4-30 is used as reference to check the compliance of the DUT.

Table 261 Template Test Details

Symbol	Min	Max	Comments
V_{TXS}	17.5 mV	1300 mV	Notes 1, 2, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for Add-in Card crosstalk that is not present during measurement.

2 V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5.8 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

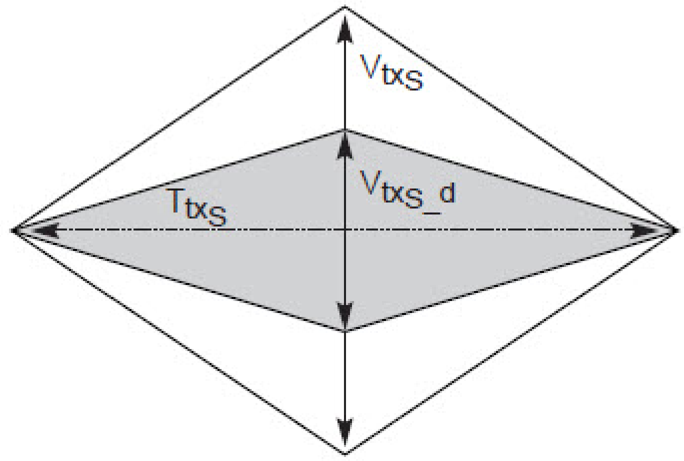


Figure 221 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> This test requires the template test with the following specifications:
> Device: PCIE 5.0
> Data Rate: 32.0 GT/s

1. Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (non transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the Online help.

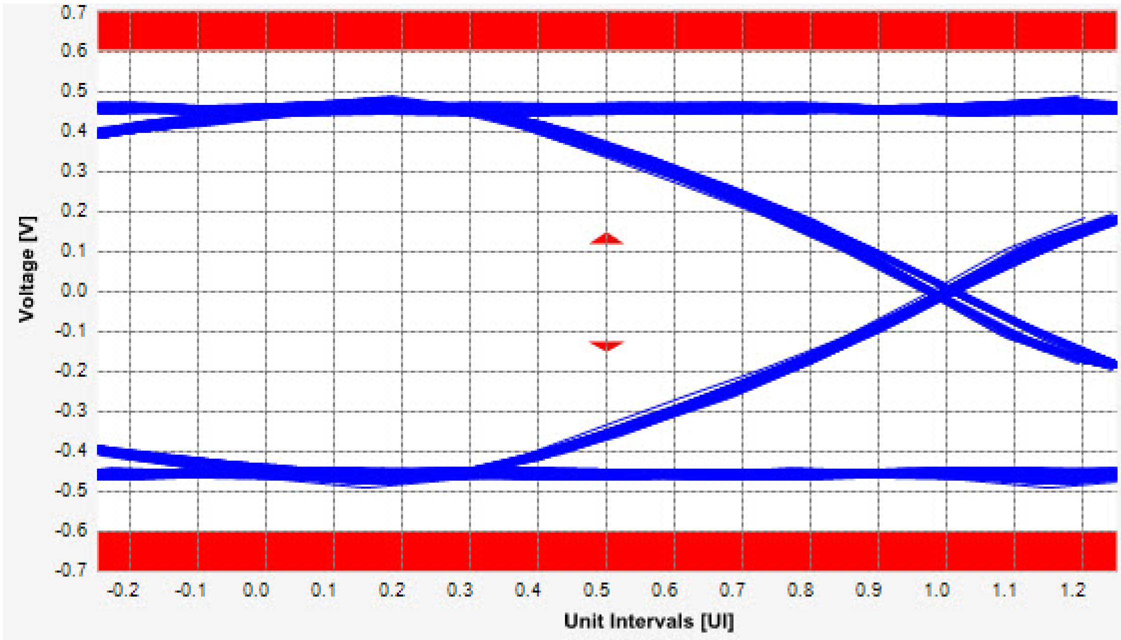


Figure 222 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test (Information Only)

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye - width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

System Board must meet the **System Board Transmitter Path Compliance Eye** Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Test Reference

PCI Express CEM Specification, Rev 5.0, Section 4.8.17, Table 4-30 is used as reference to check the compliance of the DUT.

Table 262 Template Test Details

Symbol	Min	Max	Comments
T_{TXS}	9.688 ps		Notes 1, 3, 4

Test Definition Notes from the Specification

1 All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification) is being transmitted during the test. The eye limits in this Table are different than PCIe Express Base Specification to account for Add-in Card crosstalk that is not present during measurement.

2 V_{TXS} is the minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. The sample size for this measurement is required to be at least 2 x 10^6 UI.

3 T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 2 x 10^6 UI. This calculated eye width at BER 10^{-12} must meet or exceed T_{TXS}.

4 The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 5.8 dB of 85 Ω trace, at 16.0 GHz, followed by a non-root reference package behind a standard PCI Express edge-finger. This channel shall be referenced as the 32.0 GT/s System-Board Test Channel. The S-parameter for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant Add-in Card.

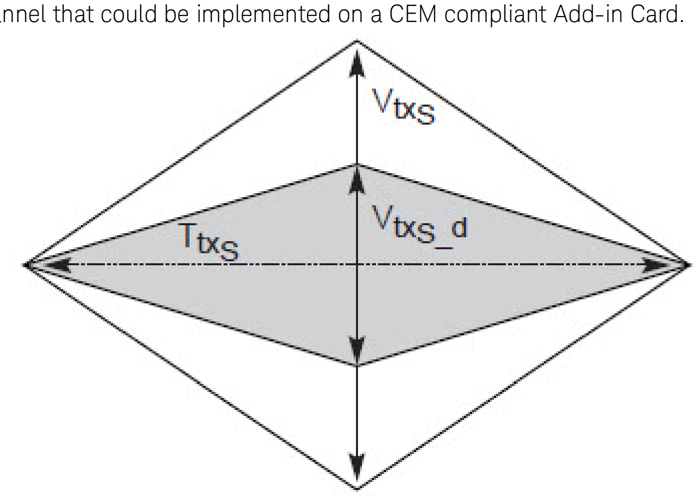


Figure 223 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
>
> This test requires the template test with the following specifications:
>
> Device: PCIE 5.0
>
> Data Rate: 32.0 GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.
2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 5.0.
3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Unit Interval Test (Information Only)

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The worst case recovered TX UI is reported here. The UI range is not specified for this test point. It is provided here as informative data only.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE **The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.**

Test Reference

This test is not required for compliance testing of the PCIe5 DUT. It is for information only.

Table 263 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.2469 ps	TBD

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

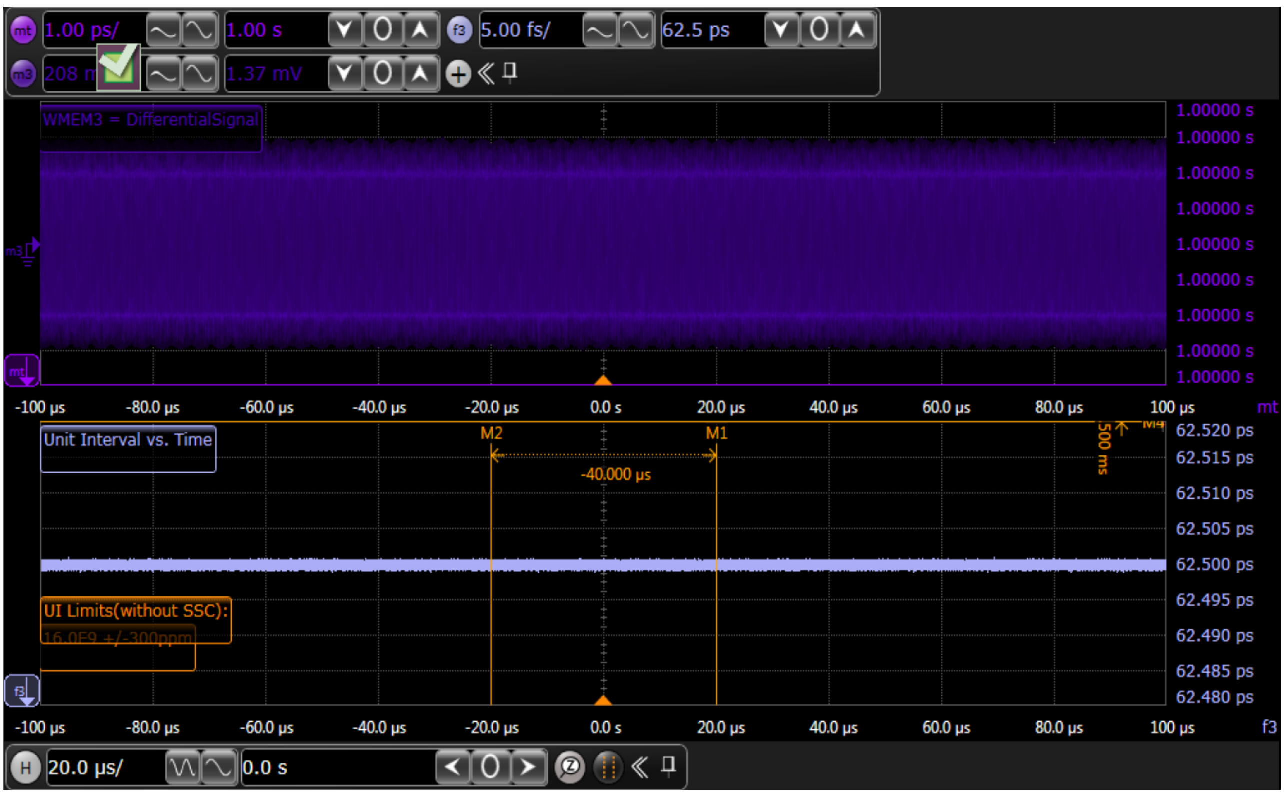


Figure 224 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test (32.0 GT/s)

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.10.2, Note 11 is used as reference to check the compliance of the DUT.

Table 264 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Uncorrelated total jitter	2.5 ps PP at BER 10^{-12}

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the uncorrelated total jitter value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test (32.0 GT/s)

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.10.2, Note 11 is used as reference to check the compliance of the DUT.

Table 265 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Uncorrelated Deterministic Jitter	3.125 ps

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the uncorrelated deterministic jitter value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.10.2, Note 11 is used as reference to check the compliance of the DUT.

Table 266 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	6.25 ps PP at BER 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P10 + two toggles at lane0.
3 Performs actual compliance testing using the SigTest tools.
   a Gets input test waveform data from scope.
   b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
   c Performs the transmitter compliance test function using the SigTest tools.
   d Gets compliance test results from SigTest tools.
   e Reports the total uncorrelated pulse width jitter value.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Pulse Width Jitter Test (32.0 GT/s)

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Architecture PHY Specification, Rev 5.0, Version 0.9, Section 2.10.2, Note 11 is used as reference to check the compliance of the DUT.

Table 267 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	2.5 ps PP at BER 10^{-12}

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.7 of the PCI Express Card Electromechanical Specification (CEM) Rev 5.0, as measured at the card edge-fingers.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
  a Gets input test waveform data from scope.
  b Acquires scope sample waveform data (re-iterate to capture at least 2M UI).
  c Performs the transmitter compliance test function using the SigTest tools.
  d Gets compliance test results from SigTest tools.
  e Reports the uncorrelated deterministic DjDD PWJ value.
3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

23 Reference Clock Tests, 32.0 GT/s, PCI-E 5.0

This section provides the Methods of Implementation (MOIs) for PCIe 5.0 Reference Clock tests at 32.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application

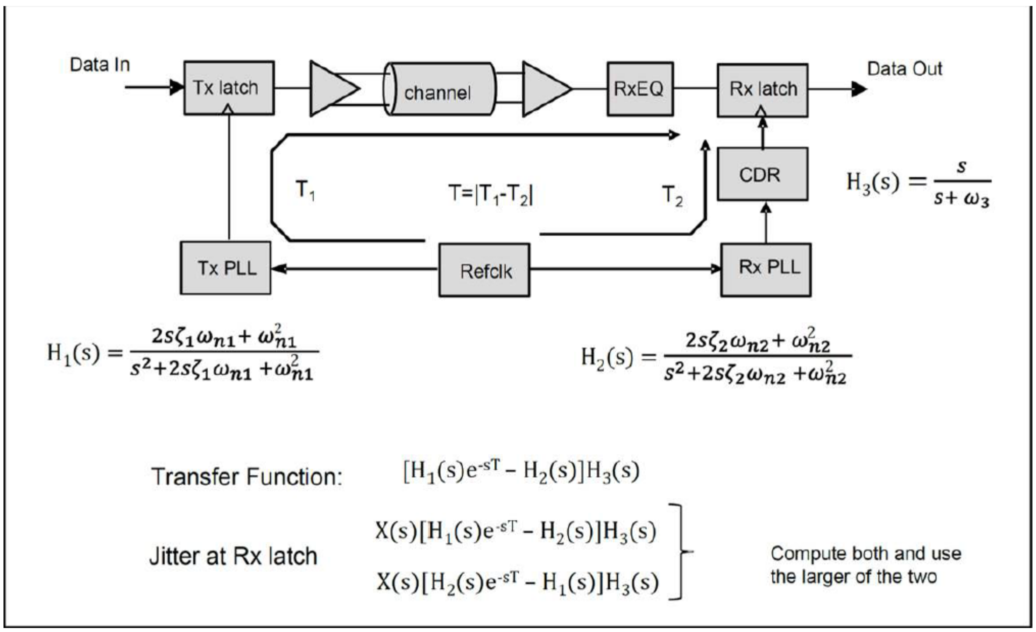
NOTE In case of Z-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

Reference Clock Architectures

For 32.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.
At 32.0 GT/s the only difference in the figure is the "behavioral CDR transfer function" as defined in PCI Express Base Specification, Rev 5.0, Section 8.3.5.5.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order		64 combinations			8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC	**CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

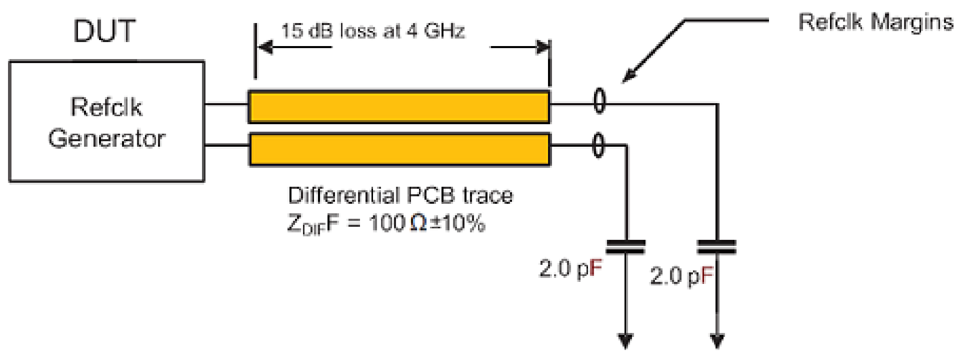


Figure 225 Driver Compliance Test Load

At 32.0 GT/s reference clock jitter is tested with the reference clock terminated directly by 50 Ohm terminations without a channel as mentioned in PCI Express Base Specification, Rev 5.0, Section 8.6.1.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 32.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

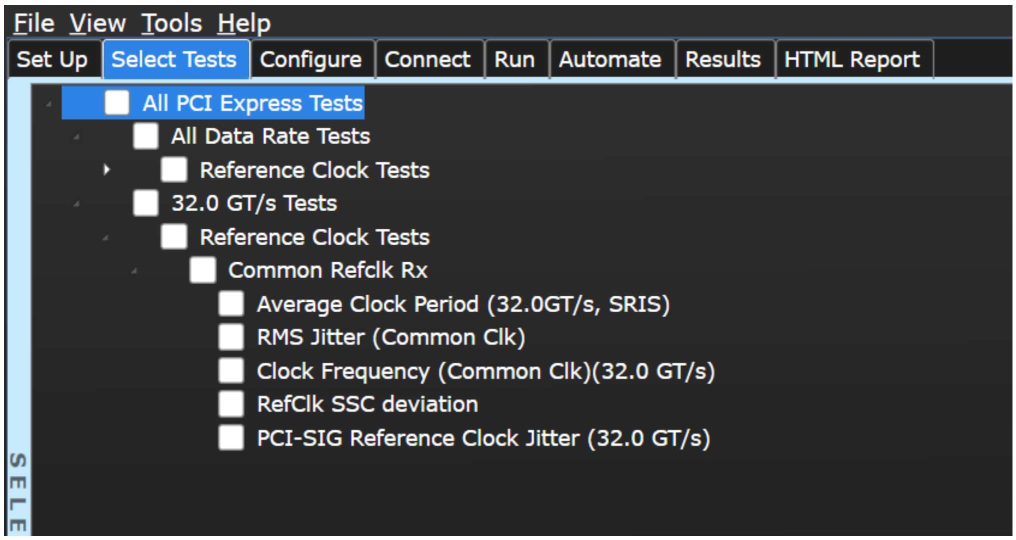


Figure 226 Selecting Reference Clock Tests when SSC or Clean Clock is Selected with SRIS Mode

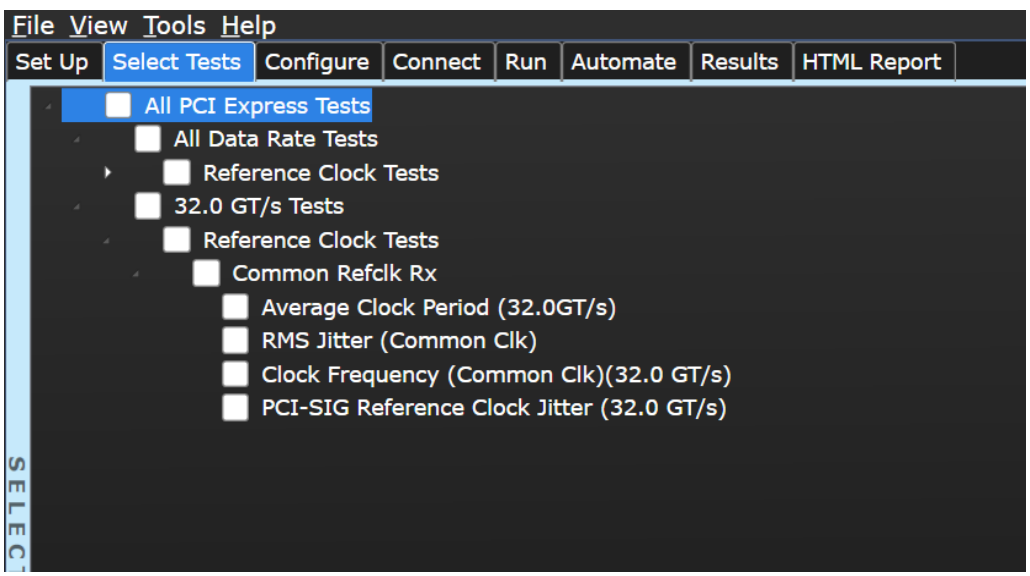


Figure 227 Selecting Reference Clock Tests when SSC or Clean Clock is Selected without SRIS Mode

Average Clock Period Test (32.0 GT/s)

This test verifies that the Refclk Average Clock Period (32 GT/s) is within the conformance limits as specified in PCIE Express Base Specification, Revision 5.0, Section 8.6.2, Table 8-16.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC, there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 32.0GT/s speed.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 (REFCLK DC Specifications and AC Timing Requirements) is used as reference to check the compliance of the DUT.

Table 268 Average Clock Period Test Details

		100 MHz Input	
Symbol	Parameter	Min	Max
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	+2800 ppm
$T_{PERIOD\ AVG\_32G\_CC}$	Average Clock Period Accuracy for devices that support 32.0 GT/s in CC Mode at any speed	-100 ppm	+2600 ppm
$T_{PERIOD\ AVG\_32G\_SRIS}$	Average Clock Period Accuracy for devices that support 32.0 GT/s in SRIS Mode at any speed	-100 ppm	+1600 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Configures memory depth and sampling rate as per the data rate.
4 Fits and displays all sample data on screen.
5 Measures the average voltage using **V average** measurement.
6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7 Measures the average frequency using **Frequency** measurement of **Clock**.
8 Measures the average period using **Period** measurement of **Clock**.
9 Computes the difference between ideal and actual frequency in terms of parts per million of 100 MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 5.0.

For SSC Mode,

-300 ppm ≤ Average Clock Period Accuracy ≤ +2800 ppm

For Clean Clock,

-100 ppm ≤ Average Clock Period Accuracy ≤ +2600 ppm

For SRIS Mode,

-100 ppm ≤ Average Clock Period Accuracy ≤ +1600 ppm

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

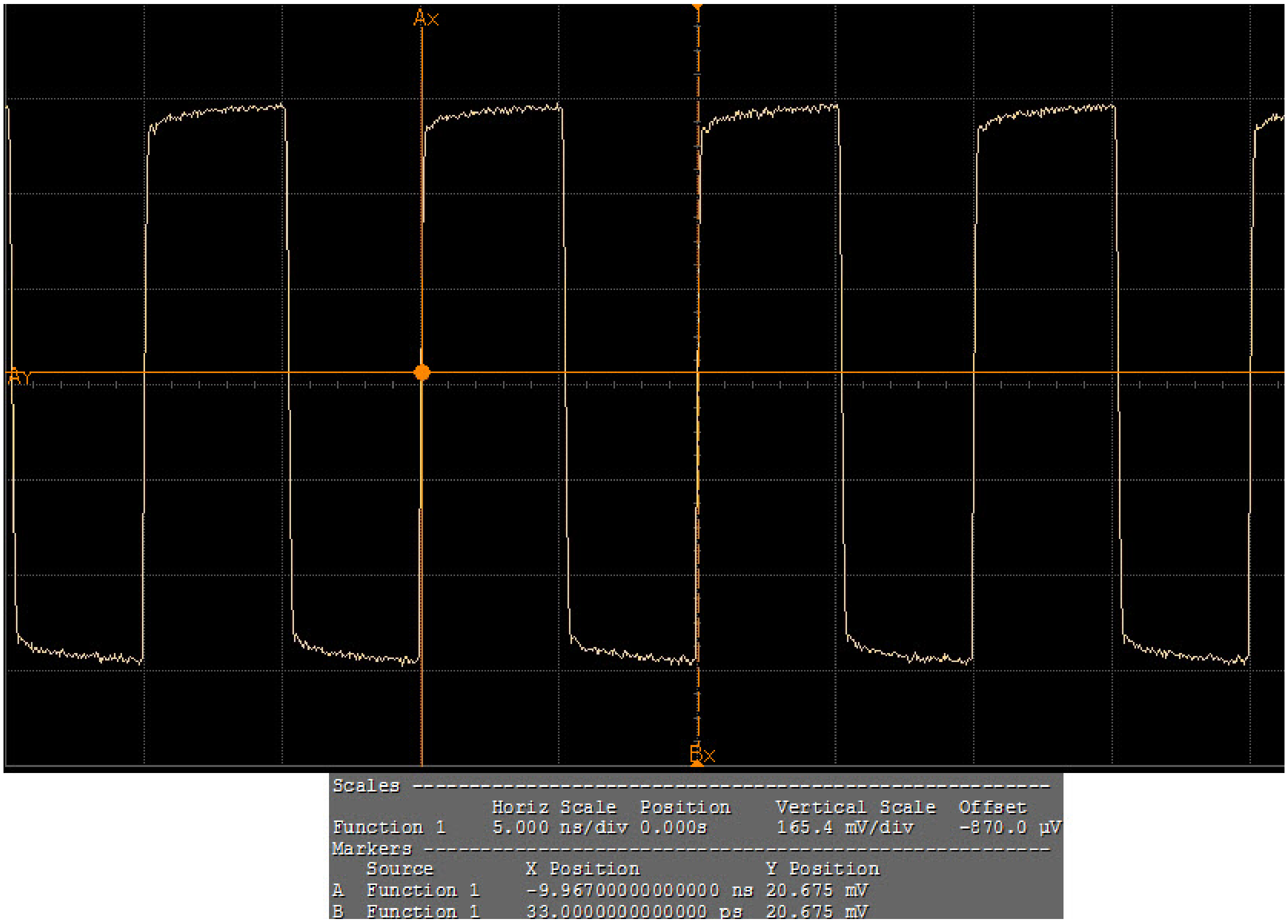


Figure 228 Reference Image for Average Clock Period

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 269 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.5 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.
10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.
11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

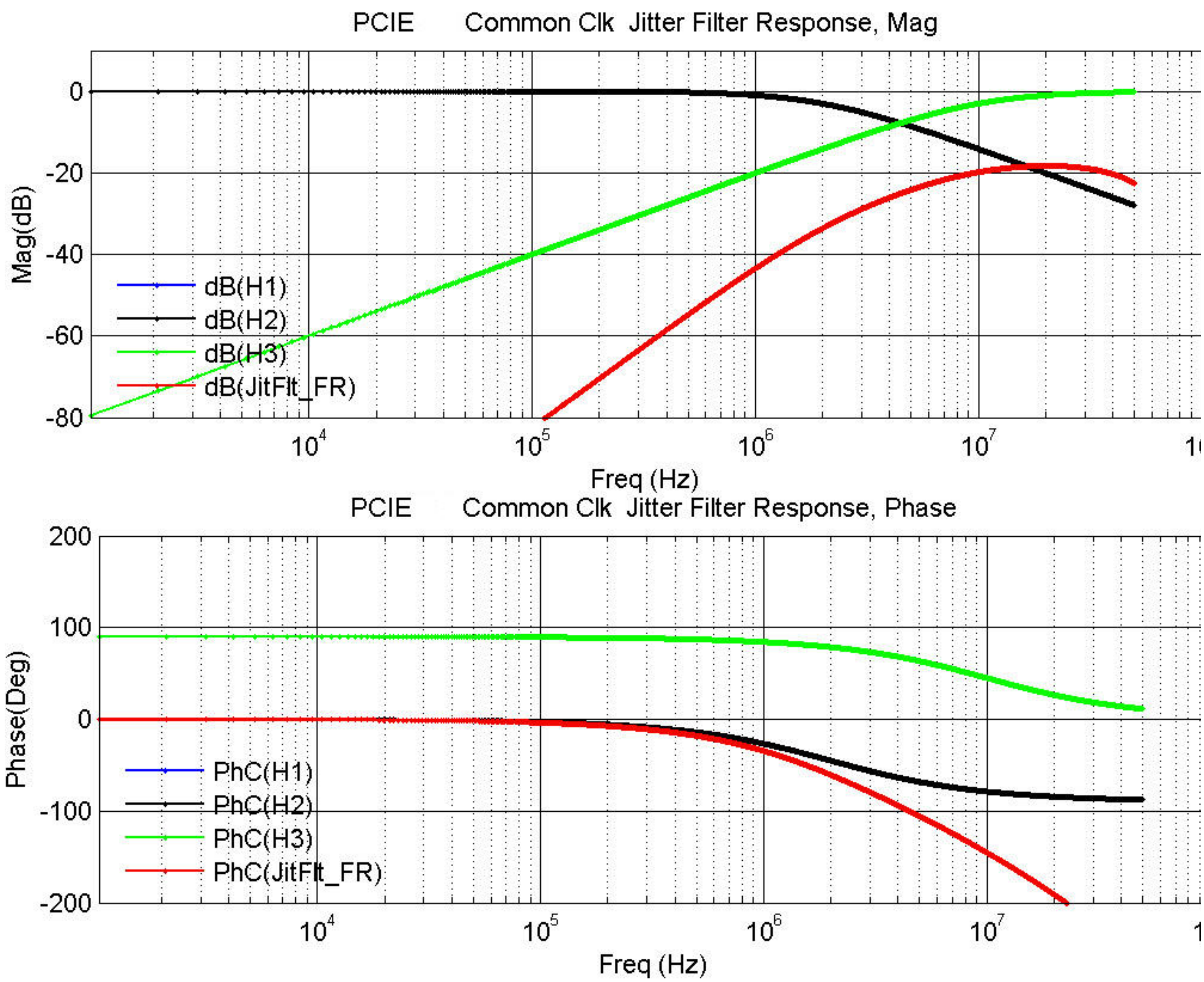


Figure 229 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

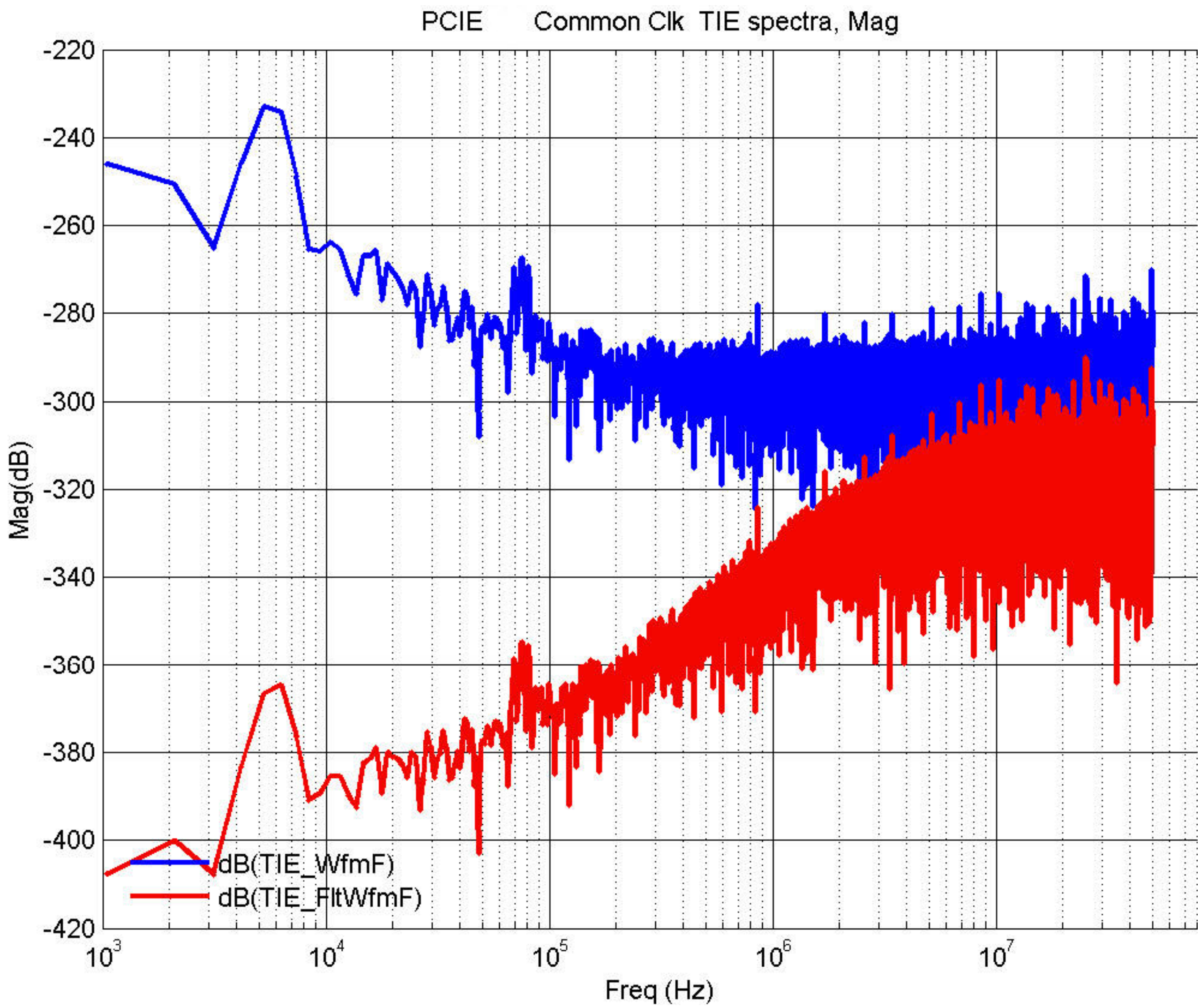


Figure 230 Reference Image for Common Clock TIE Spectra RMS Jitter Test

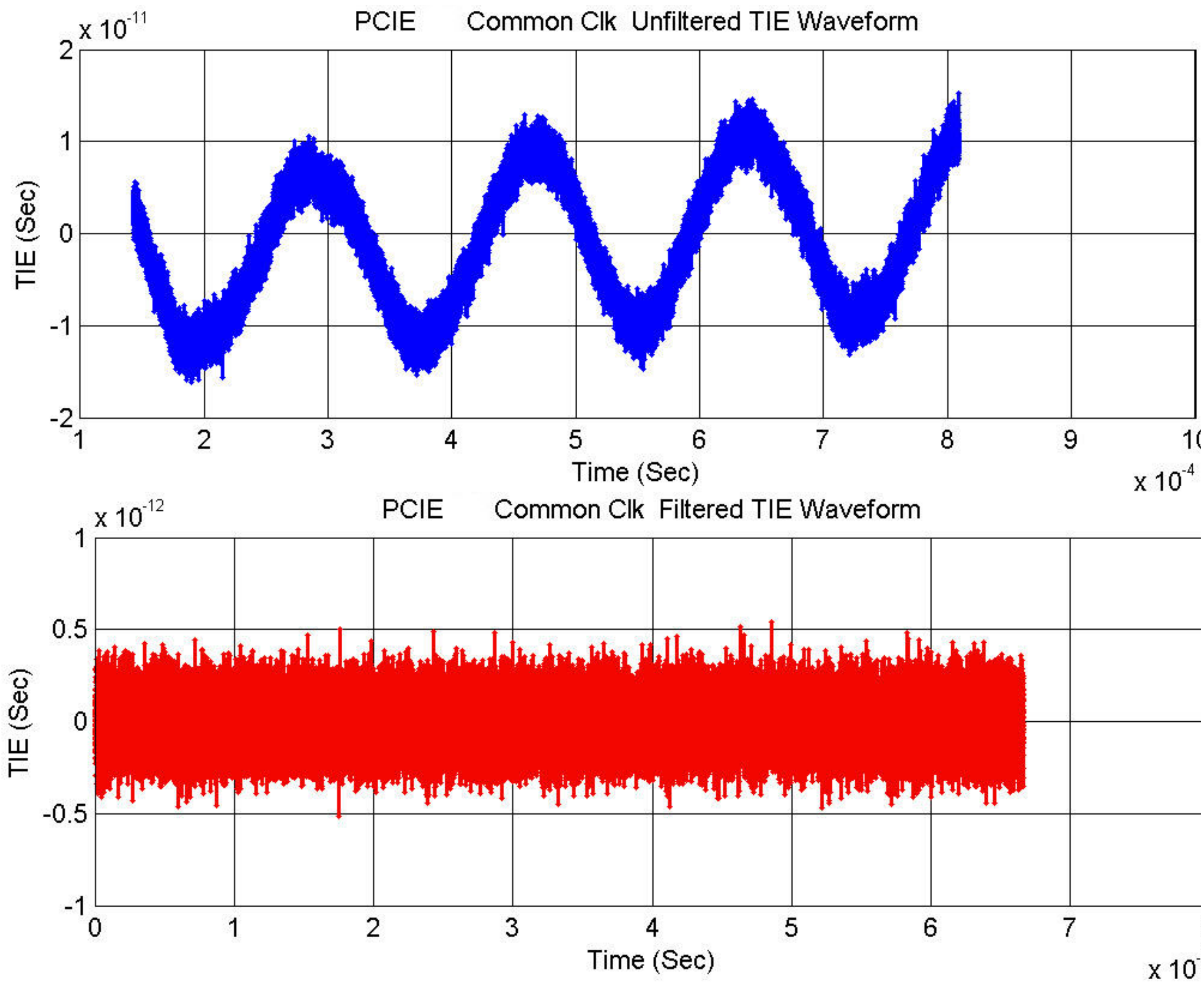


Figure 231 Reference Image for TIE Waveform RMS Jitter Test

Clock Frequency (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in the PCIE Base Specification.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.3, Table 8-17 is used as reference to check the compliance of the DUT.

Table 270 RMS Jitter Test Details

Symbol	Description	Min	Max
$T_{REFCLK-RMS-CC}$	Ref Clock Frequency (Common Clk)	99.99 MHz	100.01 MHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 639 and select **Clock Frequency (Common Clk) (Data Clk).**

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Sets the time scale to 5 ns.
5 Fits and displays all sample data on the screen.
6 Enables jitter analysis so that measurements are made on all edges.
7 Measures the clock frequency.
8 Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

PCI-SIG Reference Clock Jitter

This test measures PCI-SIG Reference Clock Jitter for PCIe 5.0 using Intel Clock Jitter Tool.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the PCI-SIG reference clock jitter.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures **Low Pass Filter**, **SSC Removal**, and **Noise Floor Deembed** option in the Clock Jitter Tool.
3 Performs compliance testing using the Clock Jitter Tool.
4 Captures the Noise Floor Signal if **Noise Floor Deembed** option is enabled.
5 Identifies overall test status.
6 Reports the overall test status, maximum phase jitter value, limits, and settings.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part VIII
PCI-Express Gen6 All GT/s Tests

24 Reference Clock Tests, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests, common to all data rates, using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE In case of Z-series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 6.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

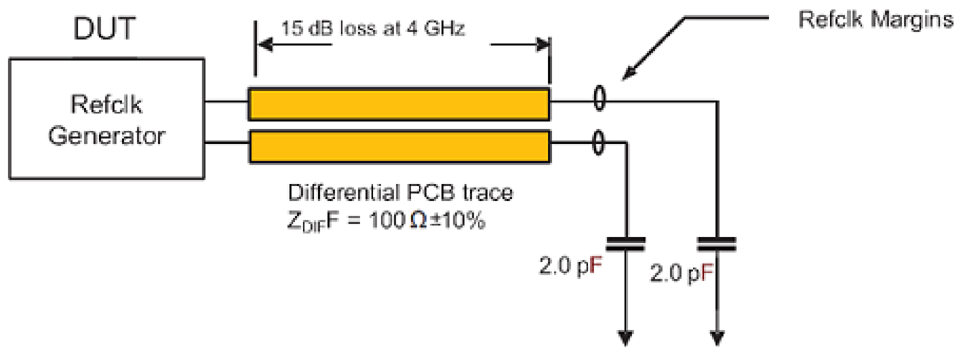


Figure 1 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > All Data Rate Tests > Reference Clock Tests**.

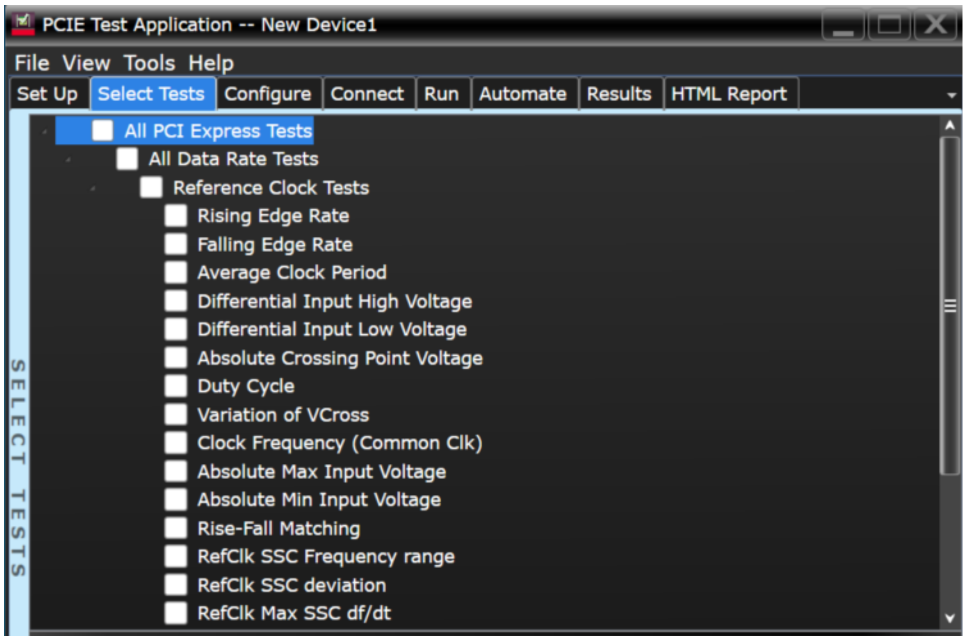


Figure 2 Selecting Reference Clock Tests

Rising Edge Rate Test

The rising edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for rise time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Rise Edge Rate	Rising Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 8-69.

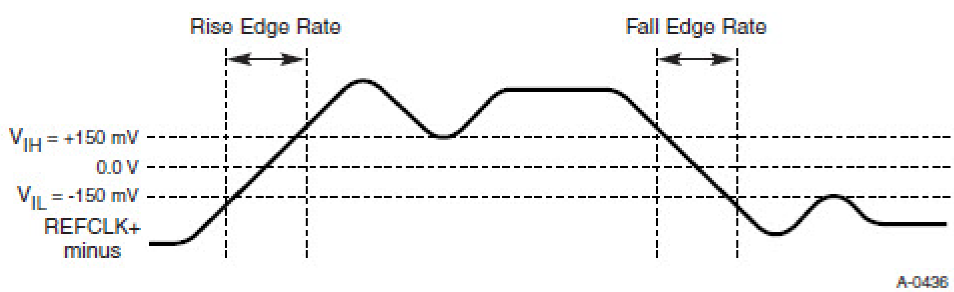


Figure 3 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the maximum rise time using **Rise time** measurement.
6 Zoom to maximum value of rise time.
7 Converts the maximum rise time to units of V/ns as given in the PCIE spec. [0.0000000003 / Maximum Rise Time value].
8 Reports the rising edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as 0.6 V/ns ≥ Rising Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

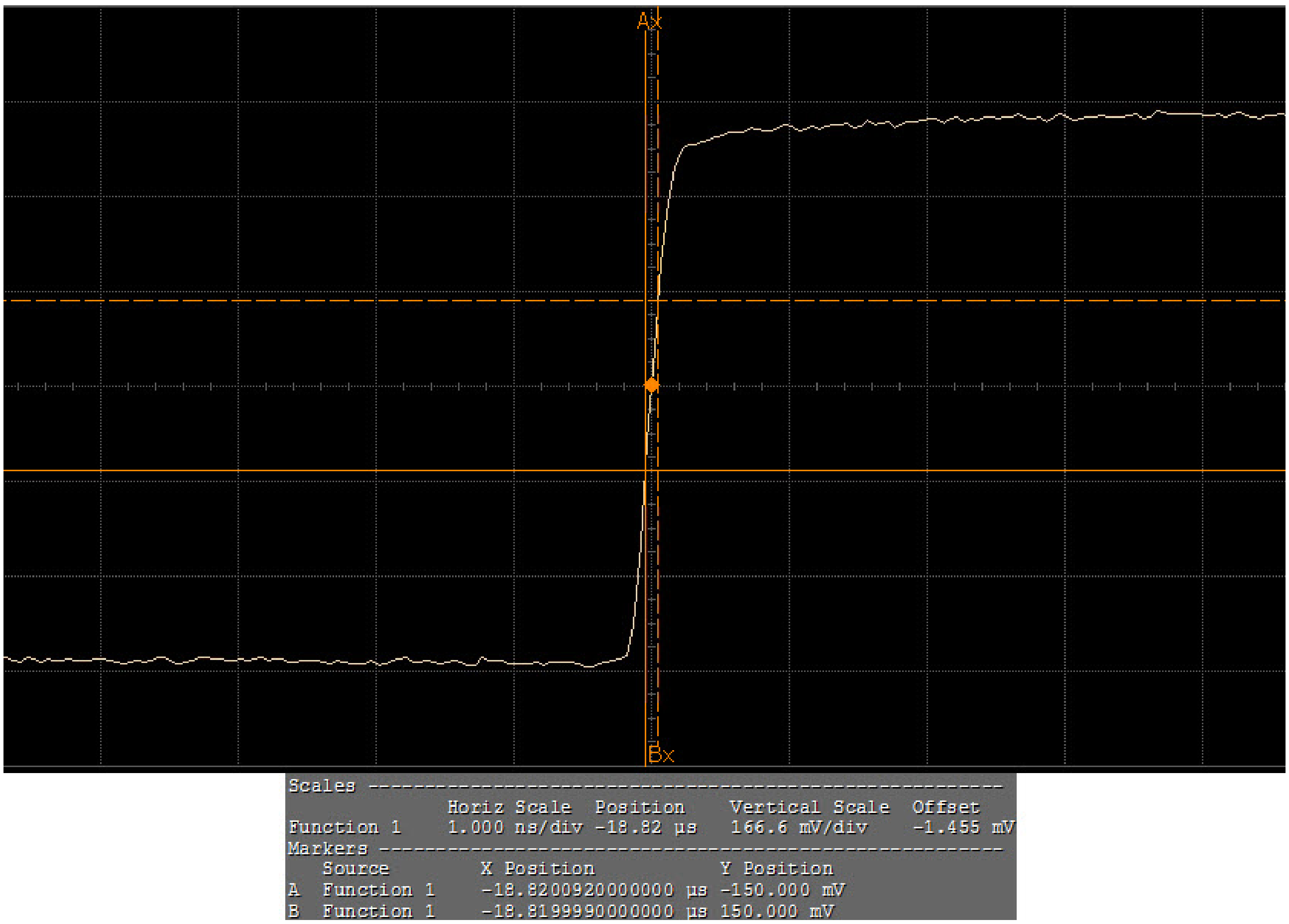


Figure 4 Reference Image for Rising Edge Rate

Falling Edge Rate Test

The falling edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for fall time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Fall Edge Rate	Falling Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See, Figure 8-69.

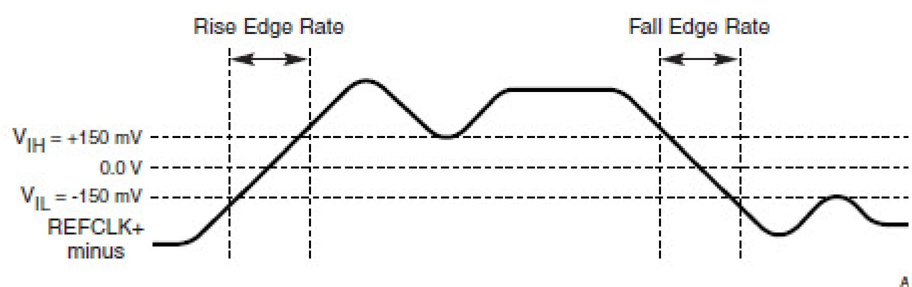


Figure 5 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5. Measures the maximum fall time using **Fall time** measurement.
6. Zoom the resultant waveform to maximum value of fall time.
7. Converts the maximum fall time to units of V/ns as given in the PCIE specification [0.0000000003 / Maximum Fall Time value].
8. Reports the falling edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as 0.6 V/ns ≤ Falling Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

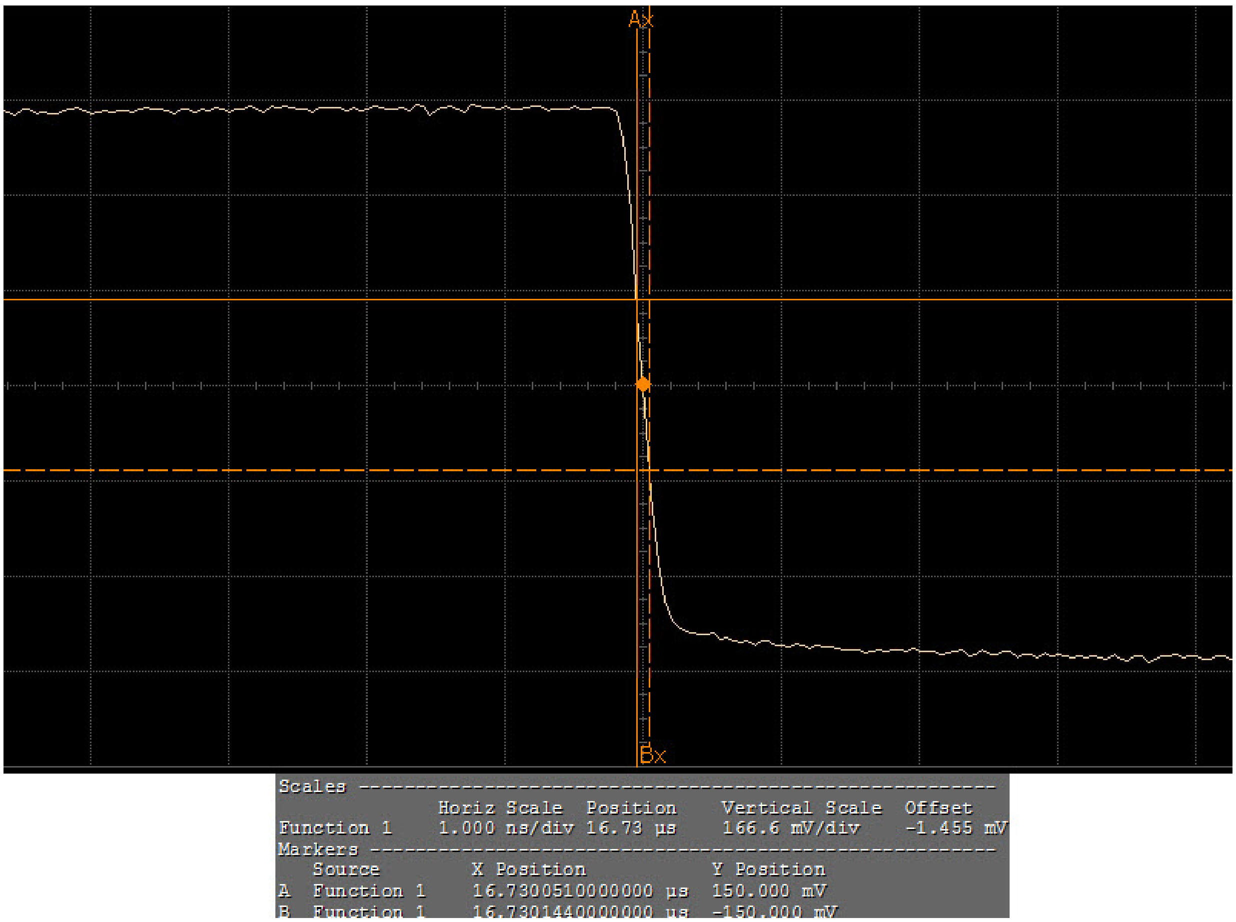


Figure 6 Reference Image for Falling Edge Rate

Average Clock Period Test

This test verifies that the Refclk Average Clock Period is within the conformance limits as specified in PCIE Express Base Specification.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2800 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Configures memory depth and sampling rate as per the data rate.
4. Fits and displays all sample data on screen.
5. Measures the average voltage using **V average** measurement.
6. Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7. Measures the average frequency using **Frequency** measurement of **Clock**.
8. Measures the average period using **Period** measurement of **Clock**.
9. Computes the difference between ideal and actual frequency in terms of parts per million of 100MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency] / 100$$

10. Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

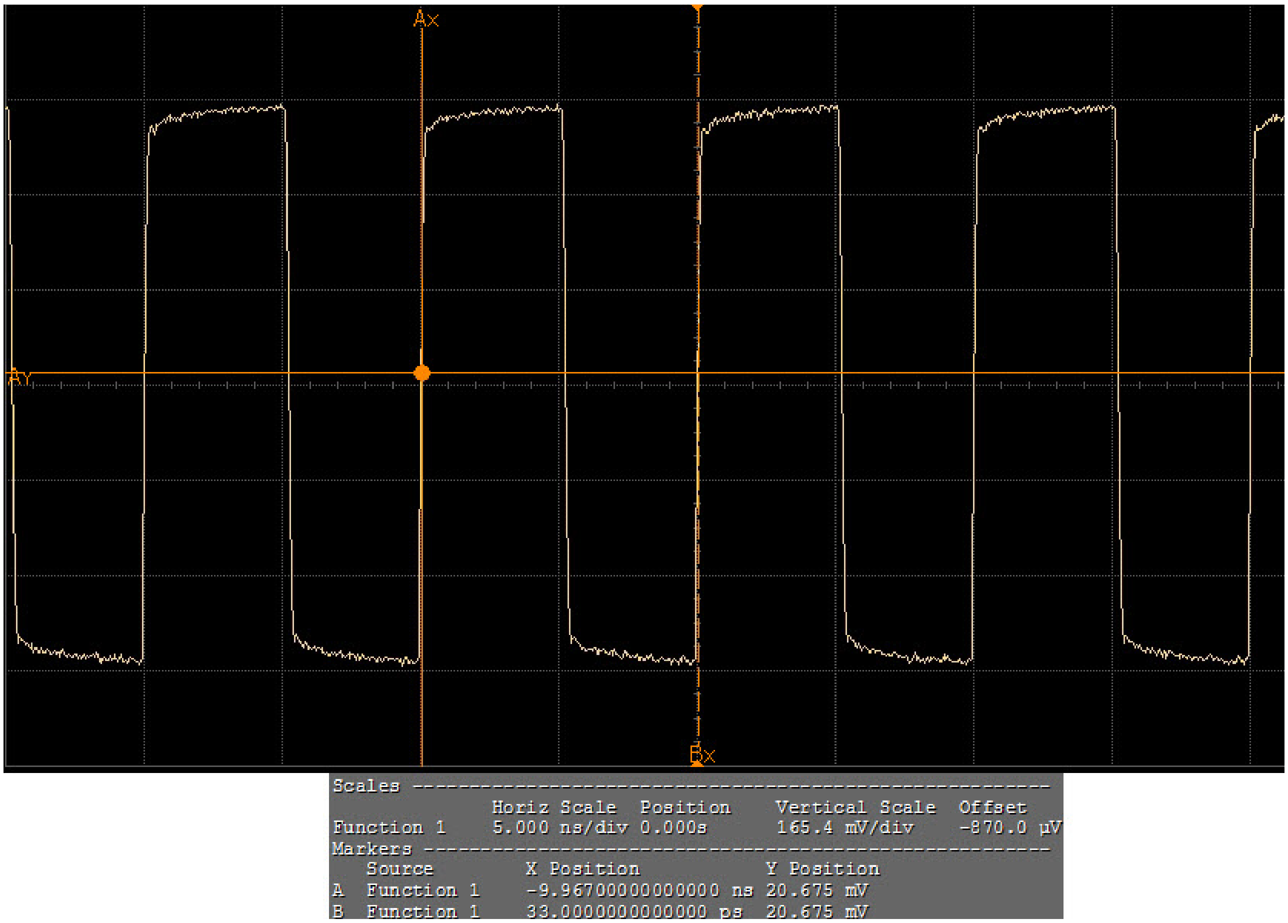


Figure 7 Reference Image for Average Clock Period

Differential Input High Voltage Test

The differential input high voltage test verifies that the reference clock differential input high voltage is within the conformance limits specified in PCI Express Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)
V_{IH}	Differential Input High Voltage	150 mV

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the maximum voltage using **V max** measurement.
6 Reports the maximum voltage value as differential input high voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as V_{IH} > 150 mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

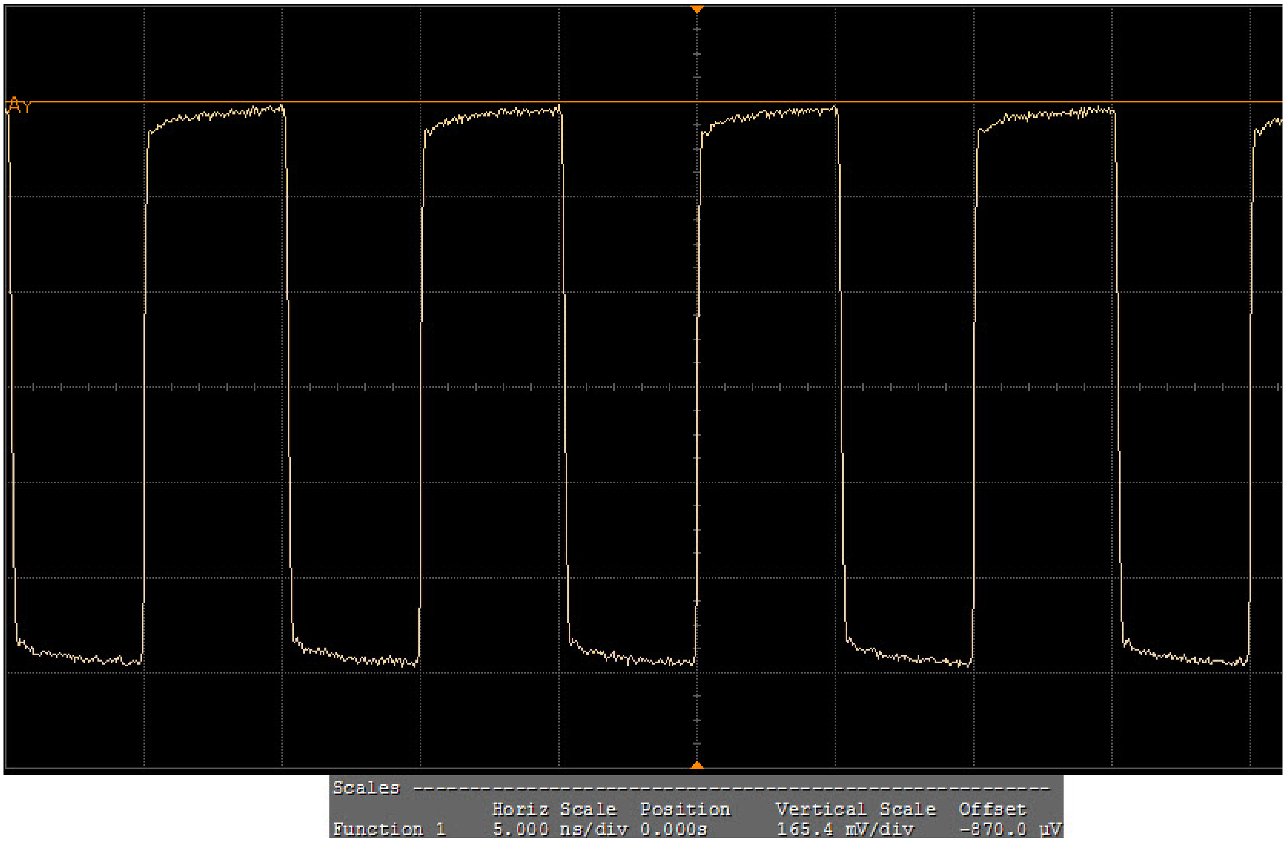


Figure 8 Reference Image for Differential Input High Voltage Test

Differential Input Low Voltage Test

The differential input low voltage test verifies that the reference clock differential input low voltage is within the conformance limits specified in PCI Express Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{IL}	Differential Input High Voltage	-150 mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Fits and displays all sample data on screen.
4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5 Measures the minimum voltage using **V min** measurement.
6 Reports the minimum voltage value as differential input low voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCIE Base Specification as V_{IL} < –150 mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

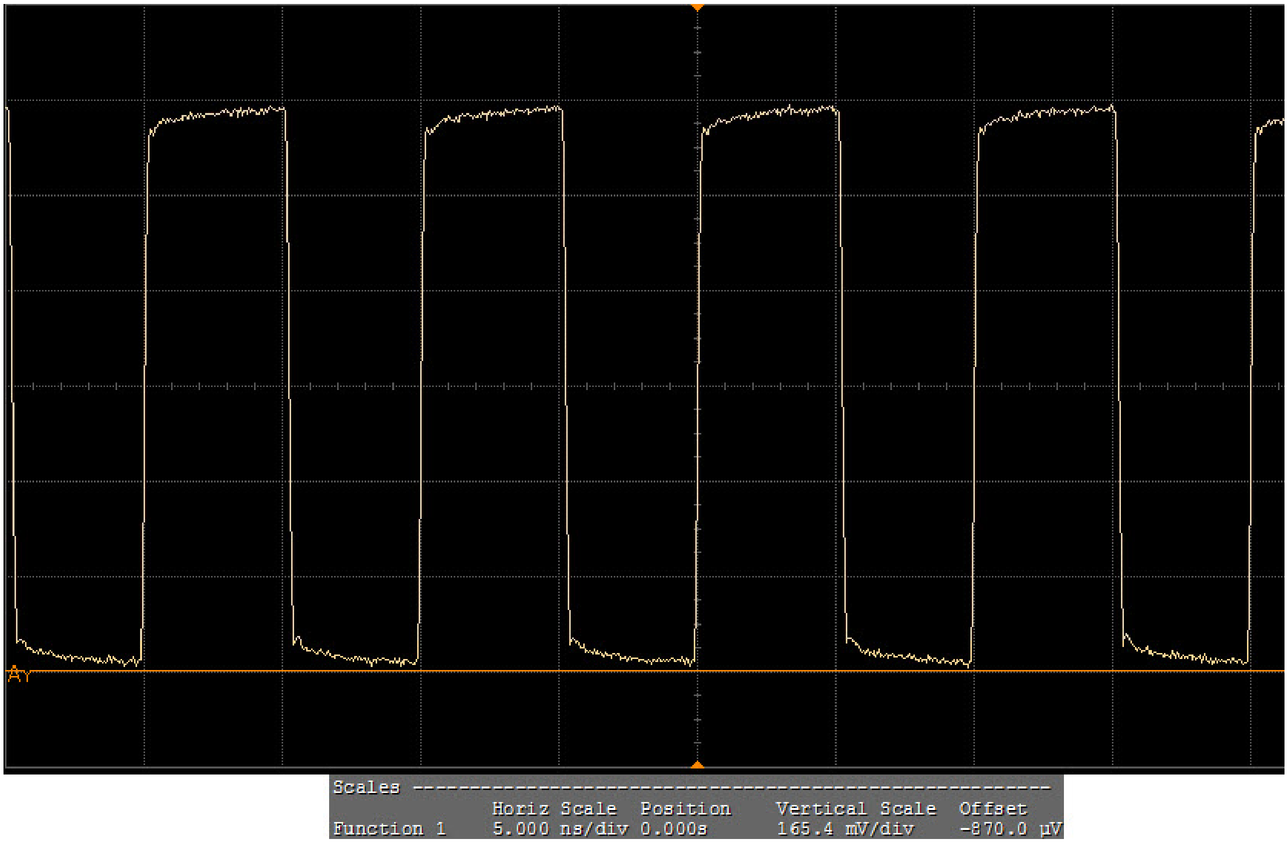


Figure 9 Reference Image for Differential Input Low Voltage Test

Absolute Crossing Point Voltage Test

The absolute crossing point voltage test is measured at crossing point where the instantaneous voltage value of the rising edge of RefClk+ equals the falling edge of RefClk-. It refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

Table 1 Absolute Crossing Point Voltage Test Details

Symbol	Parameter	Min(at 100 MHz Input)	Max (at 100 MHz Input)
V_{CROSS}	Absolute Crossing Point Voltage	+250 mV	+550 mV

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 8-65.

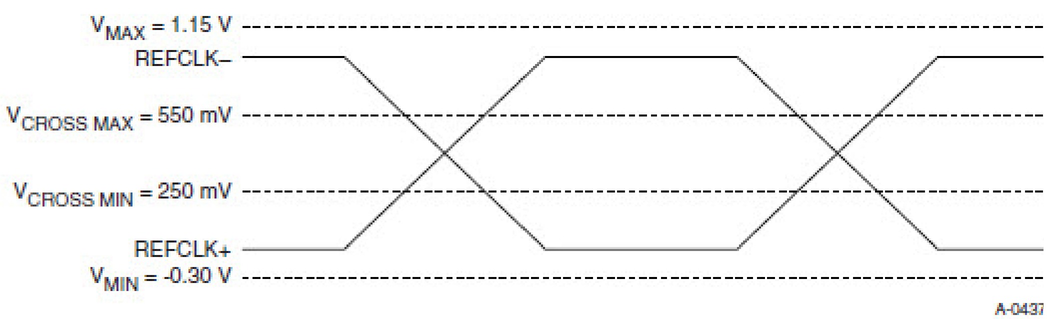


Figure 10 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.9 or 4.2.11 of the PCI Express Base Specification Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Uses MATLAB function to find the absolute crossing point voltage. The MATLAB function does the following:
   a Finds crossing edges for rising and falling edges.
   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.
4 Computes the margin for minimum crossing point voltage and margin of maximum crossing point voltage.
5 Compares the margin and choose the smallest margin to report the value (worst value) as absolute crossing point voltage.
6 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as 250mV ≤ Absolute Crossing Point Voltage ≤ 550mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Duty Cycle Test

The duty cycle test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Duty Cycle	Duty Cycle	40%	60%

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Configures memory depth and sampling rate as per the data rate.
4. Fits and displays all sample data on screen.
5. Measures the average voltage using **V average** measurement.
6. Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7. Measures the duty cycle using the **Duty cycle** measurement.
8. Finds the margin for maximum duty cycle and minimum duty cycle.
9. Compares the margin and choose the largest margin to report the value (worst value) as duty cycle.
10. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as 40% ≤ Duty Cycle ≤ 60%.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

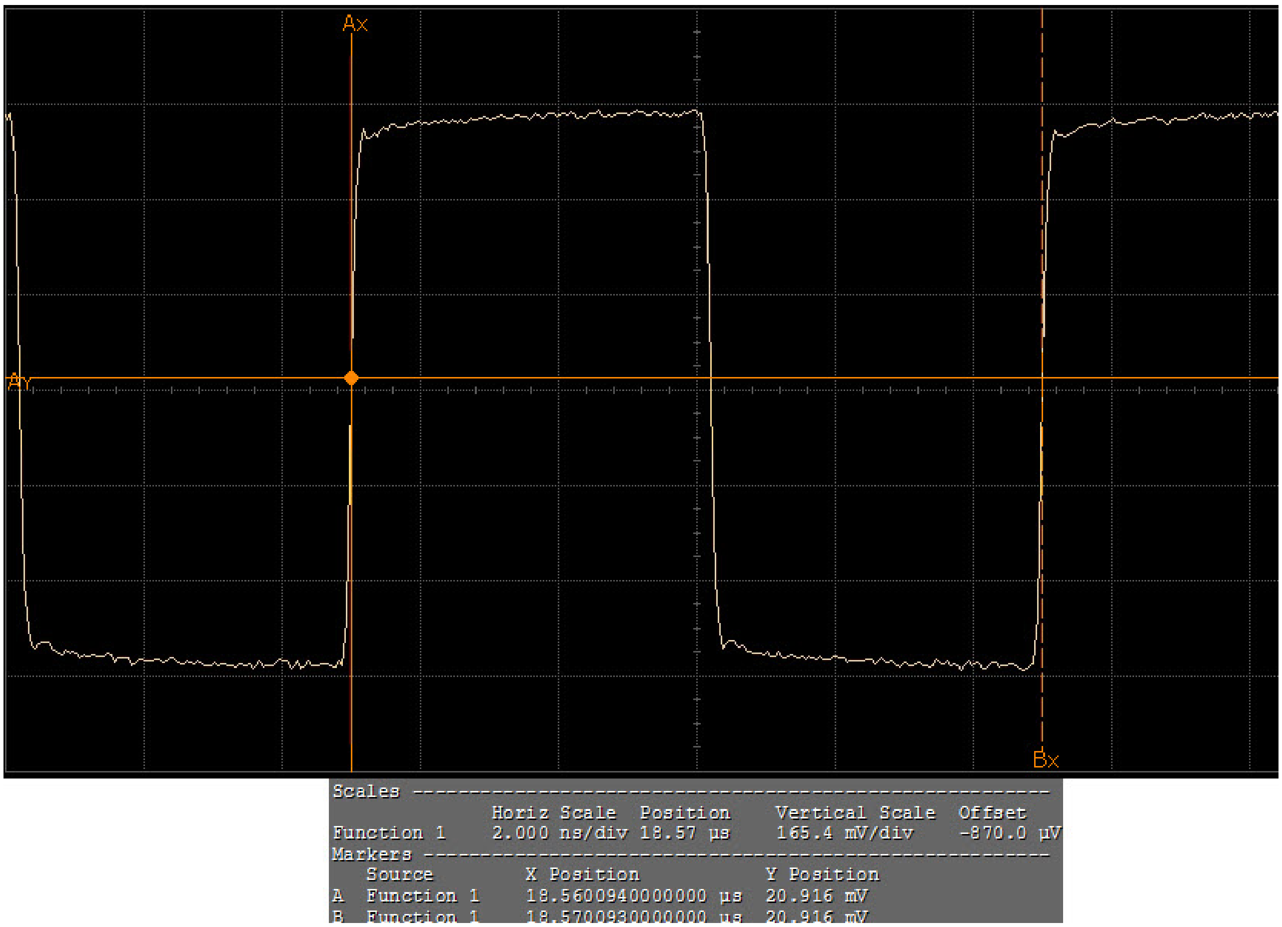


Figure 11 Reference Image for Duty Cycle

Variation of V_{Cross} Test

The variation of V_{Cross} test is measured at crossing point where the instantaneous voltage value of the rising edge of Refclk+ equals the falling edge of Refclk-. It is defined as the total variation of all voltages of rising Refclk+ and falling Refclk-.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{CROSS} Delta	Variation of V_{CROSS} over all rising clock edges	+140 mV

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 8-66.

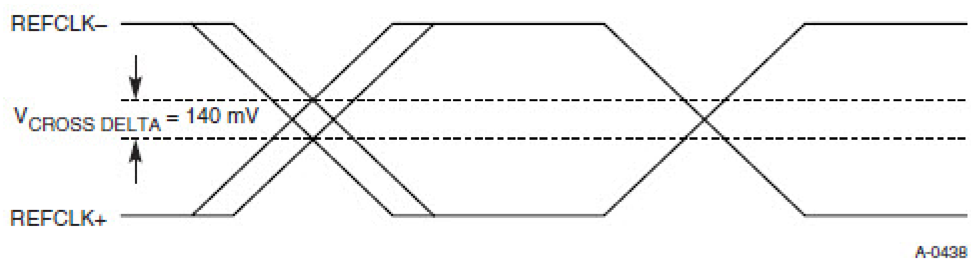


Figure 12 Single-Ended Measurement Points for Delta Cross Point

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Fits and displays all sample data on screen.
2. Uses MATLAB function to find the variation of V_{CROSS}. The MATLAB function does the following:
   a. Finds crossing edges for rising and falling edges.
   b. Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.
3. Finds the differential value between maximum crossing rising edge and minimum crossing rising edge as variation of V_{Cross}.
4. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as variation of $V_{Cross} < 140$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Clock Frequency (Common Clk)

This test verifies that the measured reference clock frequency, F_{REFCLK}, is within than the allowed frequency range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 2 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{REFCLK}	Refclk Frequency	99.97 MHz	100.03 MHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel** Setup.
4 Sets the time scale to 5 ns.
5 Fits and displays all sample data on the screen.
6 Enables jitter analysis so that measurements are made on all edges.
7 Measures the clock frequency.
8 Reports the mean frequency.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Max Input Voltage Test

The absolute max input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{MAX}	Absolute Max Input Voltage	+1.15V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the maximum instantaneous voltage including overshoot. See Figure 8-65.

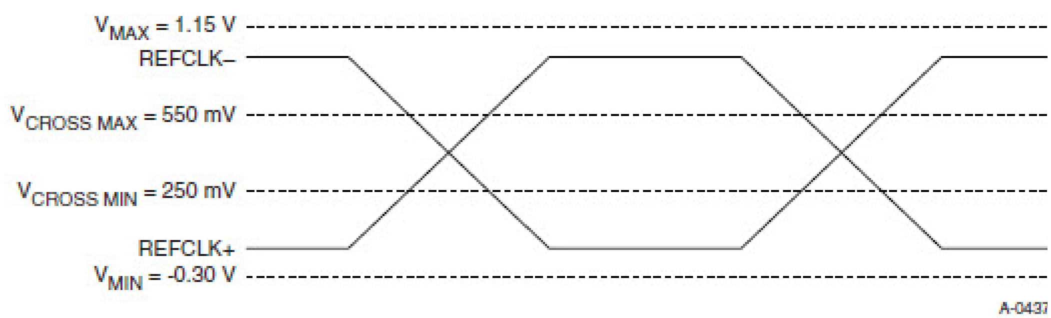


Figure 13 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5. Measures the RefClk+ maximum voltage using **V max** measurement.
6. Measures the RefClk- maximum voltage using **V max** measurement.
7. Compares the RefClk+ maximum voltage and the RefClk- maximum voltage.
8. Reports the largest value (worst value) as the Absolute Max Input Voltage.
9. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as variation of $V_{MAX} < +1.15V$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

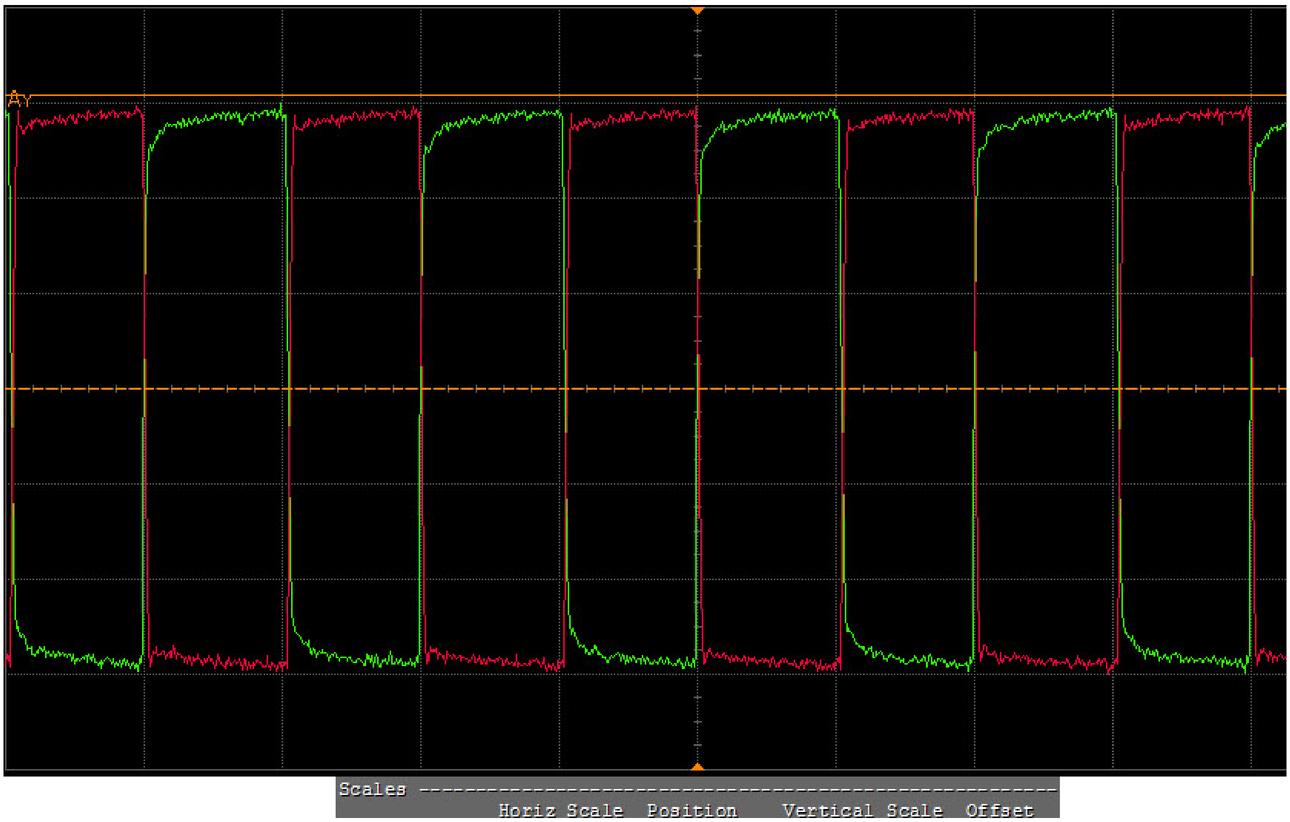


Figure 14 Reference Image for Absolute Max Input Voltage Test

Absolute Min Input Voltage Test

The absolute min input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)
V_{MIN}	Absolute Min Input Voltage	-0.3 V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the minimum instantaneous voltage including undershoot. See Figure 8-65.

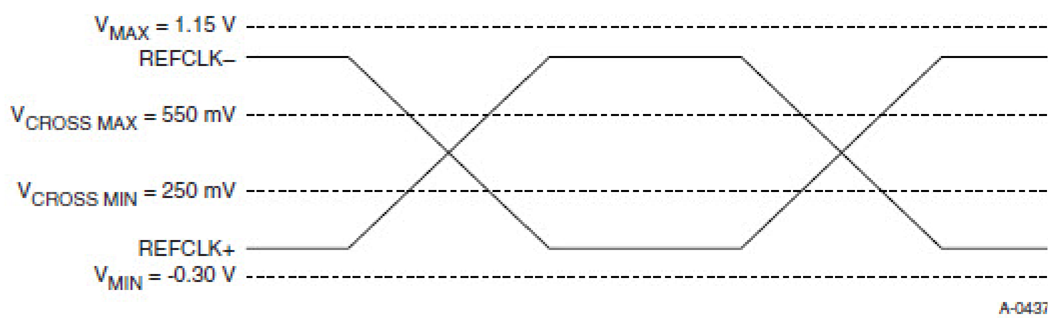


Figure 15 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures memory depth and sampling rate as per the data rate.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ minimum voltage using **V min** measurement.
6 Measures the RefClk- minimum voltage using **V min** measurement.
7 Compares the RefClk+ minimum voltage and the RefClk- minimum voltage.
8 Reports the smallest value (worst value) as the Absolute Min Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as variation of V_{MIN} < -0.3V.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

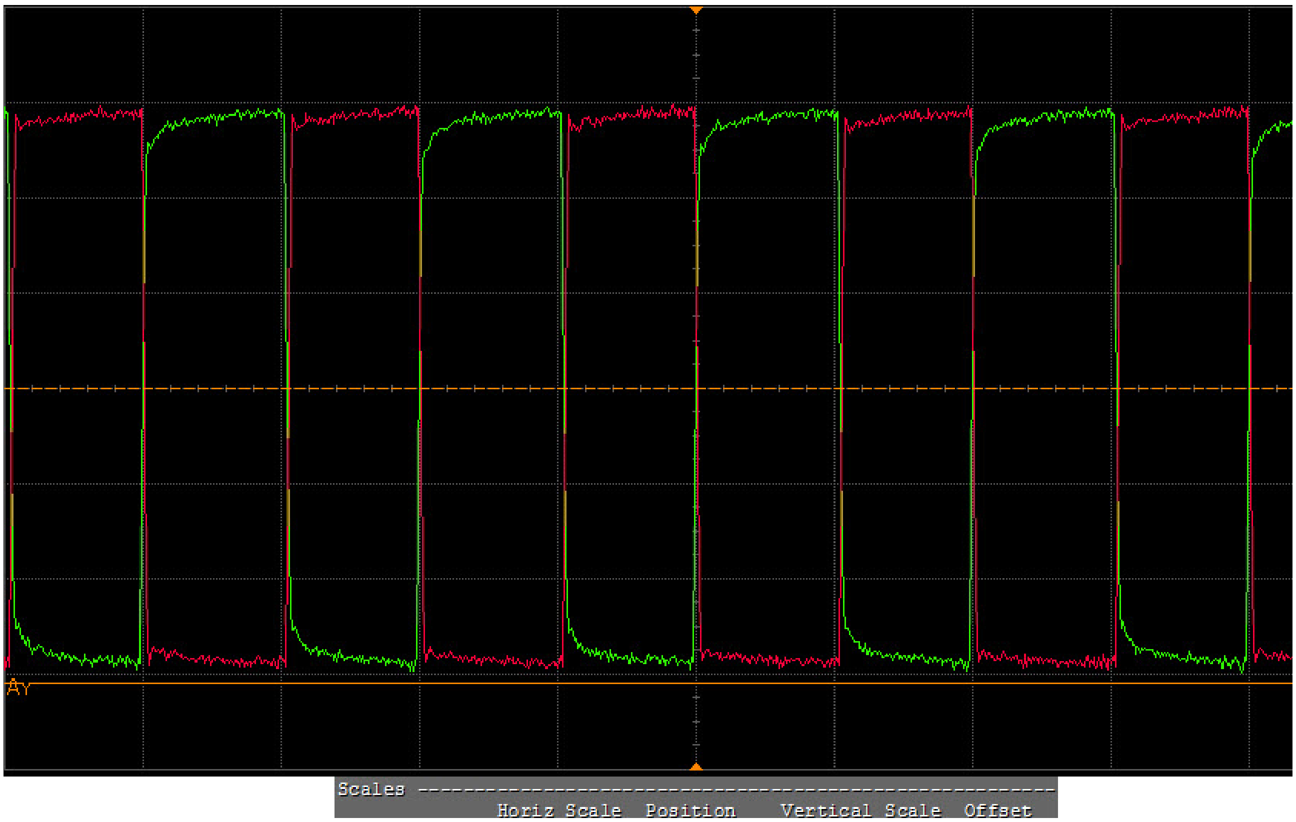


Figure 16 Reference Image for Absolute Min Input Voltage Test

Rise-Fall Matching Test

The rise-fall matching test matching applies to rising edge rate for RefClk+ and falling edge rate for RefClk-. It is measured using +/-75 mV window centered on the median cross point where RefClk+ rising meets RefClk- falling. The median cross point is used to calculate the voltage thresholds and oscilloscope is used to calculate the edge rate calculations. The rise edge rate of RefClk+ should be compared to the fall edge rate of RefClk-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	20%

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8-67.

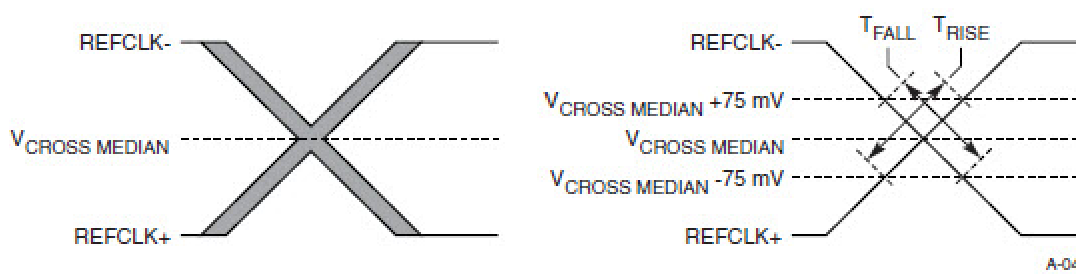


Figure 17 Single-Ended Measurement Points for Rise and Fall Time Matching

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures memory depth and sampling rate as per the data rate.
2 Fits and displays all sample data on screen.
3 Sets the Middle Threshold by ([maximum crossing rising edge value +minimum crossing rising edge value] / 2).
4 Sets the **Upper Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** + 75mV].
5 Sets the **Lower Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** - 75mV].
6 Measures RefClk+ rise time using **Rise time** measurement.

7 Measures the RefClk- fall time using **Fall time** measurement.

8 Finds the slowest edge between RefClk+ rise time and RefClk- fall time.

9 Computes the Rise-Fall matching value as follows:

$$\text{Rise-Fall Matching} = \frac{Abs|\text{RefClk+ rise time} - \text{RefClk- fall time}|}{\text{Slowest Edge Value} \times 100}$$

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as variation of RISE-FALL MATCHING < 20%.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

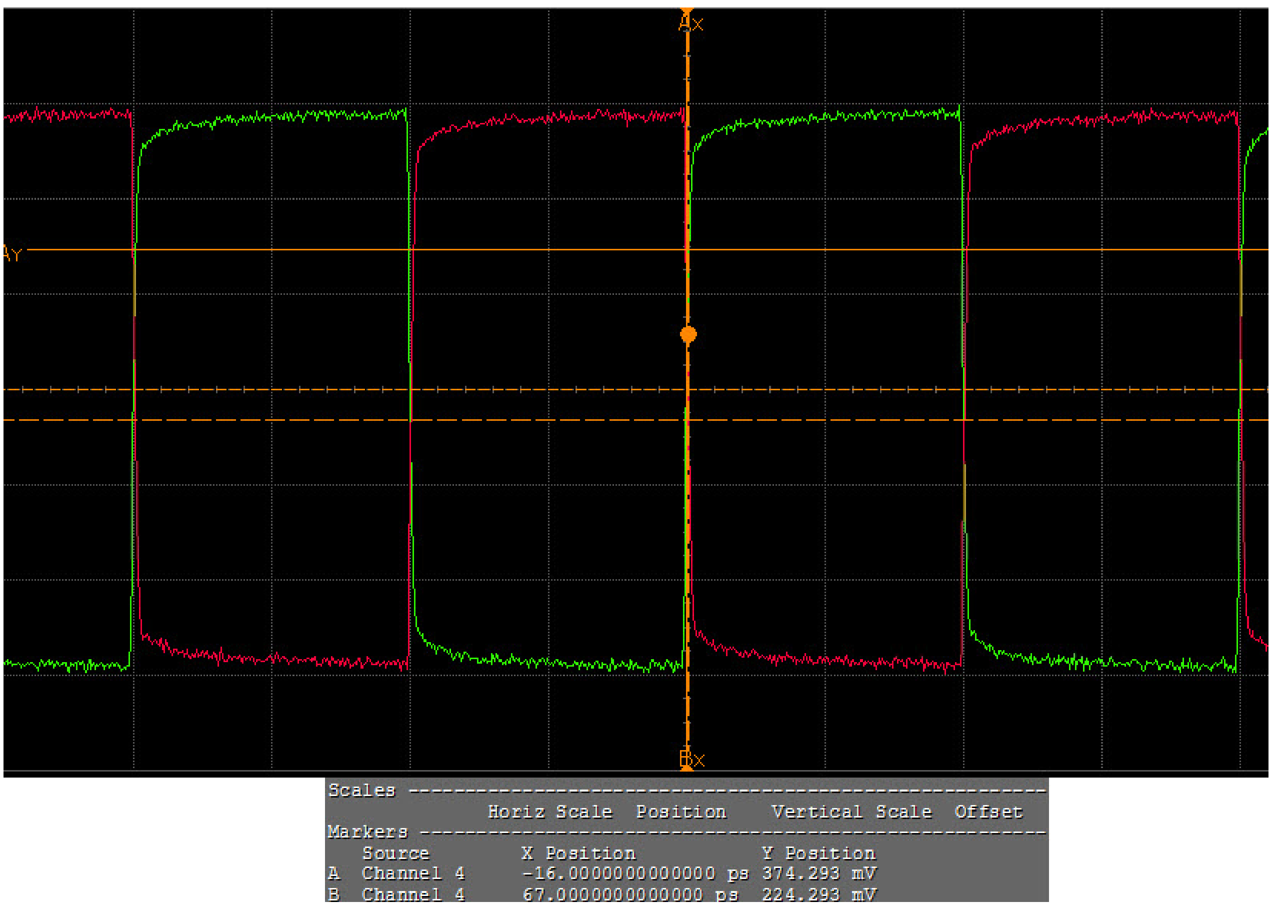


Figure 18 Reference Image for Rise-Fall Matching

RefClk SSC Frequency Range (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in PCIE Base Specification.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 3 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal frequency is ~ 100 MHz.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk SSC Deviation (Common Clk) Test

This test verifies that the measured reference clock SSC deviation is within the conformance limits specified in PCIE Base Specification.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 4 SSC Deviation Test Details

Symbol	Description	Min/Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53 /0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal frequency is ~ 100 MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min, and Period_average.
9. Computes SSC deviation Max(%) = ((1 / 100MHz) - SSC's Minimum UI) / (1 / 100MHz) * 100
10. Computes SSC deviation Min(%) = ((1 / 100MHz) - SSC's Maximum UI) / (1 / 100MHz) * 100
11. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk Max SSC df/dt (Slew Rate) (Common Clk) Test

This test verifies that the reference clock maximum SSC df/dt is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 5 RefClk Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   - *a* Generates a differential plot (x_n - x_{n-1}).
   - *b* The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

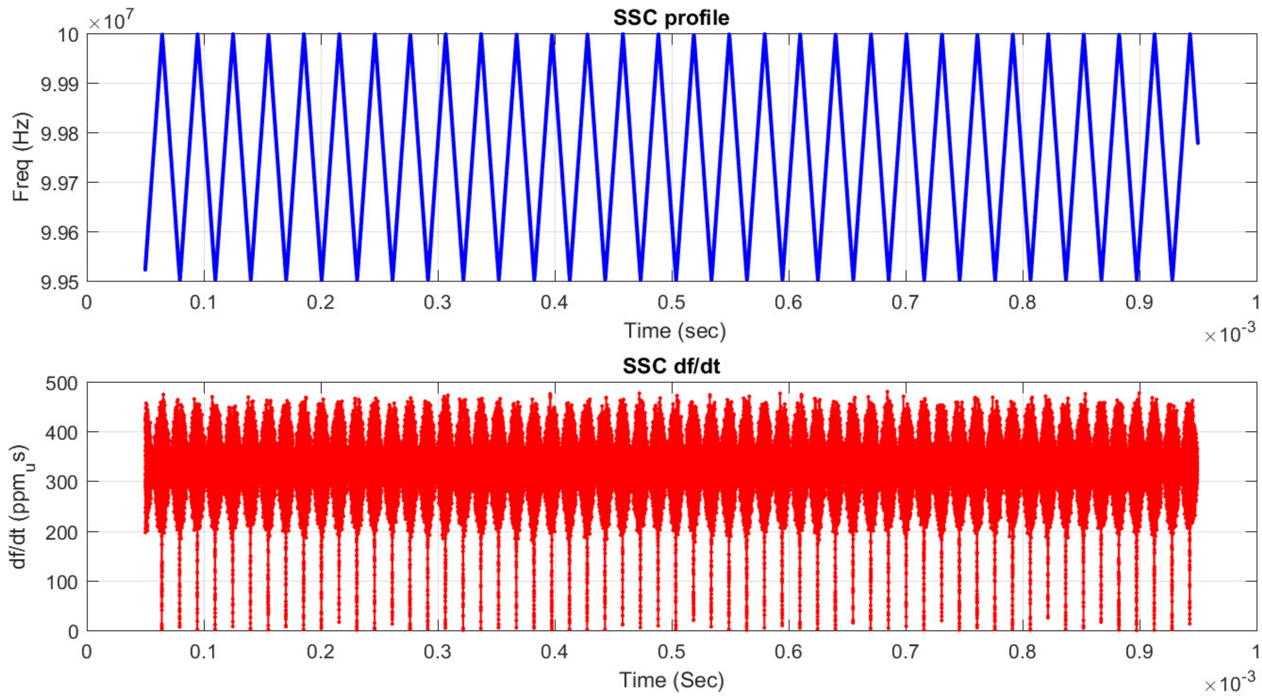


Figure 19 Maximum SSC Slew Rate

Part IX
PCI-Express Gen6 2.5 GT/s Tests

25 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 2.5 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.3.1, Figure 8-1.

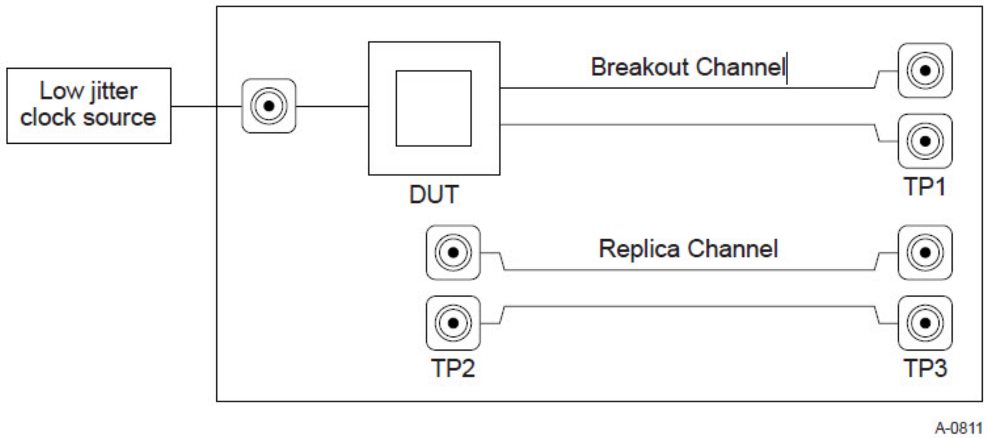


Figure 20 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 2.5 GT/s Tests > Transmitter (Tx) Tests**.

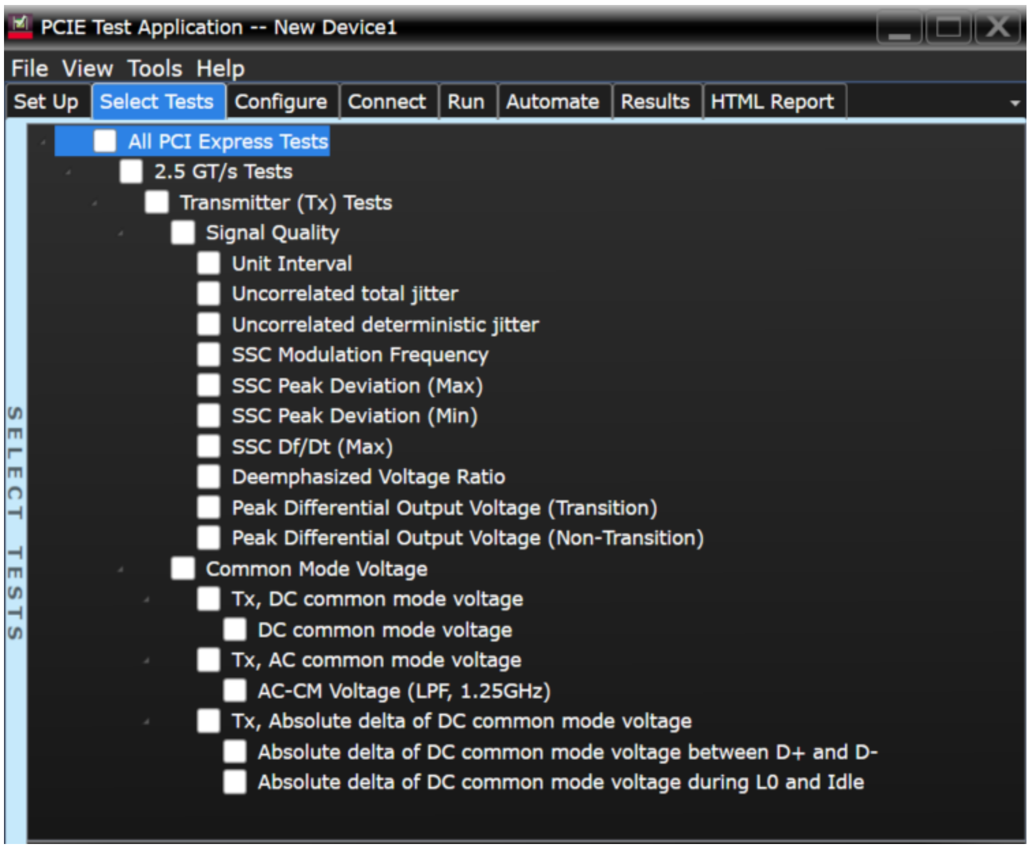


Figure 21 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 6 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

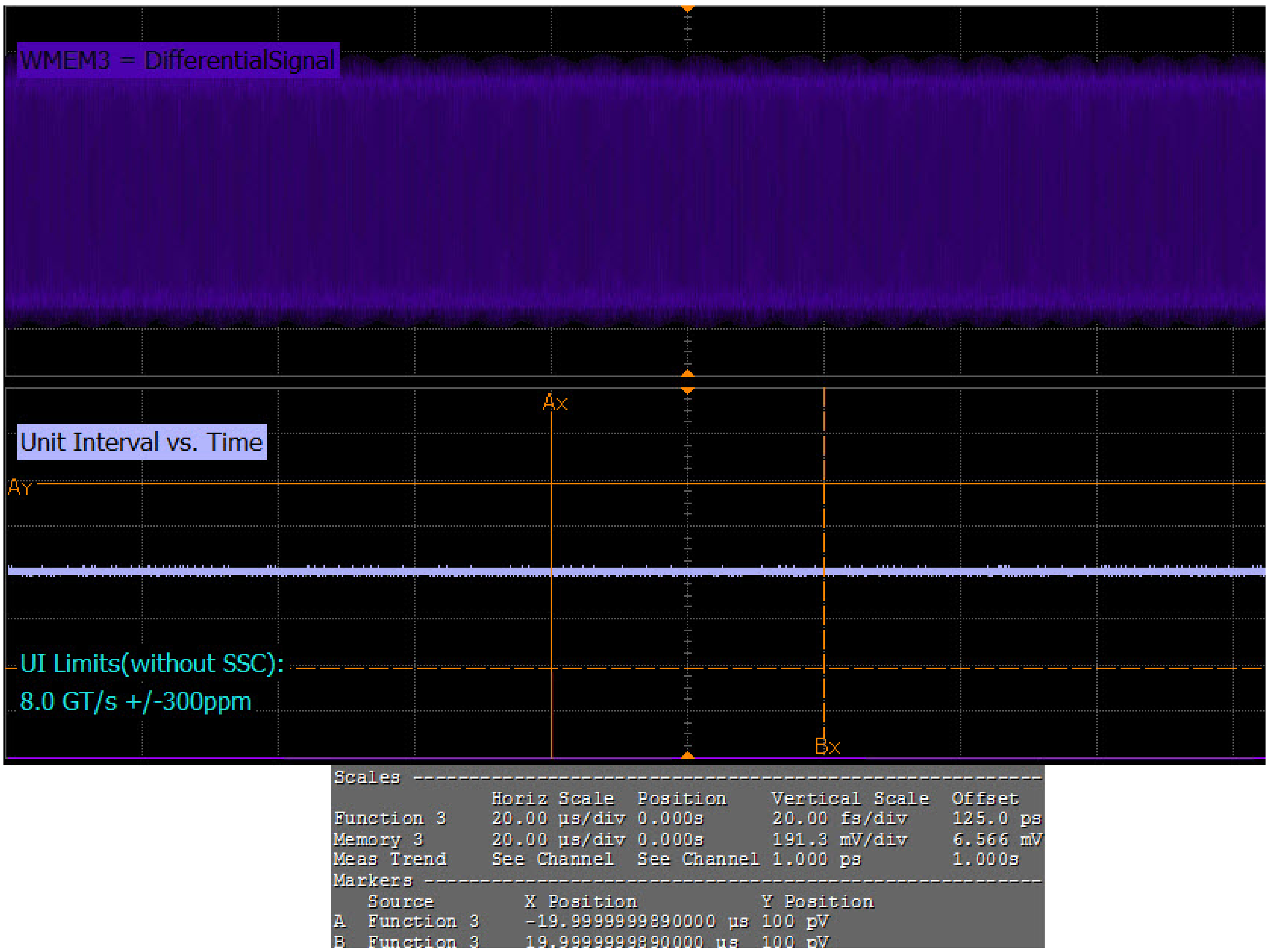


Figure 22 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 7 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	100.00 ps PP at 10^{-12}

Test Definition Notes from the Specification

- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.
- See Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$)) of the PCI Express Base Specification, Revision 6.0 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 8 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	100 ps PP

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak uncorrelated deterministic jitter value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 9 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 10 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	30.0 m%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 2.5 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option..
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 11 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.530%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC df/dt (Max) Test (Slew Rate)

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 12 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a. Generates a differential plot (x_n - x_{n-1}).
   b. The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

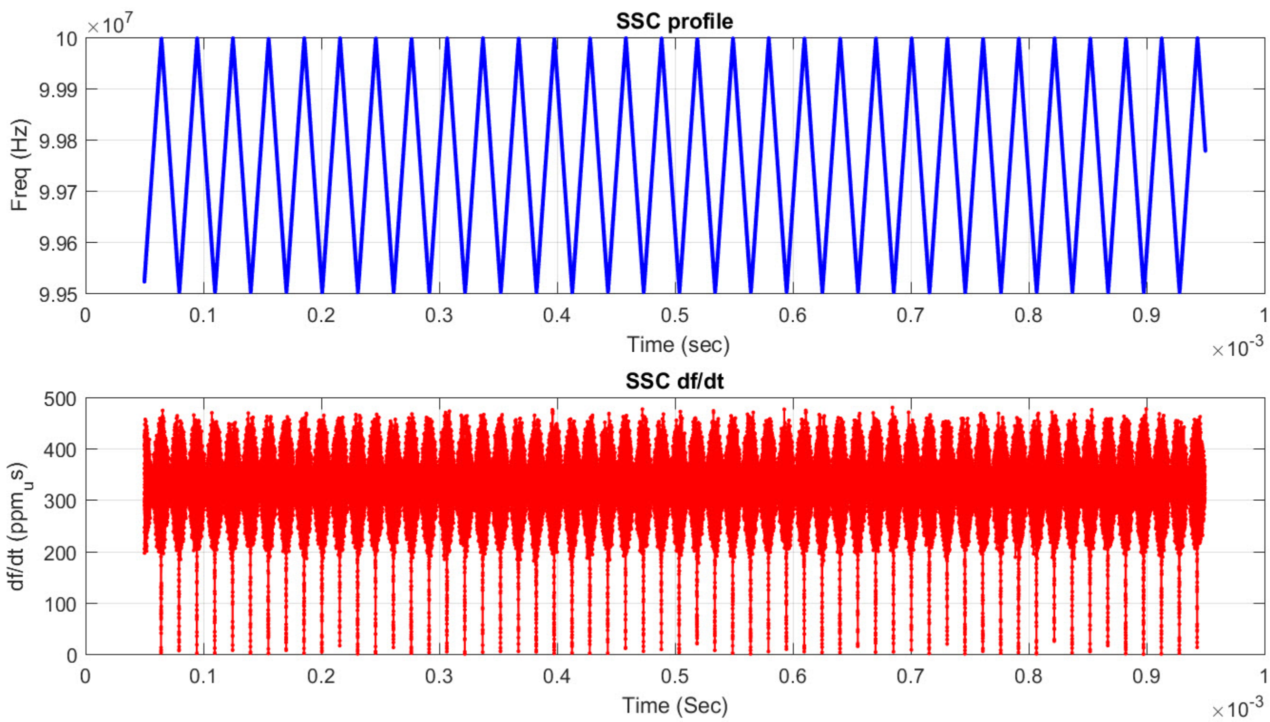


Figure 23 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 13 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground. See also the $I_{TX\text{-}SHORT}$.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

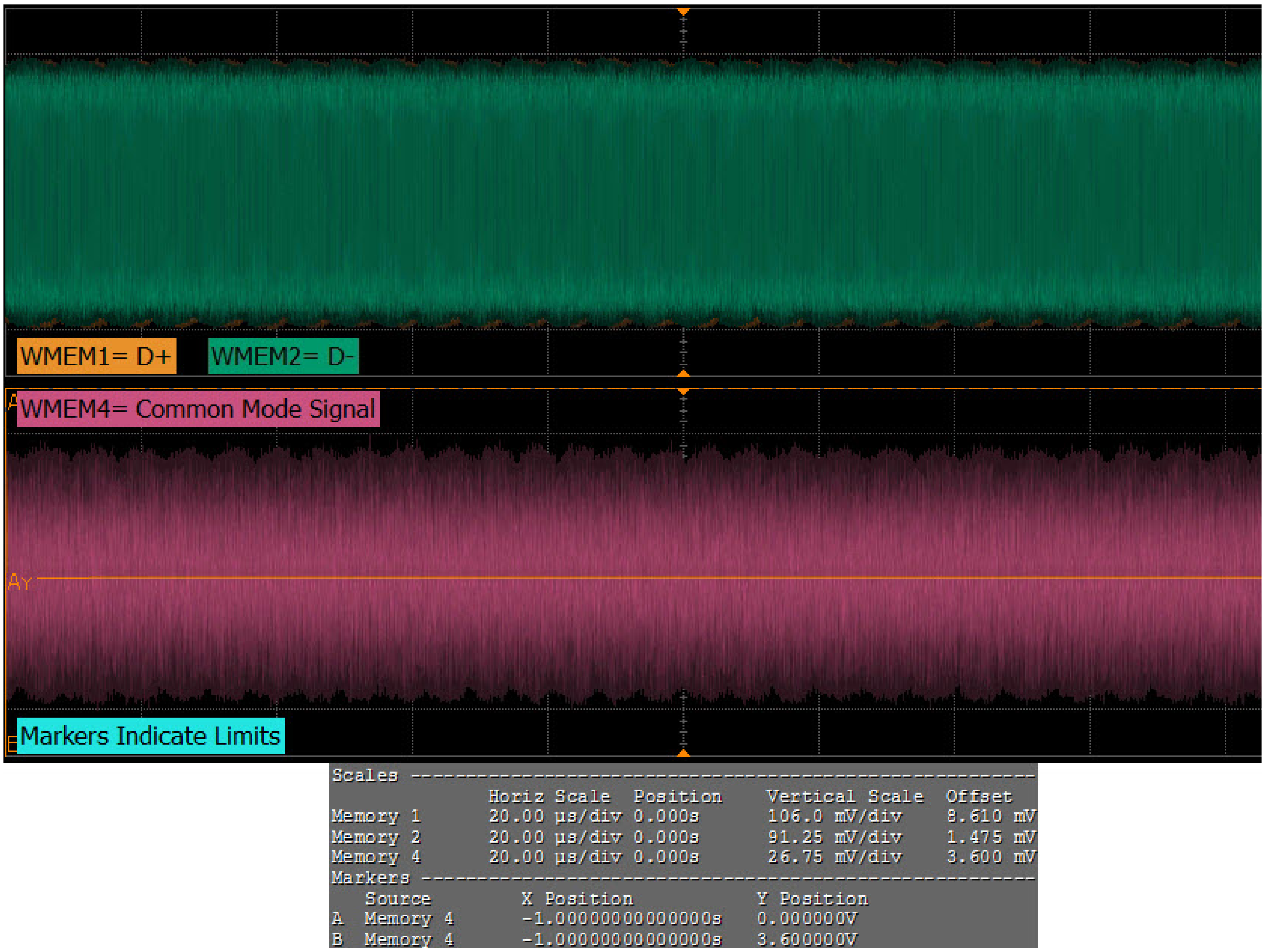


Figure 24 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 1.25 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 14 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $VT_{X-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Uses UDF LPF (Low Pass Filter) with cut off frequency of 1.25 GHz to the common mode signal.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

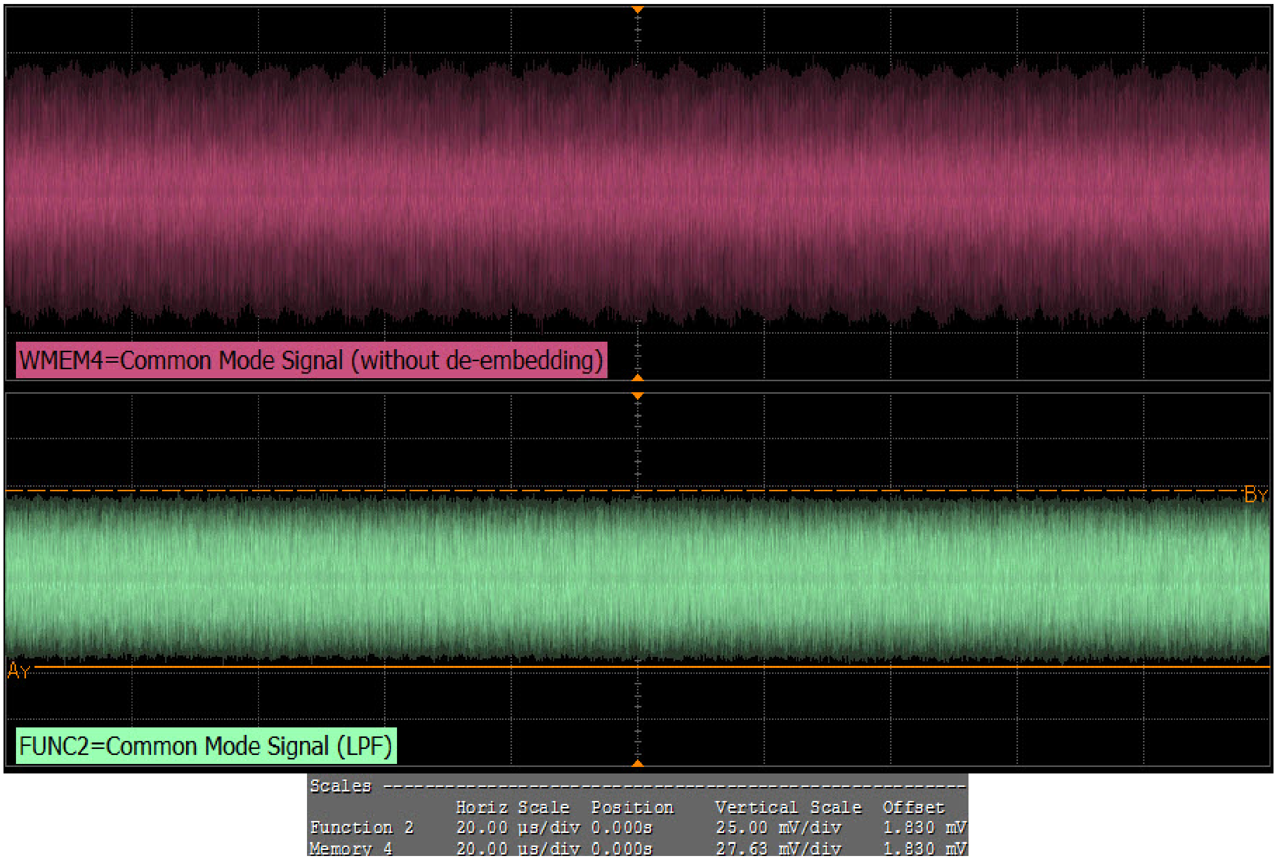


Figure 25 Reference Image for AC-CM voltage (4GHz LPF) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25\ mV$

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 15 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 16 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

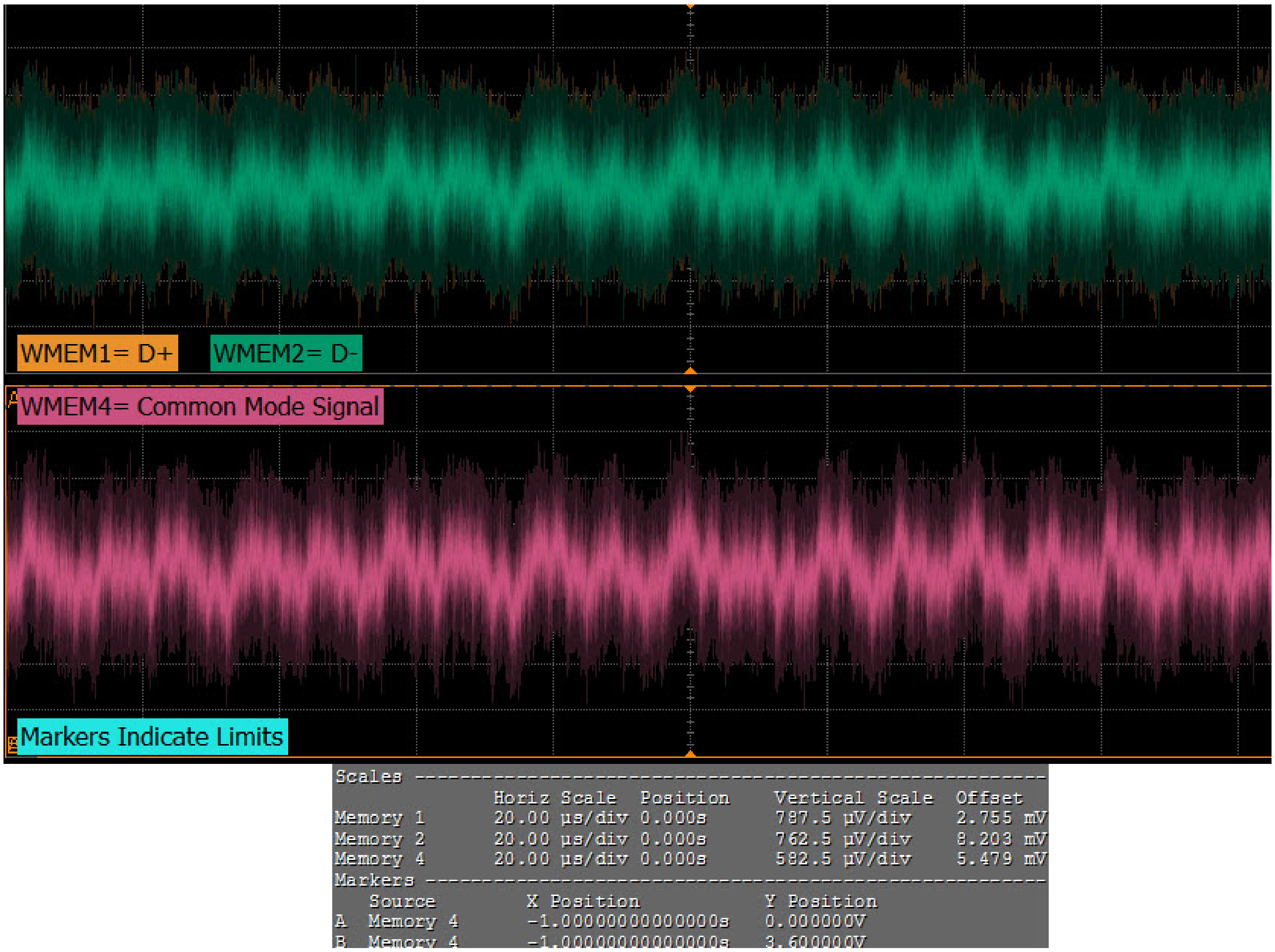


Figure 26 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Deemphasized Voltage Ratio Test

The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, $V_{TX-DE-RATIO}$ = -20log10 ($V_{TX-DIFF-PP}$/$V_{TX-DE-EMPH-PP}$).

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 17 Deemphasized Voltage Ratio (-3.5 dB) Test Details

Symbol	Description	Min	Max
$V_{TX-DE-RATIO}$	Deemphasized Voltage Ratio	-4.500 dB	-2.500 dB

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   - *a* Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with Damping Factor of 0.707.
   - *b* Sets the value of **Nominal Data Rate** as **2.5 GT/s.**
   - *c* Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s.**
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and bases.
7. Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.
8. Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.
9. Calculates de-emphasis ratio using the following formula:

   $$De\text{-}emphasis\ ratio = -20*log10(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$$

10. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the transition eye diagram data from the SigTest tools as $V_{TX\text{-}DIFF\text{-}PP}$.
2. Extracts the non-transition eye diagram data from the SigTest tools as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$.
3. Calculates de-emphasis ratio using the following formula:

   De-emphasis ratio: $-20*\log_{10}(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$

4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

The **Peak Differential Input Voltage** test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the standard specifications.

$V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 18 Peak Differential Output Voltage (Transition) Test Details

Symbol	Description	Min	Max
$V_{TX-DIFF-p-p}$	Peak Differential Output Voltage	0.800 V	1.00 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.

   b Sets the value of **Nominal Data Rate** as **2.5 GT/s.**

   c Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s.**

3 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

4 Measures the transition bits eye top and bases.

5 Finds the differential value between the transition bits eye top and base using **Histogram**.

6 Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the transition eye diagram data from the SigTest tools.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTest tools.
3. Compares the measured peak differential output/input voltage (transition) value to the compliance test limits.
4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}, Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 19 Peak Differential Output Voltage (Non-Transition) Test Details

Symbol	Description	Min	Max
$V_{TX-DIFF-p-p}$	Peak Differential Output Voltage	0.4765 V	1.00 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
   b. Sets the value of **Nominal Data Rate** as **2.5 GT/s.**
   c. Sets the value of **Loop Bandwidth** as **1.5 MHz** for **2.5 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and bases.
5. Finds the differential value between the non-transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the non-transition eye diagram data from the SigTest tools.
2 Gets largest non-transition amplitude (outer eye), smallest non-transition amplitude (inner eye) test results from SigTest tools.
3 Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

26 Reference Clock Tests, 2.5 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCIe 6.0 Reference Clock tests at 2.5 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

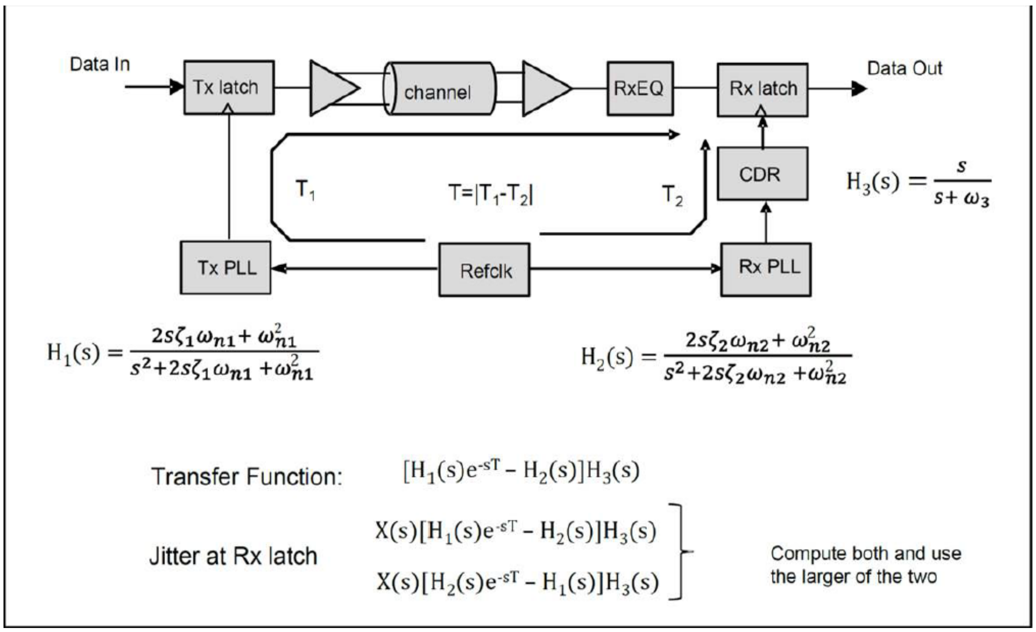
NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 2.5 GT/s, PCI-E 6.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 2.5 GT/s

PLL #1, PLL #2	0.01 dB peaking	3.0 dB peaking
$BW_{PLL}(min)$ = 1.5 MHz	ω_{n1}= .336 Mrad/s ζ_1 = 14	ω_{n1}= 5.09 Mrad/s ζ_1 = 0.54
$BW_{PLL}(max)$ = 22 MHz	ω_{n1}= 4.93 Mrad/s ζ_1 = 14	ω_{n1}= 74.68 Mrad/s ζ_1 = 0.54

$BW_{CDR}(min)$ = 1.5 MHz, 1st order — **CDR**

16 combinations

2.5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73

PLL #2	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
$BW_{PLL}(max)$ = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15

$BW_{CDR}(min)$ = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 0.5 MHz	ω_{n1}= .112Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 1.8 MHz	ω_{n1}= .403Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC	CDR

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

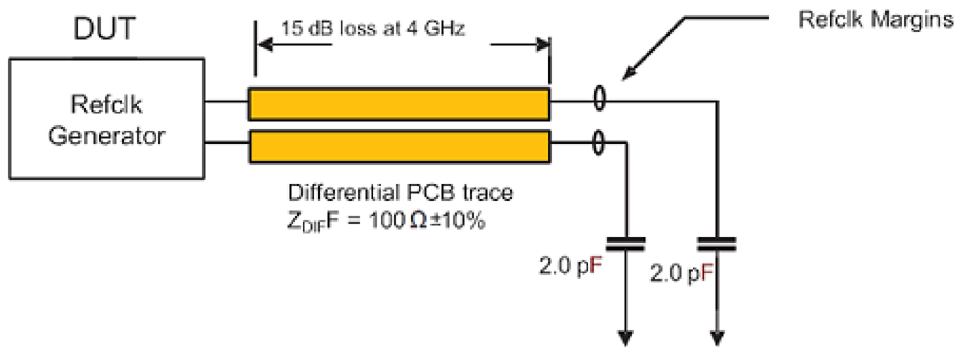


Figure 27 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 2.5 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

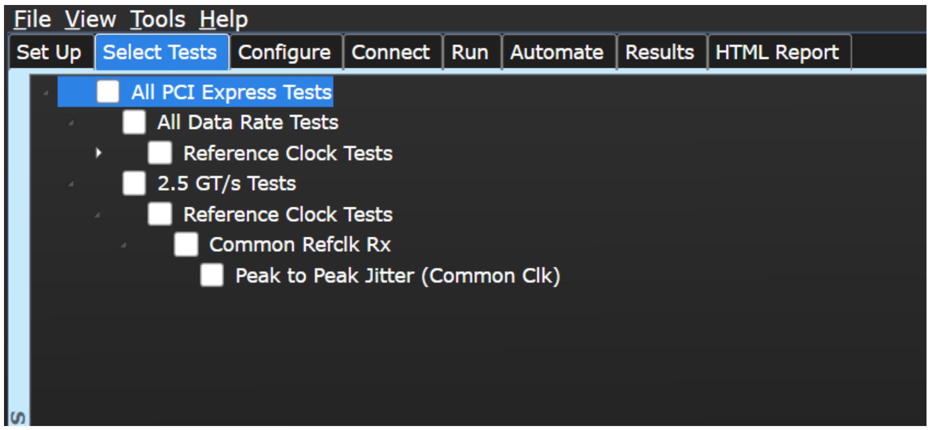


Figure 28 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

Peak to Peak Jitter (Common Clk) Test

This test verifies that the measured peak to peak jitter, $T_{REFCLK-PP-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 20 RMS Jitter Test Details

Symbol	Description	Value
$T_{REFCLK-PP-CC}$	Peak to Peak Refclk jitter for common Refclk architecture	86 ps pp

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100 MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.
10. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
    - *a* Converts time domain TIE data to frequency domain.
    - *b* Applies the PLL filter using parameters for common clocked architecture.
    - *c* Converts back the frequency domain TIE data to time domains.
    - *d* Computes the filtered peak-peak jitter.

11 Reports filtered peak-peak jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

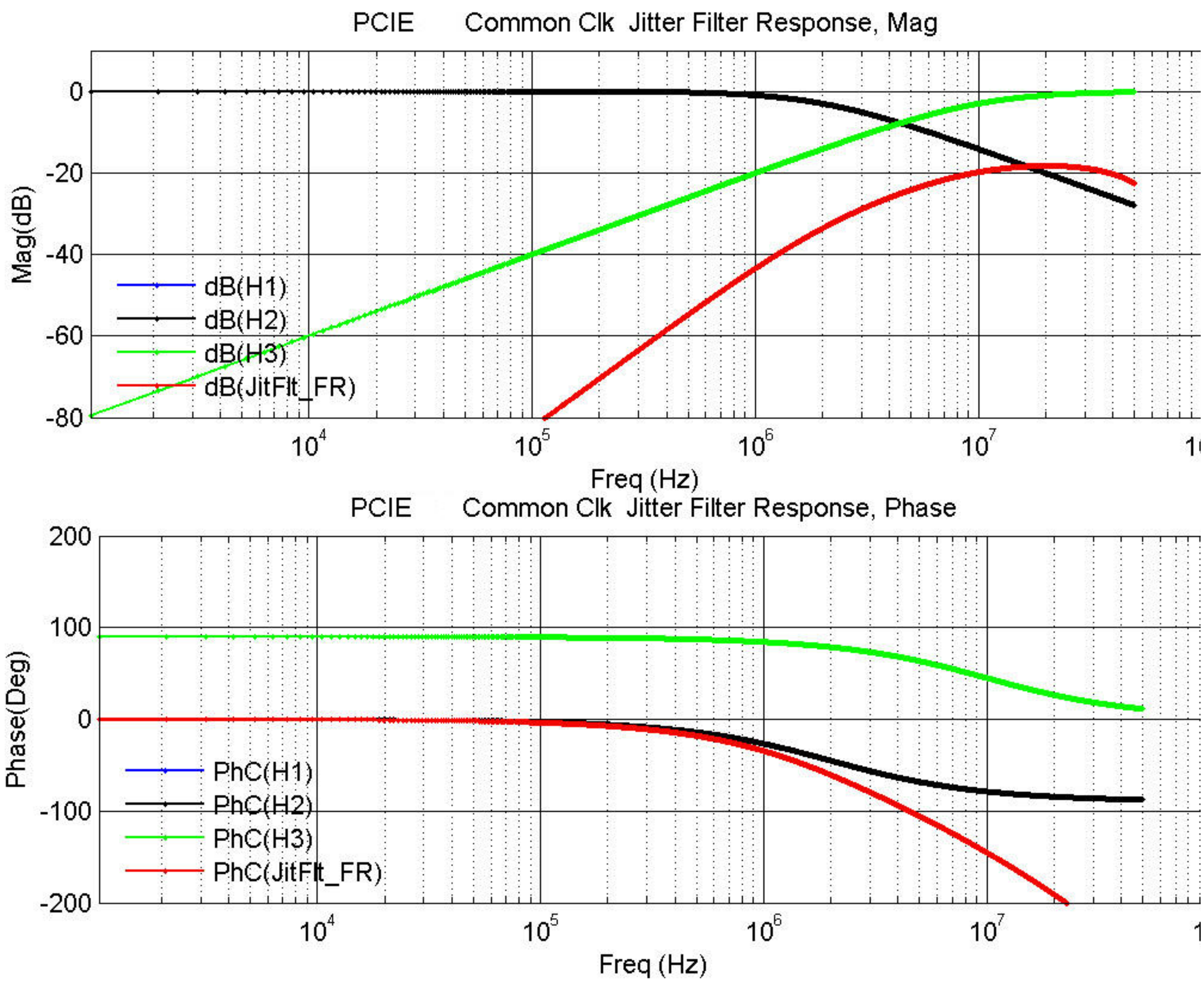


Figure 29 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

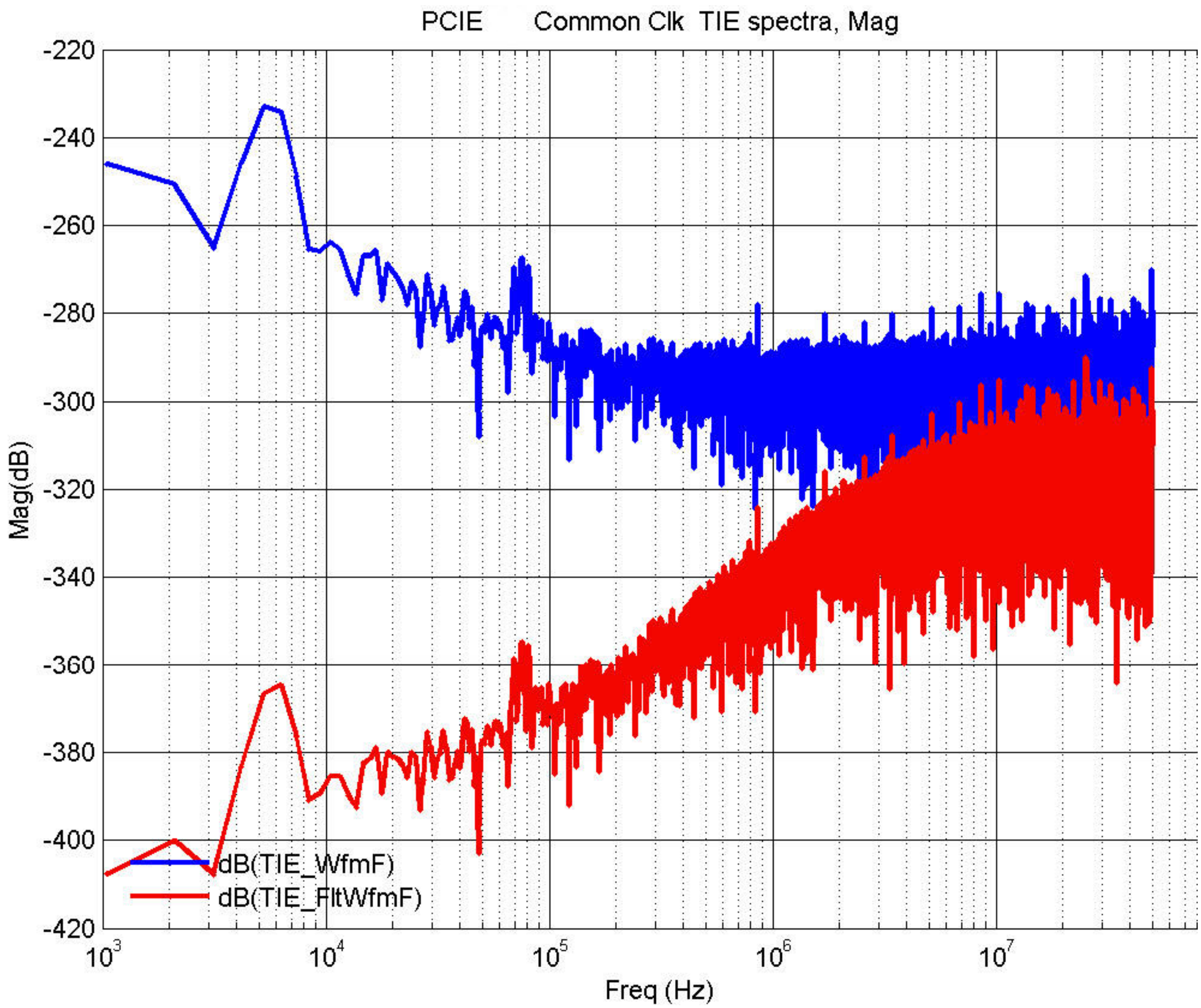


Figure 30 Reference Image for Common Clock TIE Spectra RMS Jitter Test

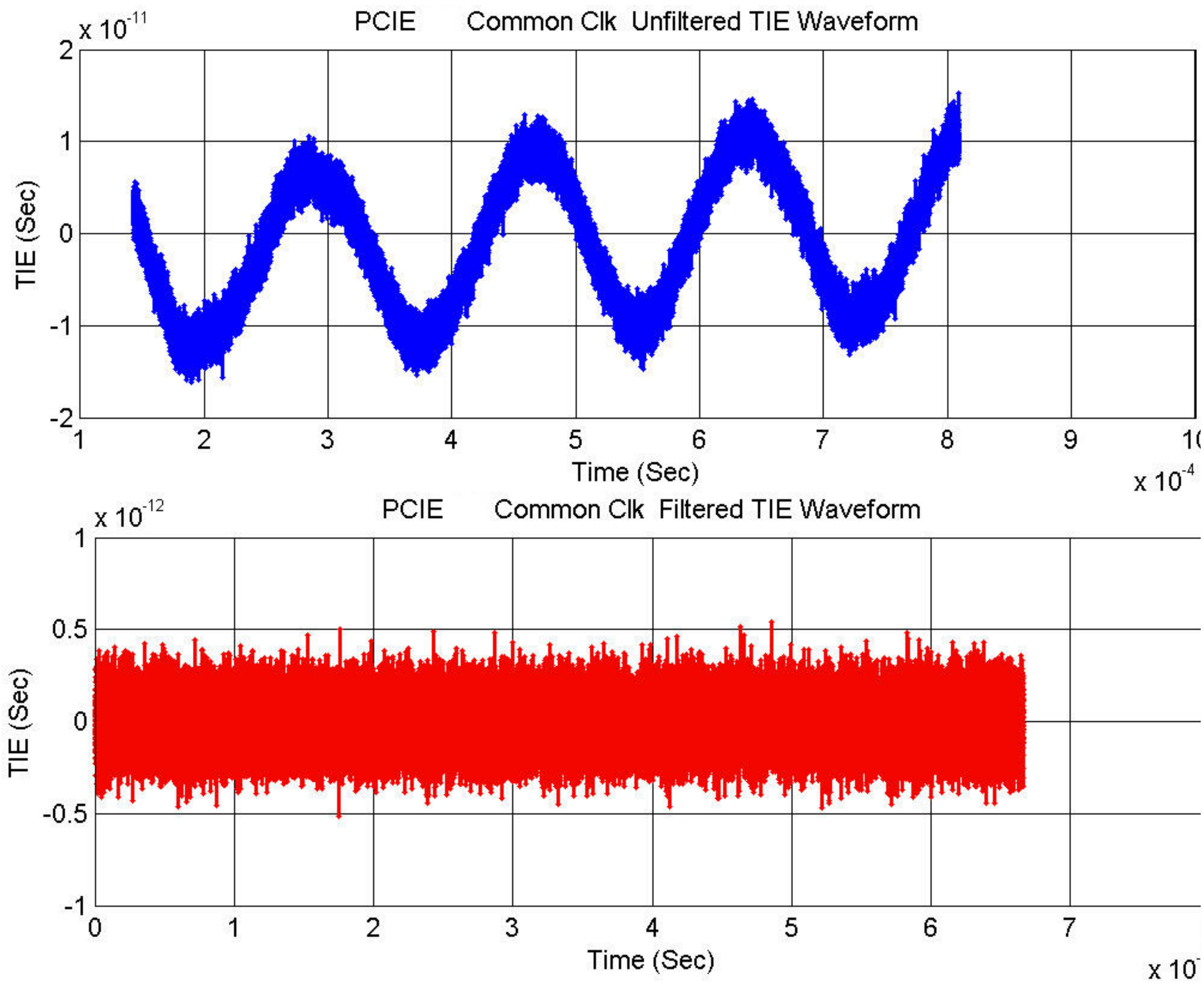


Figure 31 Reference Image for TIE Waveform RMS Jitter Test

Part X
PCI-Express Gen6
5.0 GT/s Tests

KEYSIGHT
TECHNOLOGIES

27 Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 5.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.3.1, Figure 8-1.

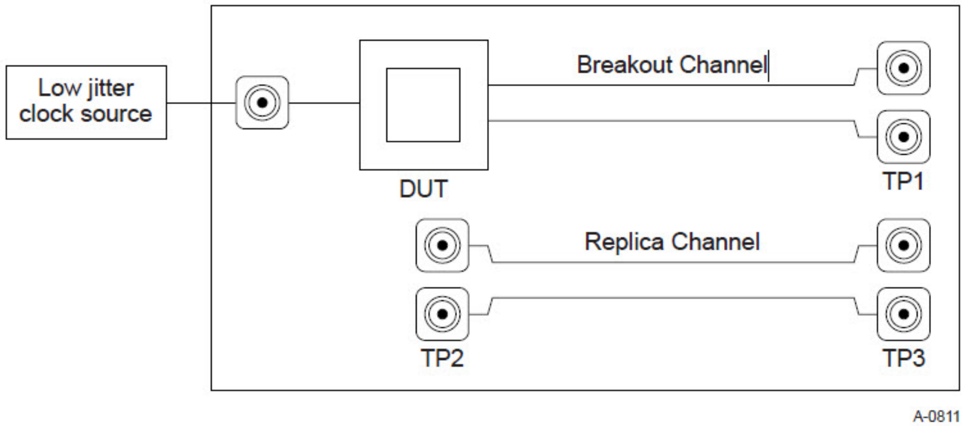


Figure 32 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 5.0 GT/s Tests > Transmitter (Tx) Tests**.

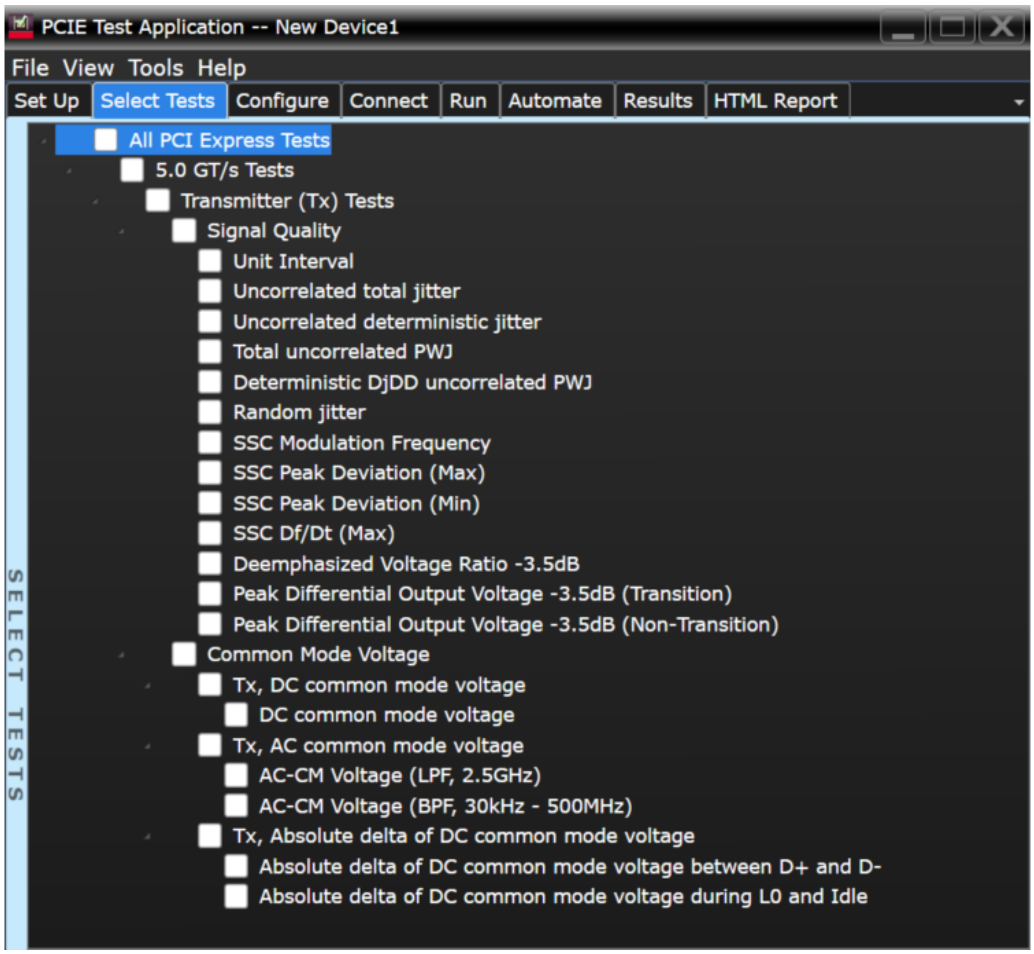


Figure 33 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

‘n’ is the index of UI in the current 2,000,000 UI clock recovery window.

‘p’ indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 21 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

  a Selects **Unit Interval** as data measurement analysis unit.

  b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.

4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 6.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

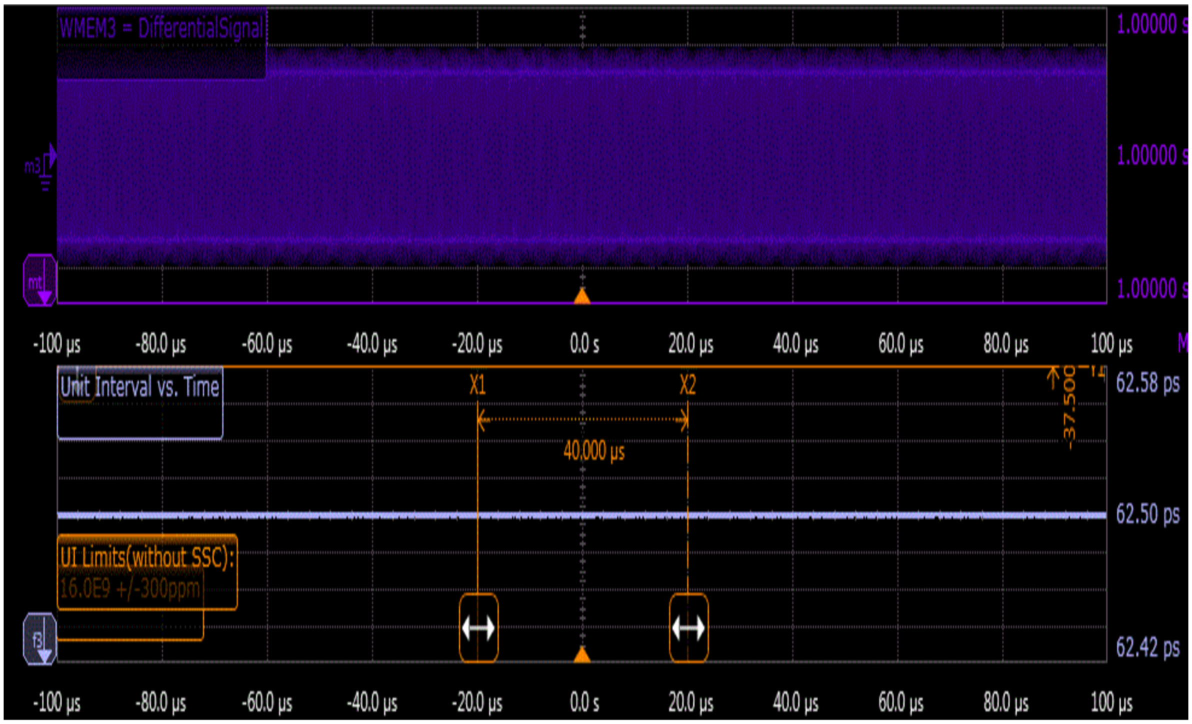


Figure 34 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 22 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	50 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 23 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	30 ps PP

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak uncorrelated deterministic jitter value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 24 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	40 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 25 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	40 ps PP

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test (Information Only Test)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 26 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.4 - 3.6 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 27 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 28 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	30.0 m%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 5.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 29 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 5.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC df/dt (Max) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 30 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures memory depth and sampling rate as per the data rate.
3 Fits and displays all sample data on screen.
4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5 Analyzes measurements trend using the jitter **Meas Trend** function.
6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a Generates a differential plot (x_n - x_{n-1}).
   b The maximum slew rate corresponds to the peak of the differential plot.
7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

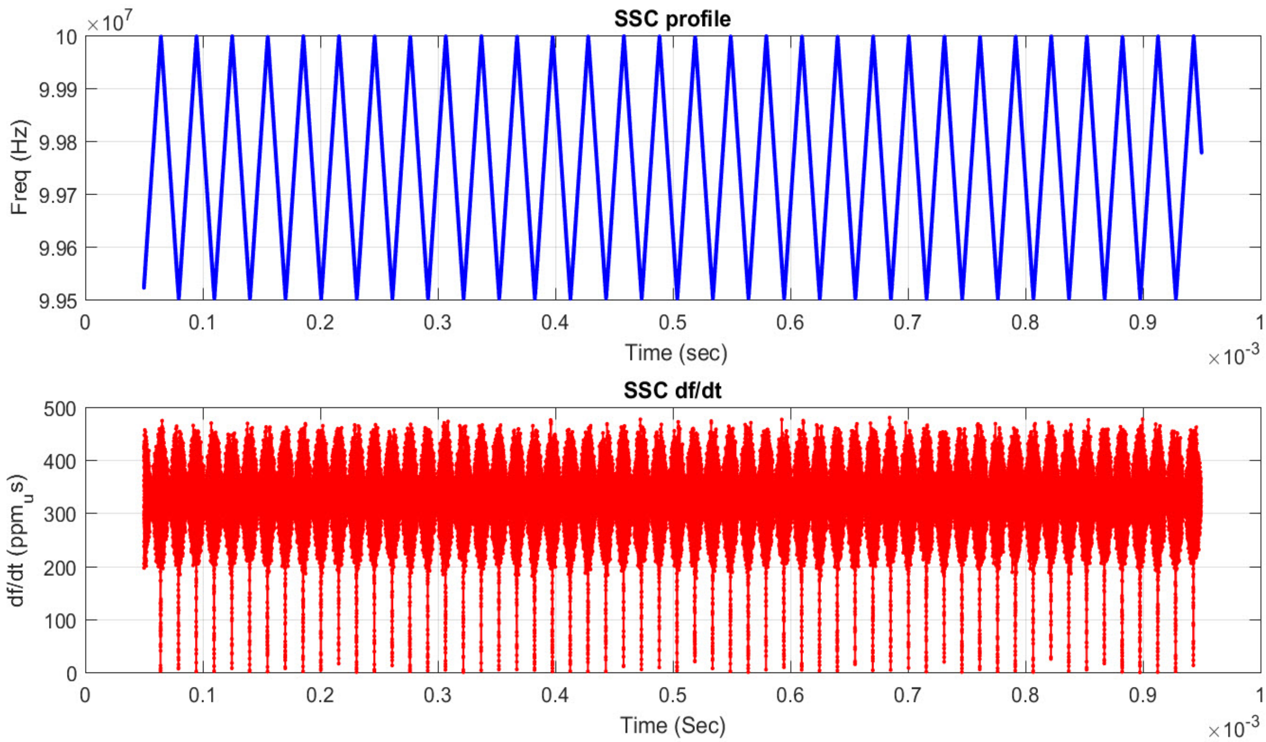


Figure 35 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX-DC-CM} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-DC-}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 31 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

  a Enables and displays common mode measurements.

  b Loads common mode signal to waveform memory.

  c Loads and enhance dynamic range D+ signal and D- signal.

  d Enables the average common mode measurement.

  e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 2.5 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max(V_{D+} + V_{D-})/2 - \min(V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 32 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Uses UDF LPF (Low Pass Filter) with cut off frequency of 2.5 GHz to the common mode signal.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 33 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	Tx AC peak-peak common mode voltage	100 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 2.5 GHz) test.

1 Gets PCIE6 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25$ mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 34 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Test Definition Notes from the Specification

$| V_{TX-CM-DC-D+\ [during\ L0]} - V_{TX-CM-DC-D-\ [during\ L0]} | \leq 25$mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $| V_{TX-D+\ [during\ L0]} |$

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $| V_{TX-D-\ [during\ L0]} |$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 35 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Test Definition Notes from the Specification

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

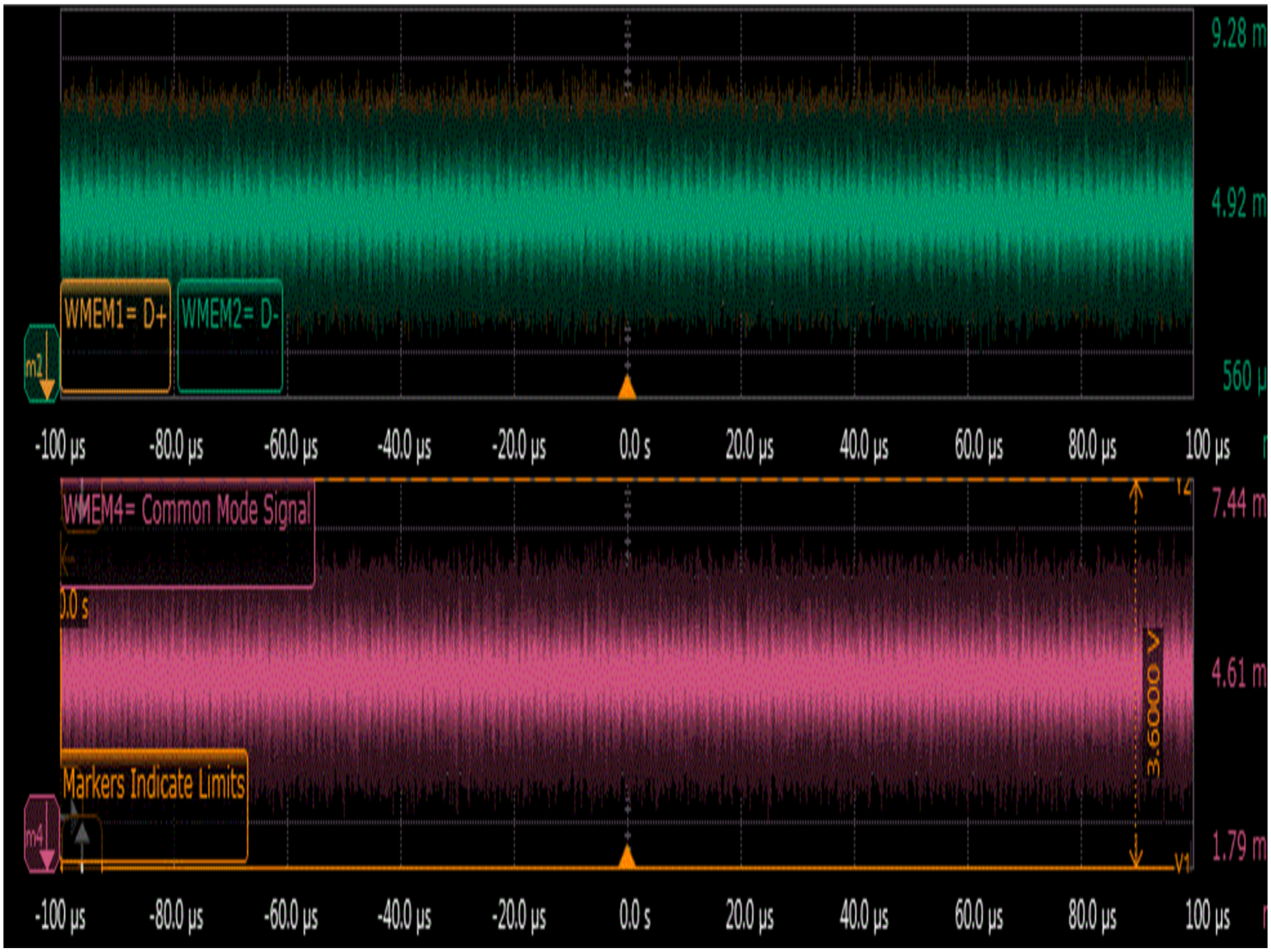


Figure 36 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 36 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground. See also the $I_{TX\text{-}SHORT}$.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as $V_{TX-DC-CM}$ is `0` to `3.6 V (+/- 100mV)`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

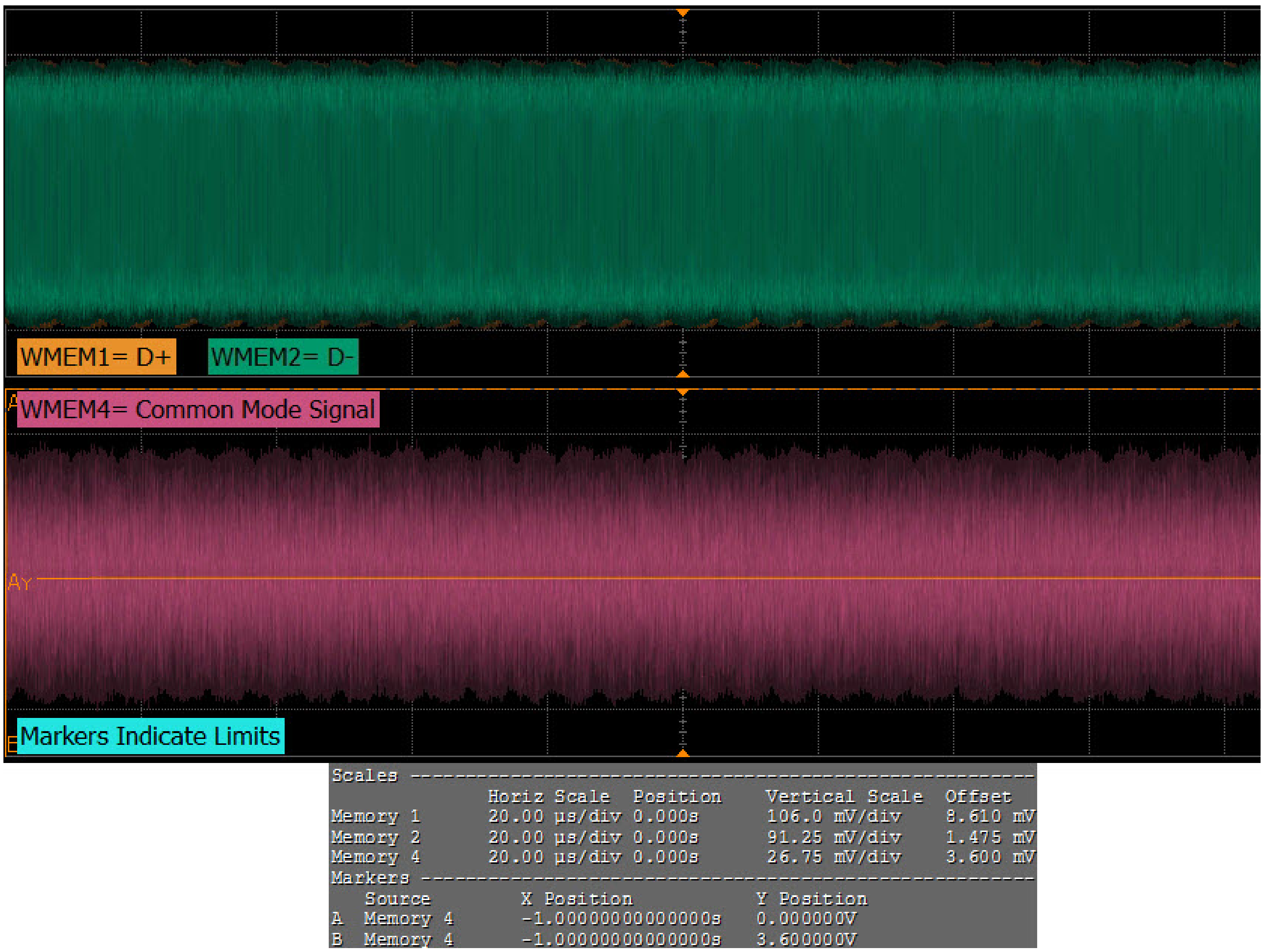


Figure 37 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 1.25 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 37 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $VT_{X-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 1.25 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

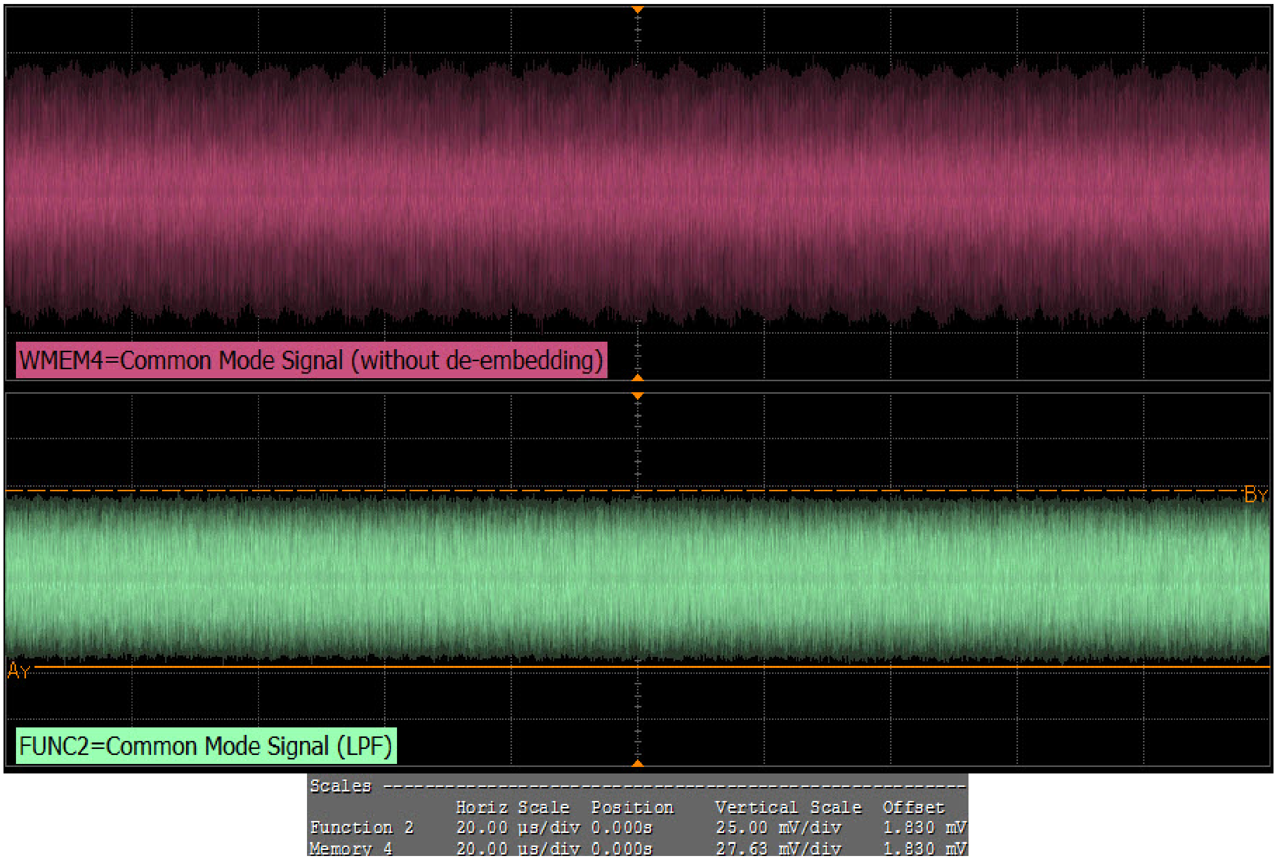


Figure 38 Reference Image for AC-CM voltage (4GHz LPF) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25$ mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 38 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX-CM-DC\ [during\ L0]} - V_{TX-CM-Idle-DC\ [during\ electrical\ idle]}| \leq 100$ mV

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$

$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 39 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

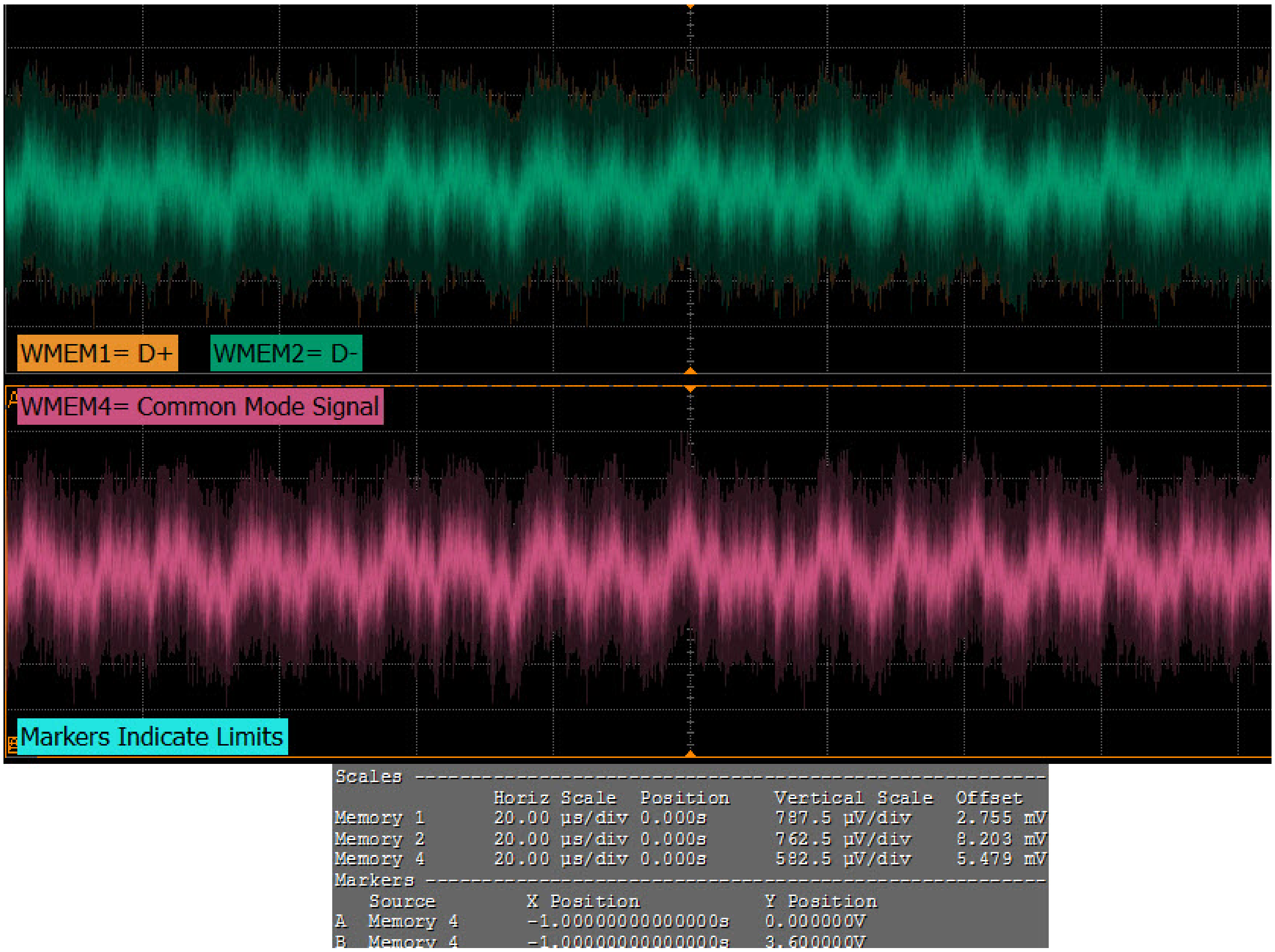


Figure 39 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Deemphasized Voltage Ratio Test

The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, $V_{TX-DE-RATIO} = -20log10\ (V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 40 Deemphasized Voltage Ratio -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DE-RATIO}$	Deemphasized Voltage Ratio	-4.500 dB	-2.500 dB

Table 41 Deemphasized Voltage Ratio -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DE-RATIO}$	Deemphasized Voltage Ratio	-7.500 dB	-4.500 dB

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   - *a* Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with Damping Factor of 0.707.
   - *b* Sets the value of **Nominal Data Rate** as **5.0 GT/s**.
   - *c* Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and bases.
7. Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.
8. Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.
9. Calculates de-emphasis ratio using the following formula:

   De-emphasis ratio = $-20*log10(V_{TX\text{-}DIFF\text{-}PP}/V_{TX\text{-}DE\text{-}EMPH\text{-}PP})$

10. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the transition eye diagram data from the SigTest tools as $V_{TX-DIFF-PP}$.

2 Extracts the non-transition eye diagram data from the SigTest tools as $V_{TX-DE-EMPH-PP}$.

3 Calculates de-emphasis ratio using the following formula:

De-emphasis ratio: $-20*\log_{10}(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$

4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX\text{-}DIFF\text{-}p\text{-}p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

The **Peak Differential Input Voltage** test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the standard specifications.

$V_{RX\text{-}DIFFp\text{-}p} = 2*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 42 Peak Differential Output Voltage (Transition) -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.800 V	1.00 V

Table 43 Peak Differential Output Voltage (Transition) -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX\text{-}DIFF\text{-}p\text{-}p}$	Peak Differential Output Voltage	0.800 V	1.00 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
   b. Sets the value of **Nominal Data Rate** as **5.0 GT/s**.
   c. Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the transition bits eye top and bases.
5. Finds the differential value between the transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Extracts the transition eye diagram data from the SigTest tools.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTest tools.
3. Compares the measured peak differential output/input voltage (transition) value to the compliance test limits.
4. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}, Min(V_{DIFF(i)}))$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.6, Table 8-6.

Table 44 Peak Differential Output Voltage (Non-Transition) -3.5 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DIFF-p-p}$	Peak Differential Output Voltage	0.4765 V	1.00 V

Table 45 Peak Differential Output Voltage (Non-Transition) -6.0 dB Test Details

Symbol	Description	Min	Max
$V_{TX-DIFF-p-p}$	Peak Differential Output Voltage	0.3374 V	1.00 V

Understanding the Test Flow - Using Infiniium Measurement Method

NOTE

This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
    a. Sets the value of **Clock Recovery Method** as **First Order PLL**. However, when SSC signals are used, sets the value of **Clock Recovery Method** as **Second Order PLL** with **Damping Factor** of **0.707**.
    b. Sets the value of **Nominal Data Rate** as **5.0 GT/s** depending on the data rate.
    c. Sets the value of **Loop Bandwidth** as **5.0 MHz** for **5.0 GT/s.**
3. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
4. Measures the non-transition bits eye top and bases.
5. Finds the differential value between the non-transition bits eye top and base using **Histogram**.
6. Reports the measurement results.

Understanding the Test Flow - Using SigTest Measurement Method

NOTE This test by default runs with **SigTest**. However, it can be run with **Infiniium** as well. Please select the required **Voltage Test Measurement Method** in the **Configure** tab.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Extracts the non-transition eye diagram data from the SigTest tools.
2 Gets largest non-transition amplitude (outer eye), smallest non-transition amplitude (inner eye) test results from SigTest tools.
3 Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

28 Reference Clock Tests, 5.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 5.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

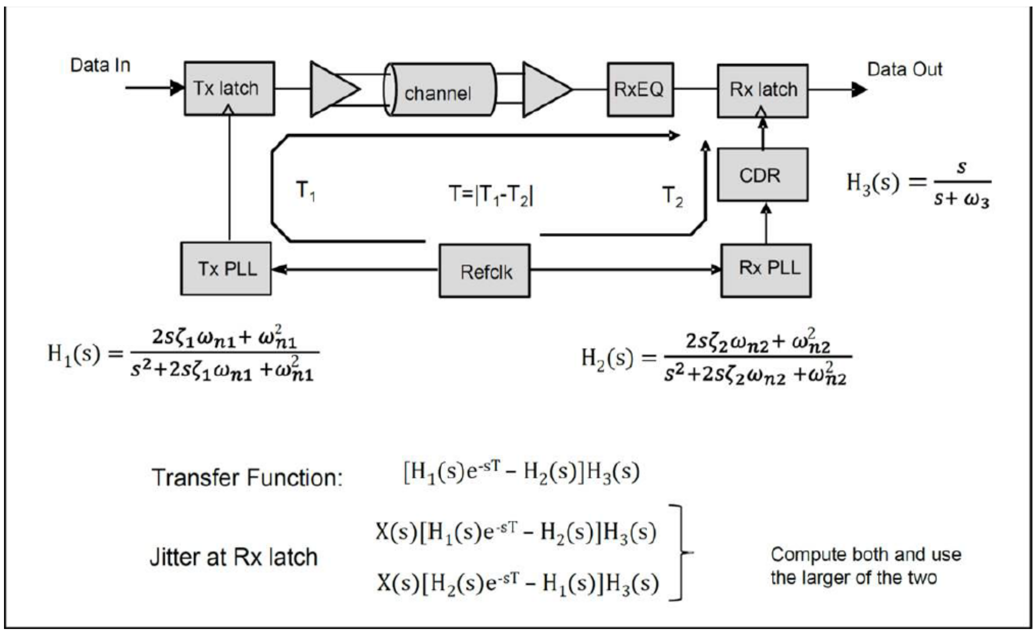
NOTE **It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.**

Reference Clock Architectures

For 5.0 GT/s, PCI-E 6.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 5 GT/s

PLL #1	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(min)$ = 5.0 MHz	ω_{n1}= 1.12 Mrad/s ζ_1 = 14	ω_{n1}= 11.01 Mrad/s ζ_1 = 1.16
$BW_{PLL}(max)$ = 16 MHz	ω_{n1}= 3.58 Mrad/s ζ_1 = 14	ω_{n1}= 35.26 Mrad/s ζ_1 = 1.16

PLL #2	0.01 dB peaking	3.0 dB peaking
$BW_{PLL}(min)$ = 8.0 MHz	ω_{n2}= 1.79 Mrad/s ζ_2 = 14	ω_{n2}= 26.86 Mrad/s ζ_2 = 0.54
$BW_{PLL}(max)$ = 16 MHz	ω_{n2}= 3.58 Mrad/s ζ_2 = 14	ω_{n2}= 53.73 Mrad/s ζ_2 = 0.54

$BW_{CDR}(min)$ = 5 MHz, 1st order

64 combinations

5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73

PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15

BW_{CDR}(min) = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC | CDR

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

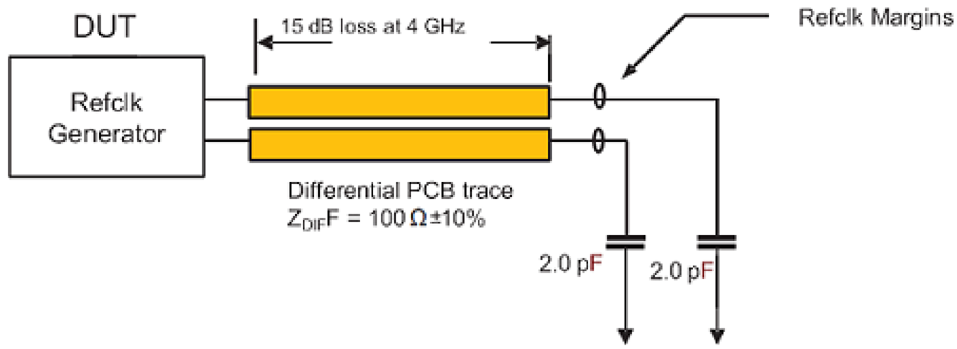


Figure 40 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 5.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

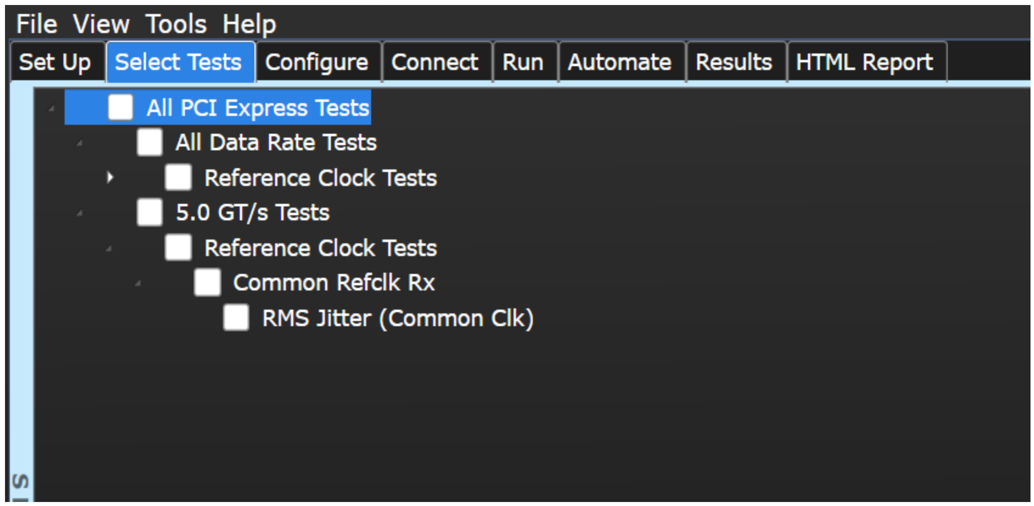


Figure 41 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK\text{-}RMS\text{-}CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 46 RMS Jitter Test Details

Symbol	Description	Value
$T_{REFCLK\text{-}RMS\text{-}CC}$	RMS Refclk jitter for common Refclk architecture	3.1 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

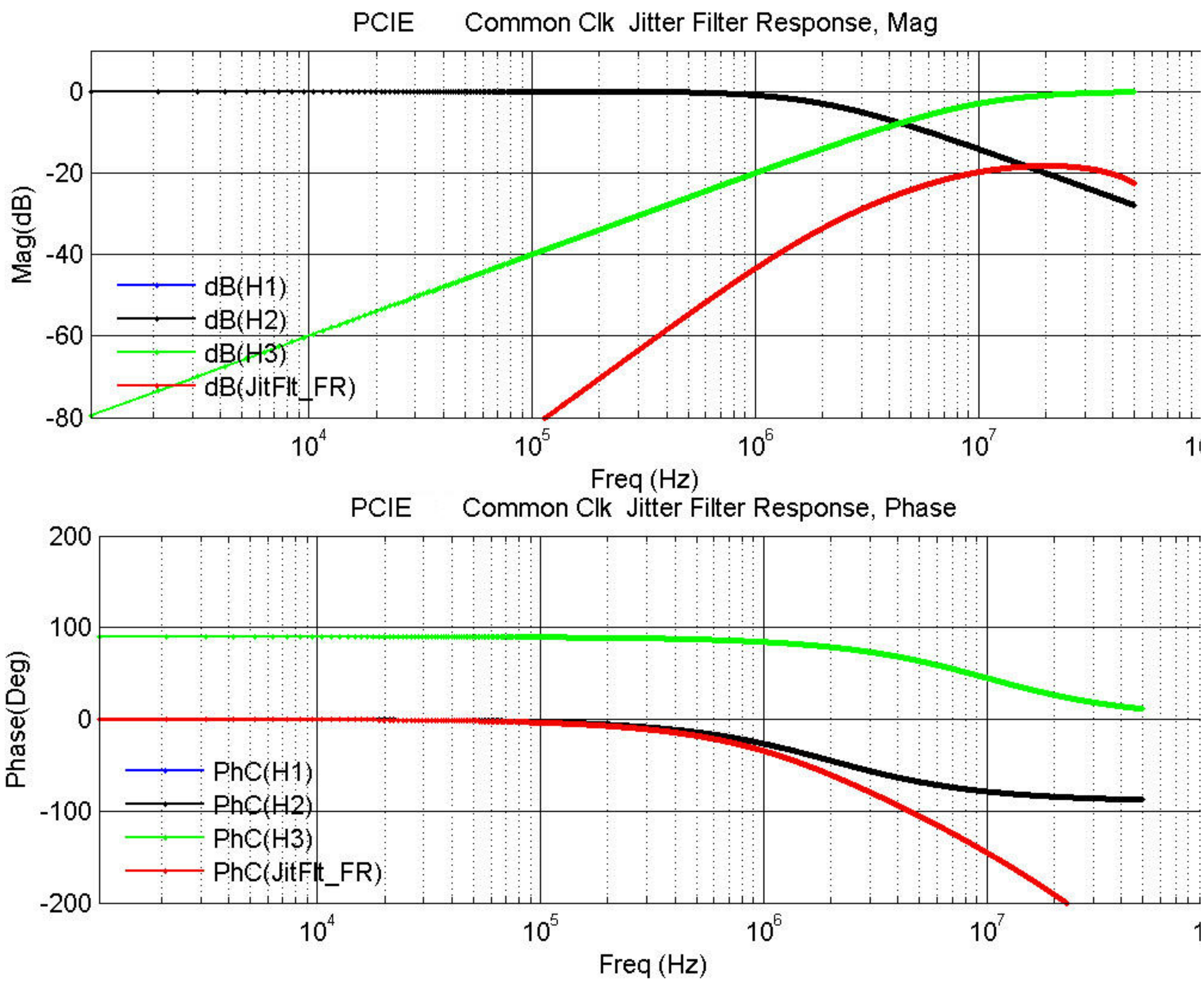


Figure 42 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

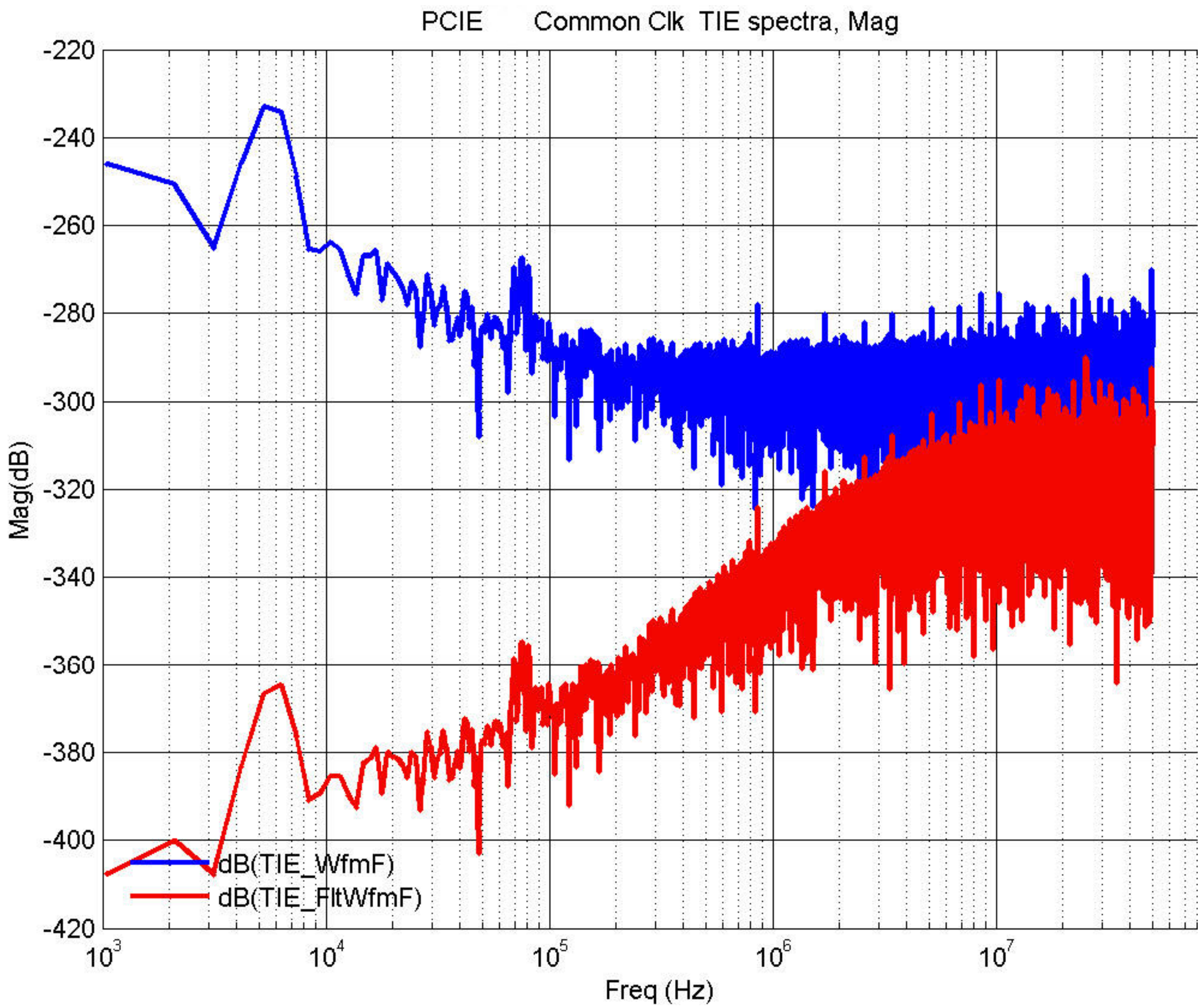


Figure 43 Reference Image for Common Clock TIE Spectra RMS Jitter Test

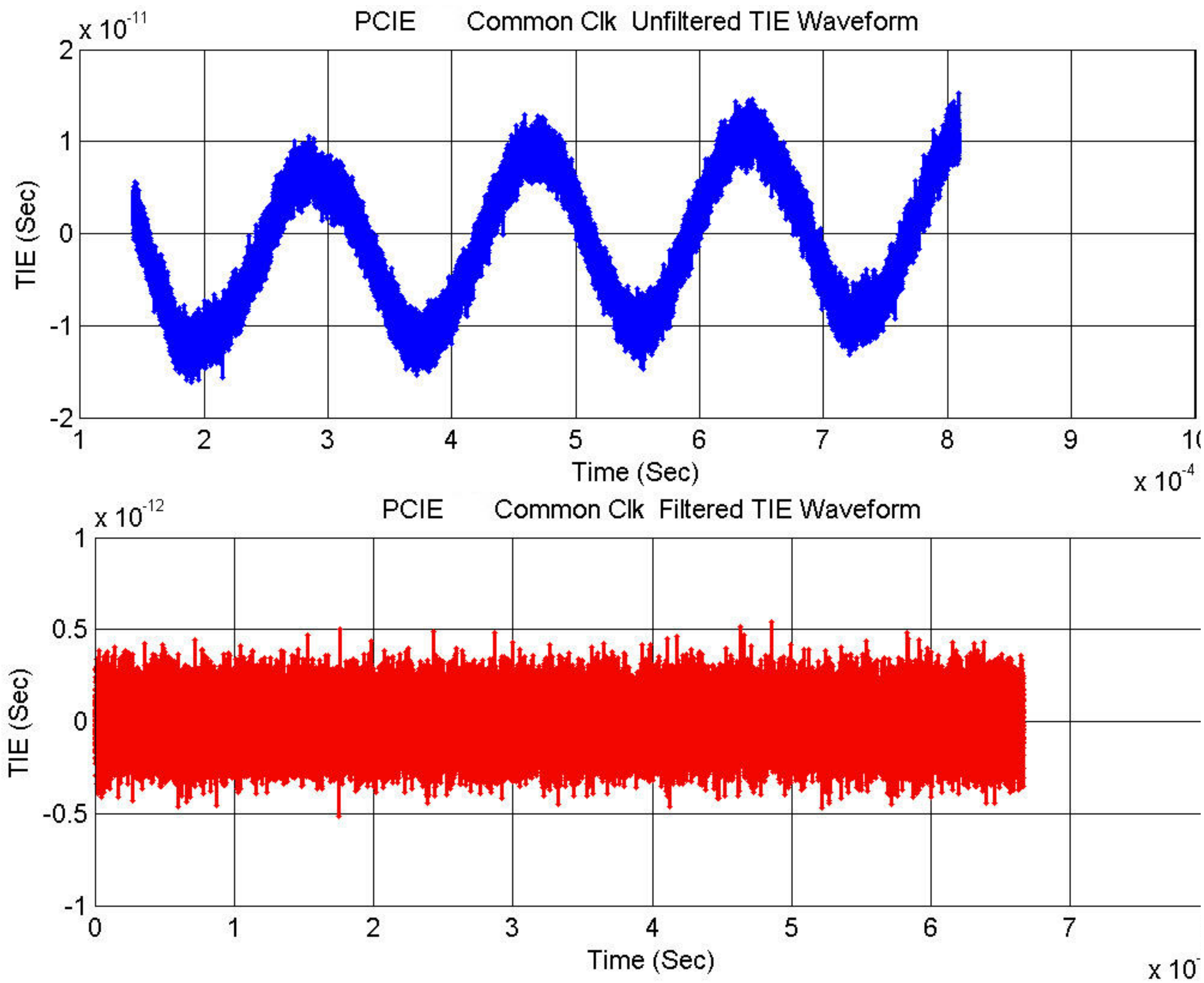


Figure 44 Reference Image for TIE Waveform RMS Jitter Test

Part XI
PCI-Express Gen6 8.0 GT/s Tests

29 Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 8.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

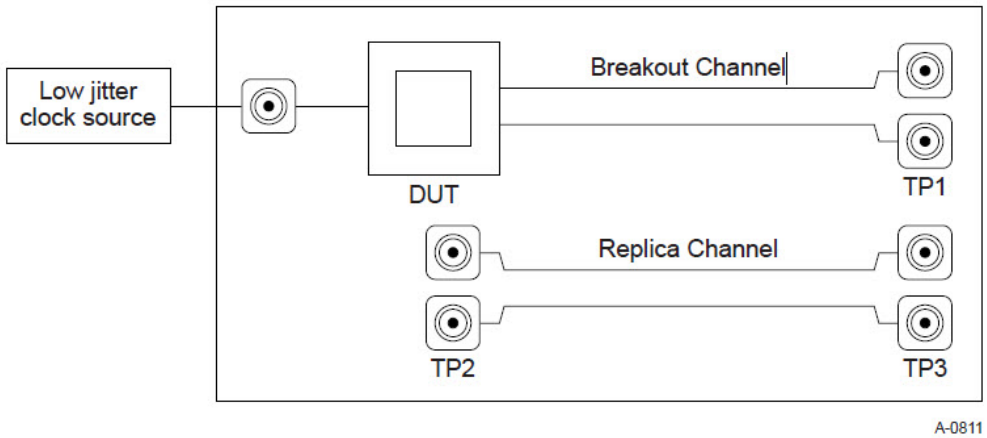


Figure 45 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 8.0 GT/s Tests > Transmitter (Tx) Tests**.

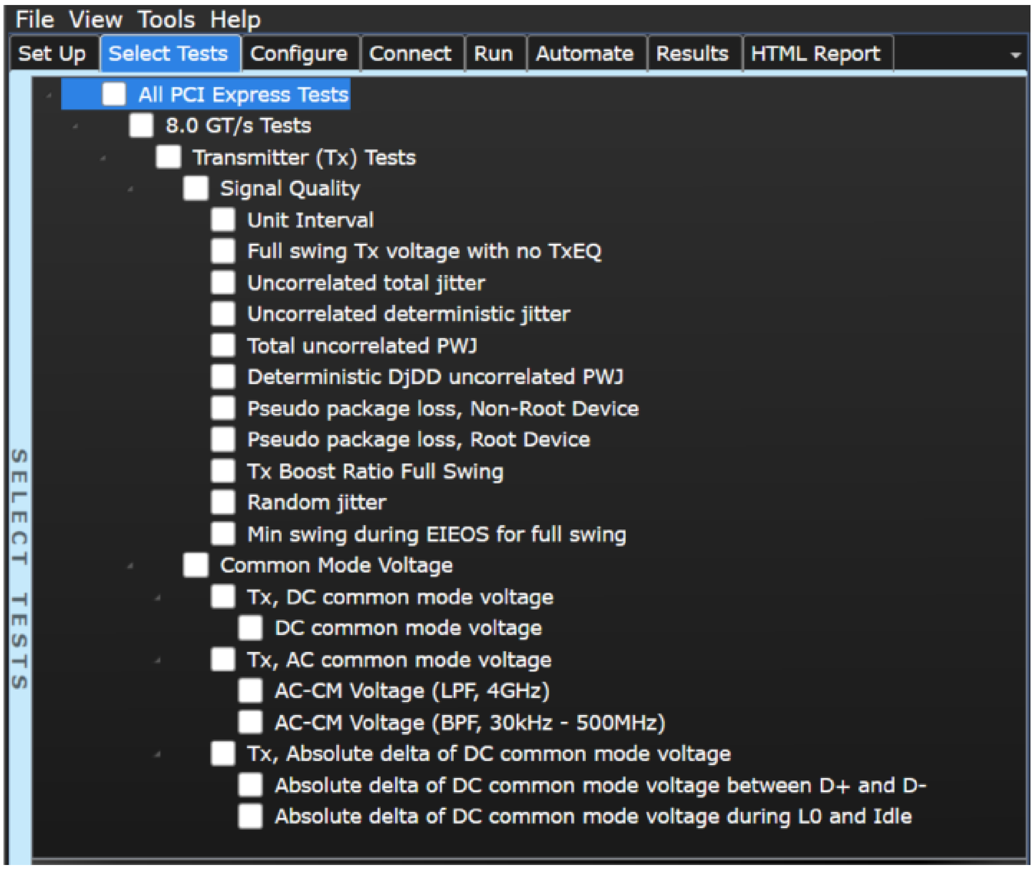


Figure 46 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 47 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	Clean Clock: 124.9625 ps	Clean Clock 125.0375 ps
		SSC: 124.9625 ps	SSC: 125.6603 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 6.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

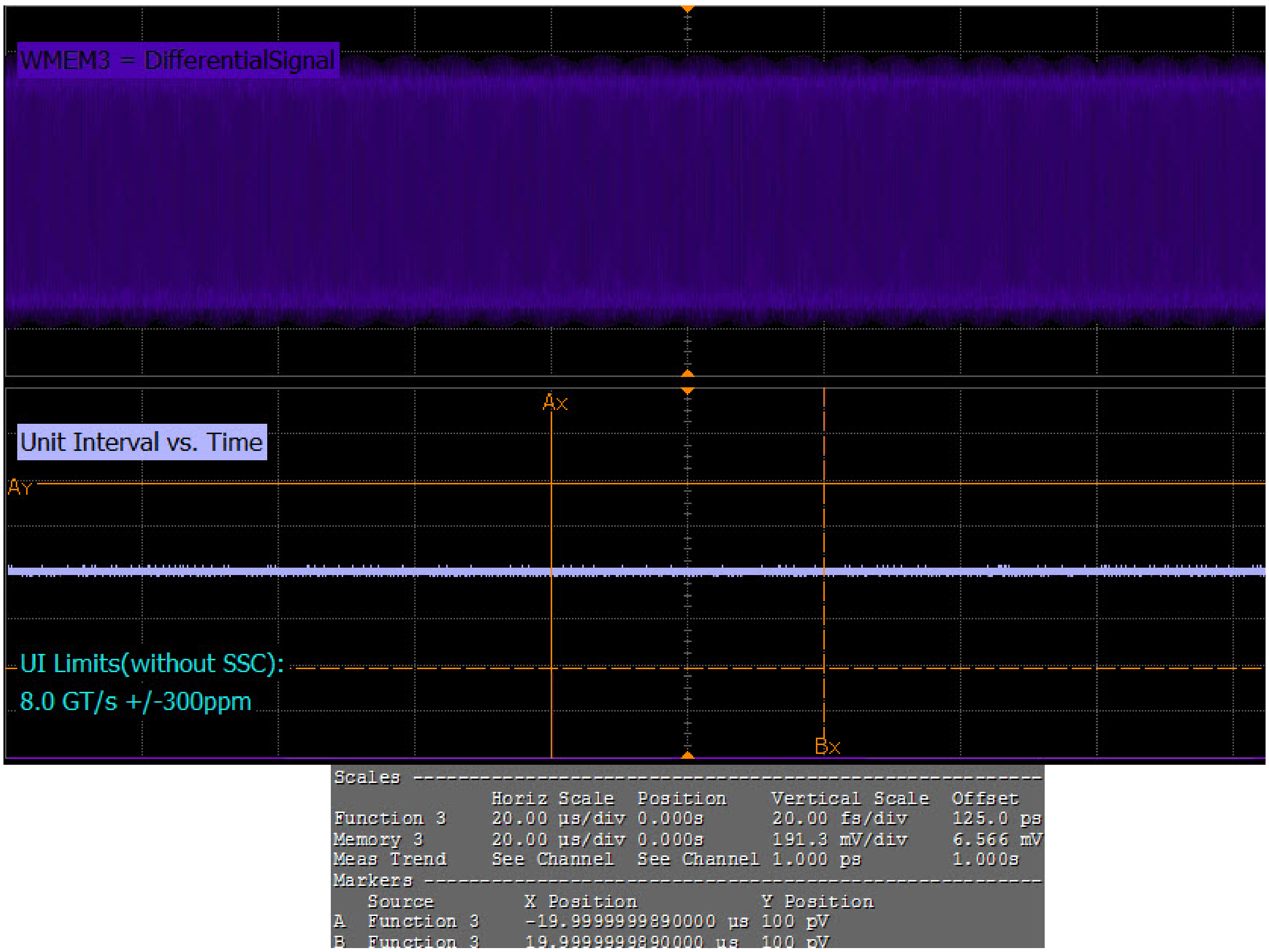


Figure 47 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 48. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP}$ is used as reference to check the compliance of the DUT.

Table 48 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEQ	800 mV_{PP}	1.0 V_{PP}

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times |V_{TXD+} - V_{TXD-}|$
- See section 8.3.3.6 and section 8.3.3.7 for measurement details.

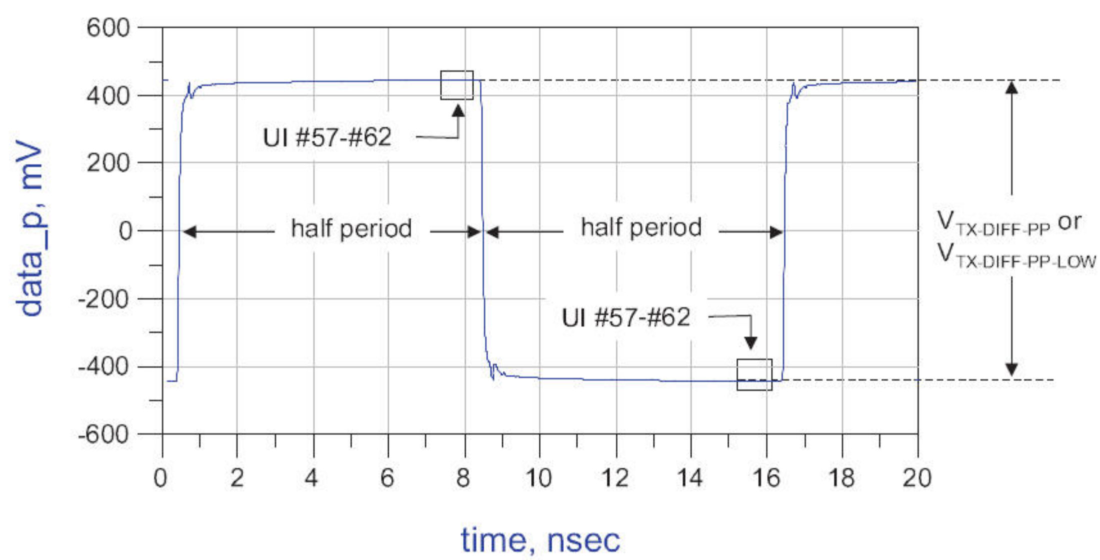


Figure 48 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 49. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 49 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mV_{PP}	1 V_{PP}

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as 2 × | V_{TXD+}-V_{TXD-}|
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

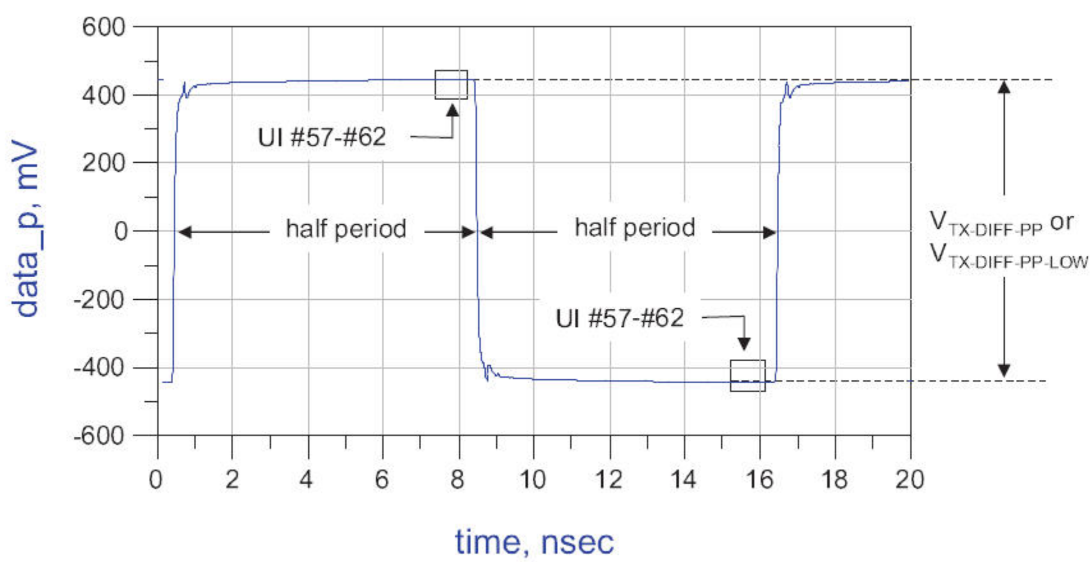


Figure 49 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE**
> Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

> **NOTE**
> Base - Transmitter Tests:
> MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 50 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	27.55 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the RJ RMS jitter value.
8. Reports the peak total jitter value.
9. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 51 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	12 ps PP

Test Definition Notes from the Specification

See section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 52 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	24 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 53 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	10 ps PP

Test Definition Notes from the Specification

- See section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak deterministic DjDD uncorrelated PWJ value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V111) against a 1010 pattern (V101). Tx package loss measurement is made with c-1 and c+1 both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V101 and V111. Multiple measurements shall be made and averaged to obtain stable values for V101 and V111. Due to the HF content of V101, ps21 TX measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V101 and V111 is made towards the end of each interval to minimize ISI and low frequency effects. V101 is defined as the peak-peak voltage between minima and maxima of the clock pattern. V111 is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 54 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	3.0 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	3.0 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.

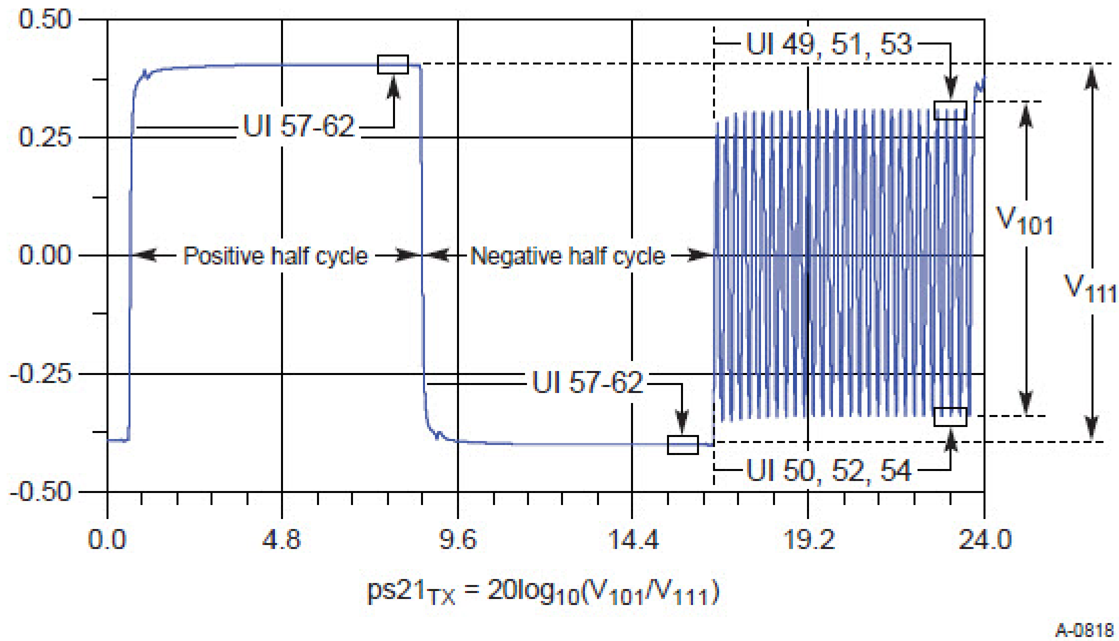


Figure 50 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX\text{-}BOOST\text{-}FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 55 Tx Boost Ratio Full Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}BOOST\text{-}FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P10.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P10 signal in *.bin format.
13 Inputs the P10 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P10.
15 Reports the measurement of Vb during preset values P10 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 56 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 6.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test (Information Only)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 57 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.17 - 1.97 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 58 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}FS}$	Min swing during EIEOS for full swing	250 mV_{PP}

Test Definition Notes from the Specification

$V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

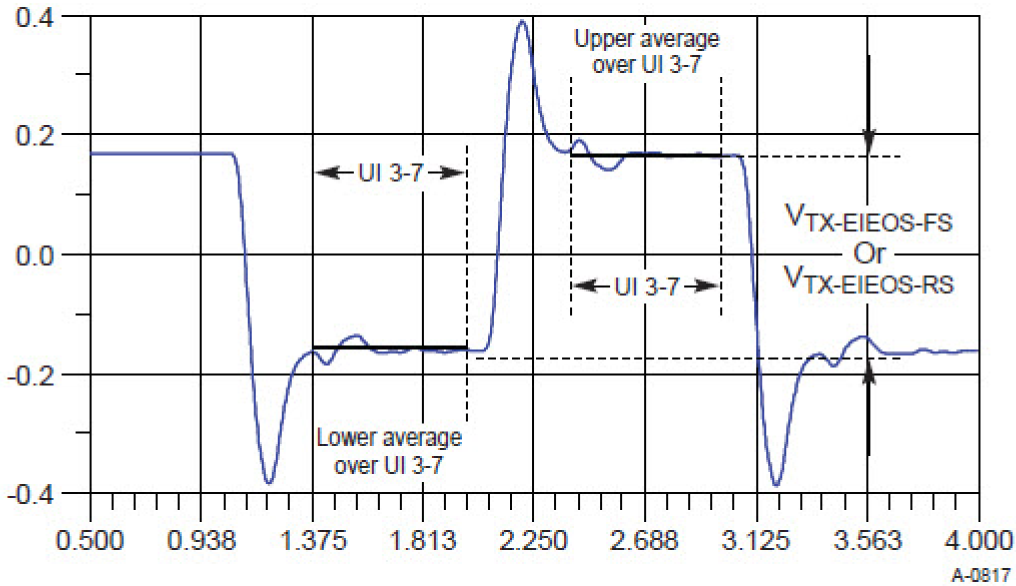


Figure 51 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTestWrapper tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 59 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

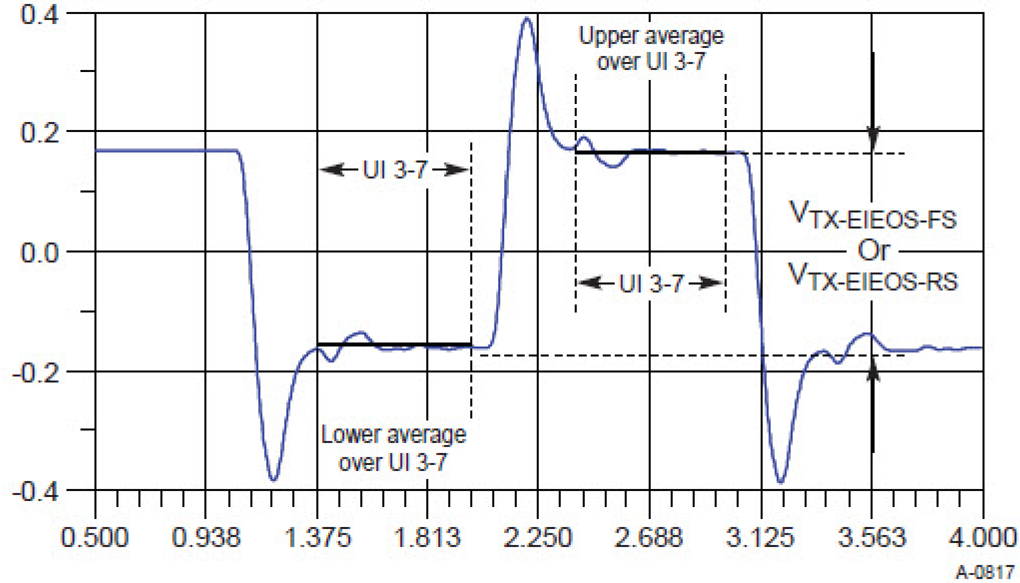


Figure 52 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 60 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 8.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 61 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 8.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 62 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 8.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC df/dt (Max) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 63 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a. Generates a differential plot (x_n - x_{n-1}).
   b. The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

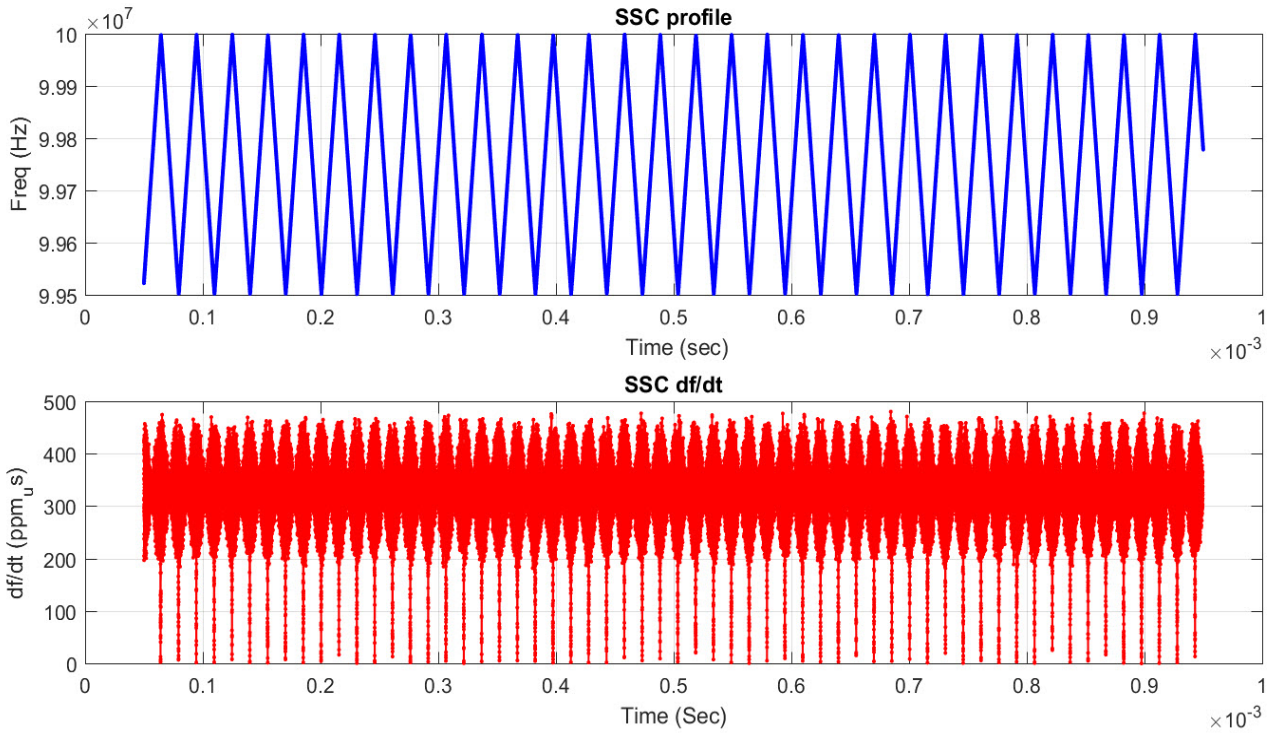


Figure 53 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-DC-}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 64 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

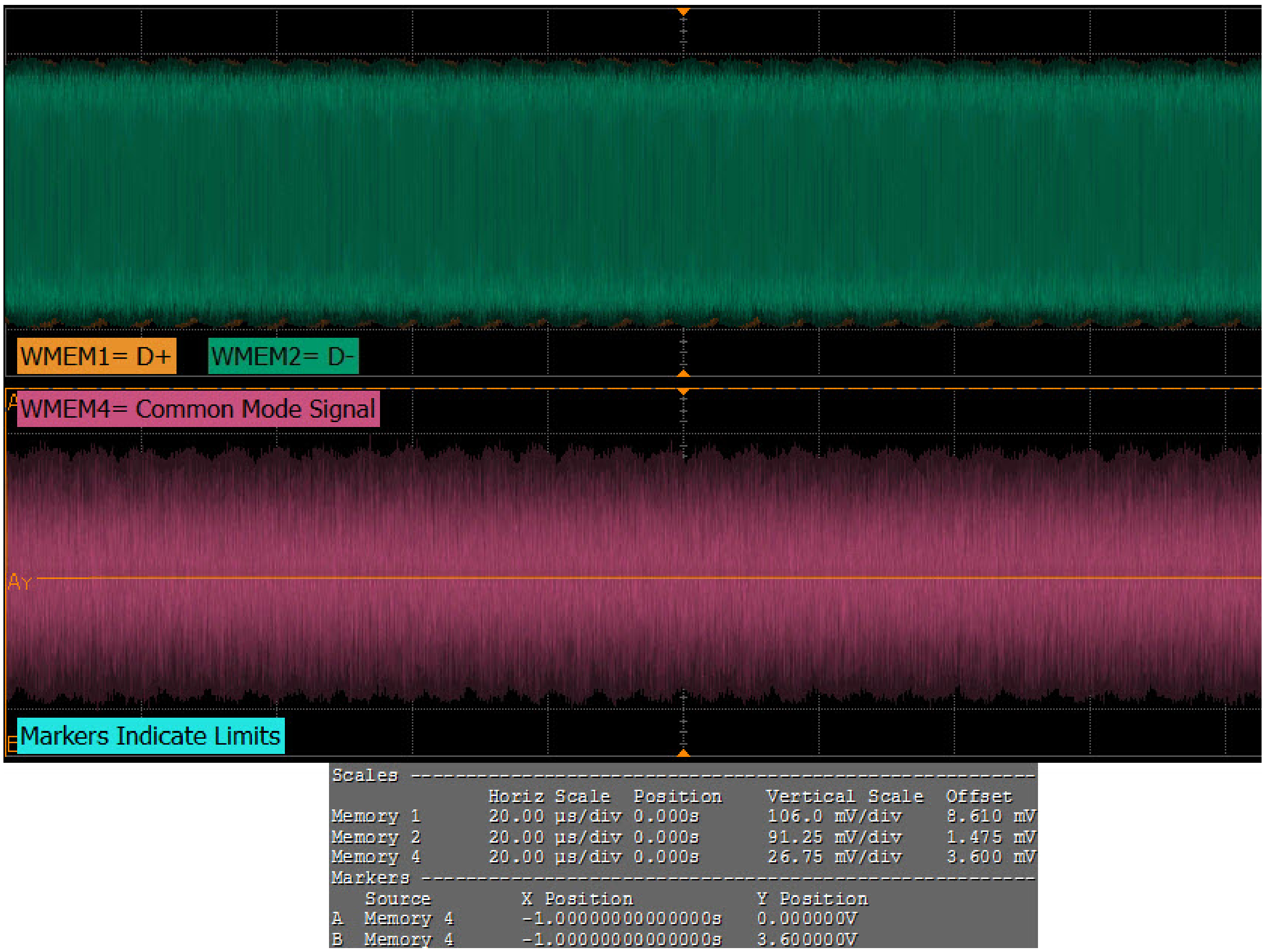


Figure 54 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 4 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 65 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mV_{PP}

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

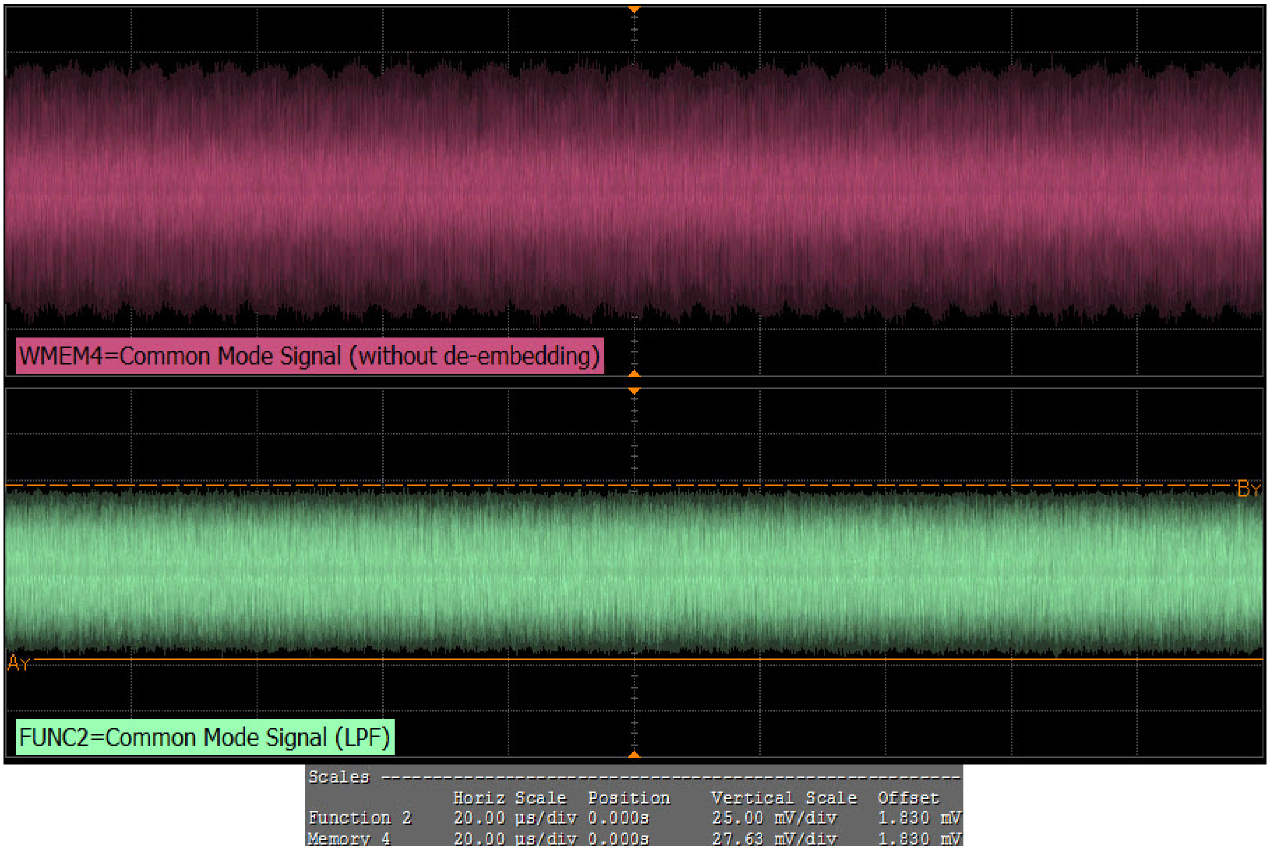


Figure 55 Reference Image for AC-CM voltage (4GHz LPF) Test

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 66 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	50 mV_{PP}

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 4 GHz) test.

1 Gets PCIE6 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

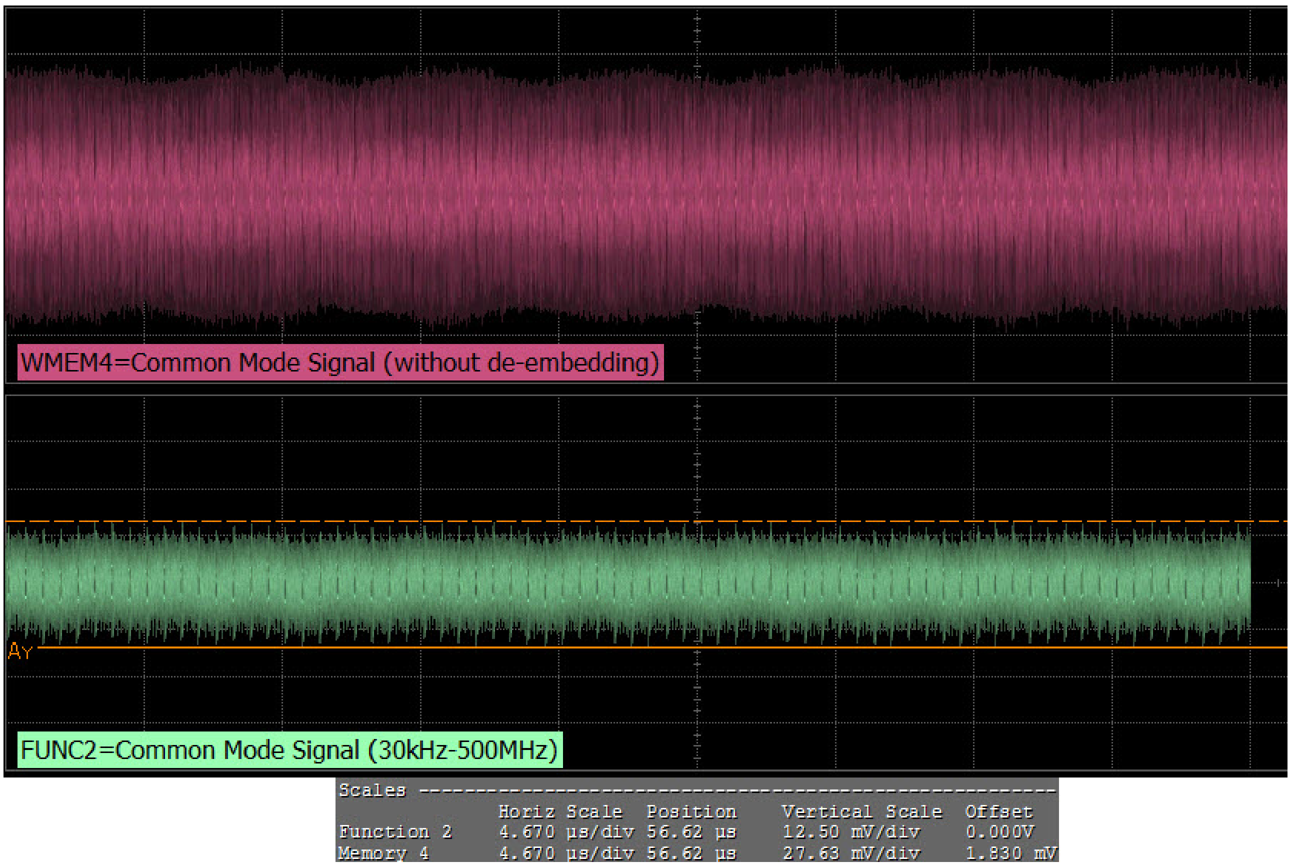


Figure 56 Reference Image for AC-CM voltage (30KHz - 500MHz) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25$ mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 67 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Test Definition Notes from the Specification

$| V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-\ [during\ L0]} | \leq 25$mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $| V_{TX\text{-}D+\ [during\ L0]} |$

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $| V_{TX\text{-}D-\ [during\ L0]} |$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
- DC Common Mode Line Delta
- Average DC value of D+
- Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 68 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Test Definition Notes from the Specification

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

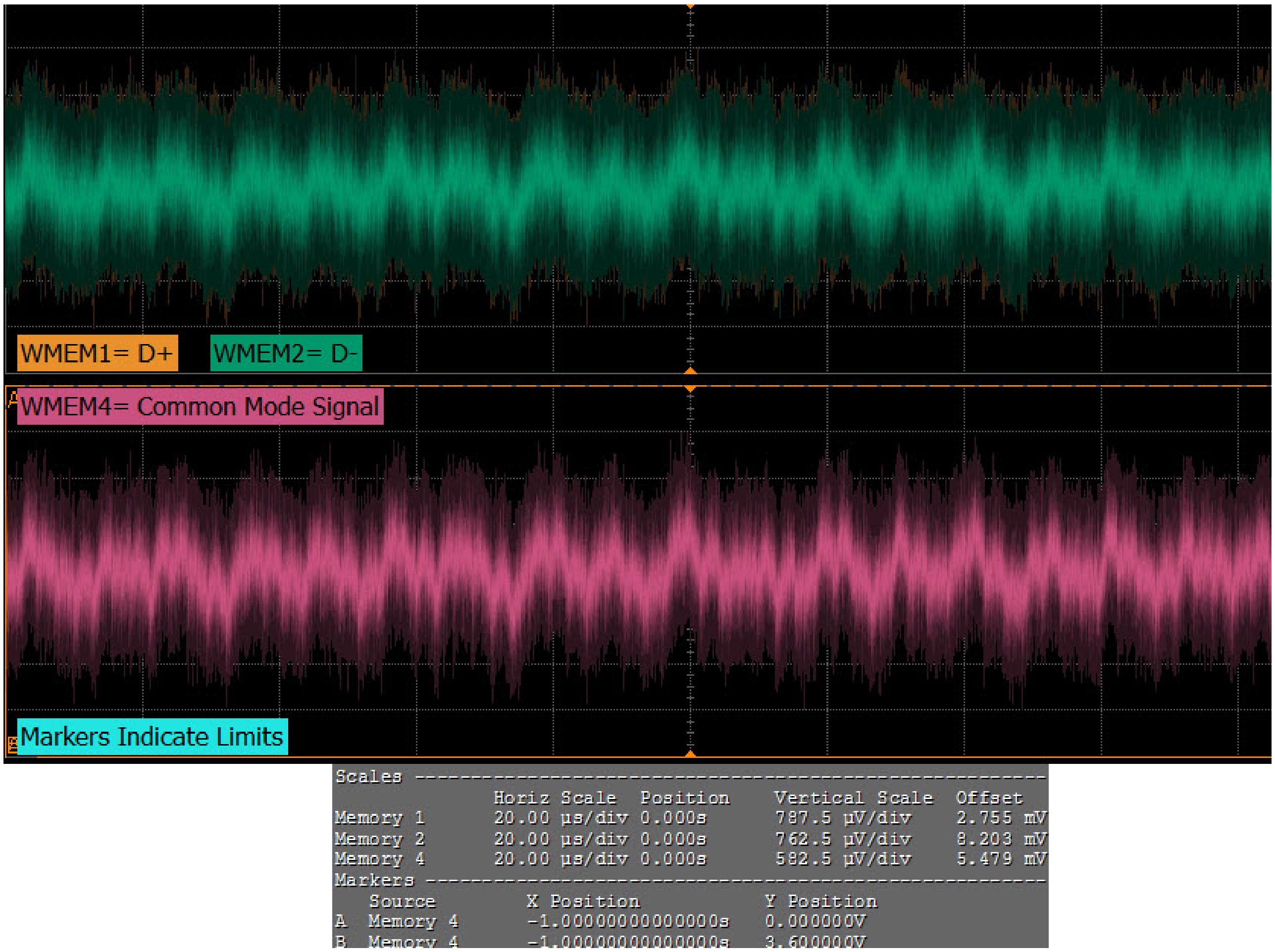


Figure 57 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to "Equalization Presets Tests".

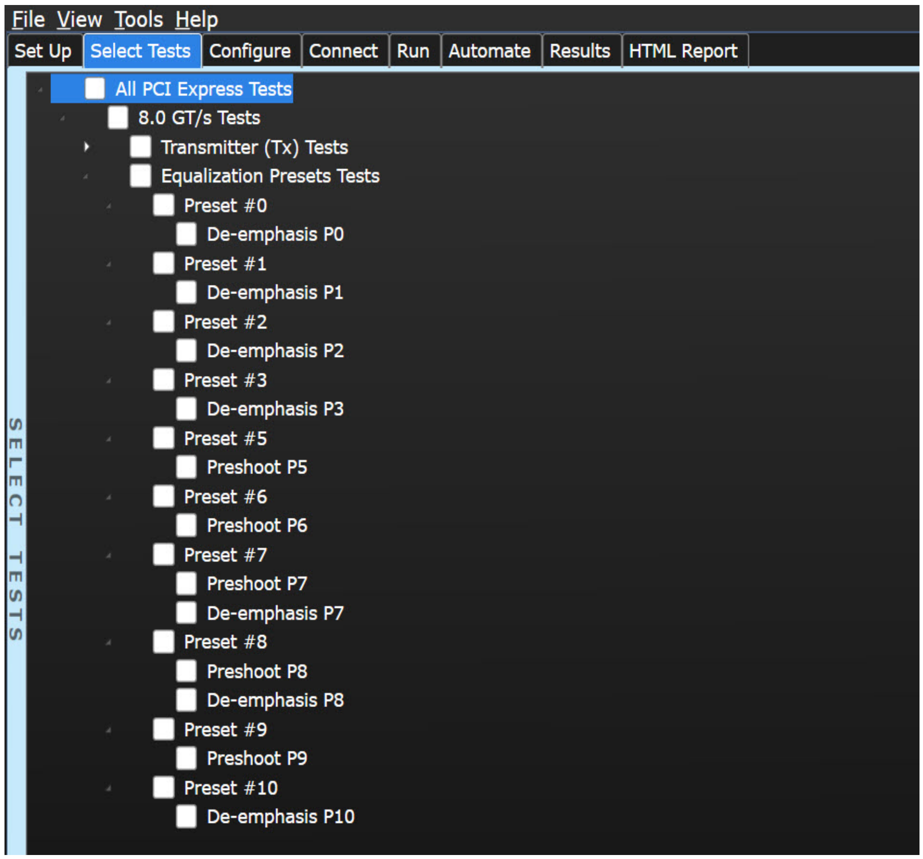


Figure 58 Selecting Equalization Presets Tests

Preset #0 Measurement (P0), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 69 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

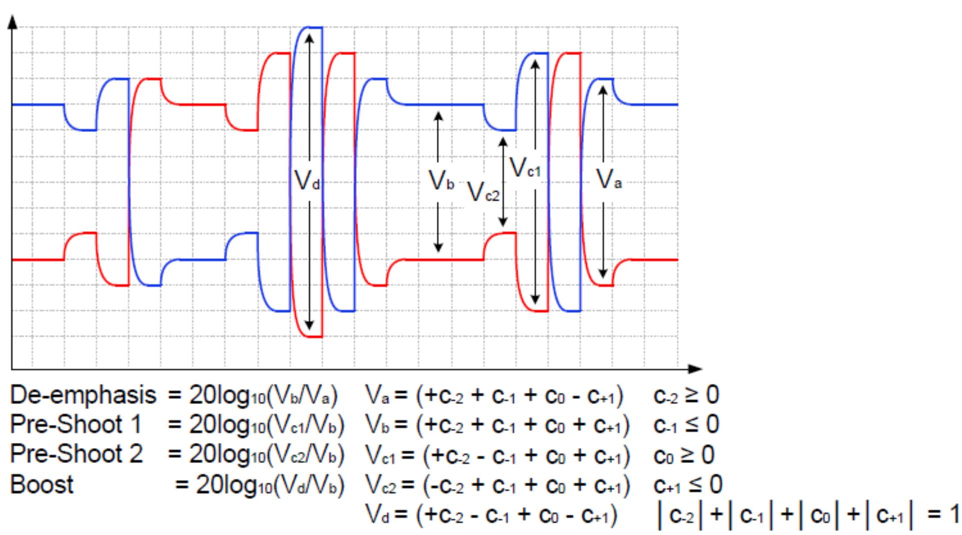


Figure 59 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 70 Preset P0 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P0	0.0	0.0 ±1 dB	–6.0 ± 1.5 dB	0.000	0.000	–0.250	1.000	0.500	0.500	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P0.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P0 signal in *.bin format.

12 Inputs the P4 and P0 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P0.

14 Reports the measurement of Vb during preset values P0 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (P1), De-emphasis Test

This test verifies that the de-emphasis of the preset number P1 is within the conformance limits as specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 71 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

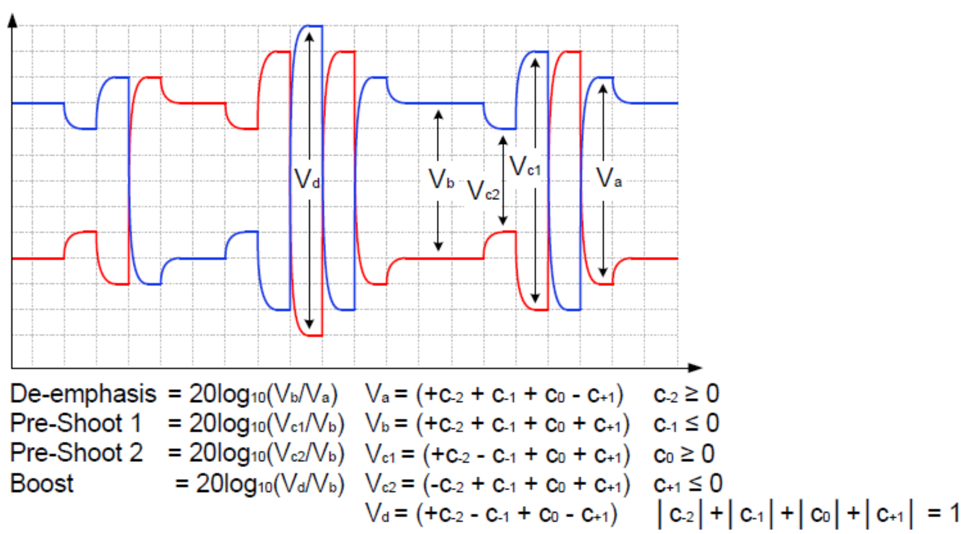


Figure 60 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 72 Preset P1 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P1	0.0	0.0 ±1 dB	–3.5 ± 1 dB	0.000	0.000	–0.167	1.000	0.666	0.666	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P1.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P1 signal in *.bin format.
12. Inputs the P4 and P1 saved waveform into SigTest tool.
13. Computes the de-emphasis at preset value P1.
14. Reports the measurement of Vb during preset values P1 and P4.
15. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis Test

This test verifies that the de-emphasis of the preset number P2 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 73 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

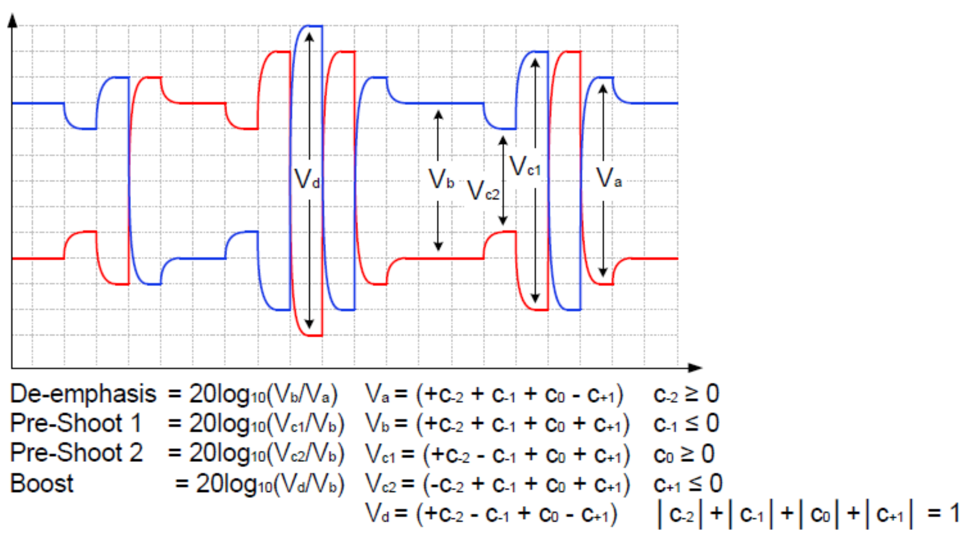


Figure 61 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 74 Preset P2 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P2	0.0	0.0 ±1 dB	-4.4 ±1.5 dB	0.000	0.000	-0.200	1.000	0.600	0.600	0.600

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain** Scale to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P2.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P2 signal in *.bin format.

12 Inputs the P4 and P2 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P2.

14 Reports the measurement of Vb during preset values P2 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis Test

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 75 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

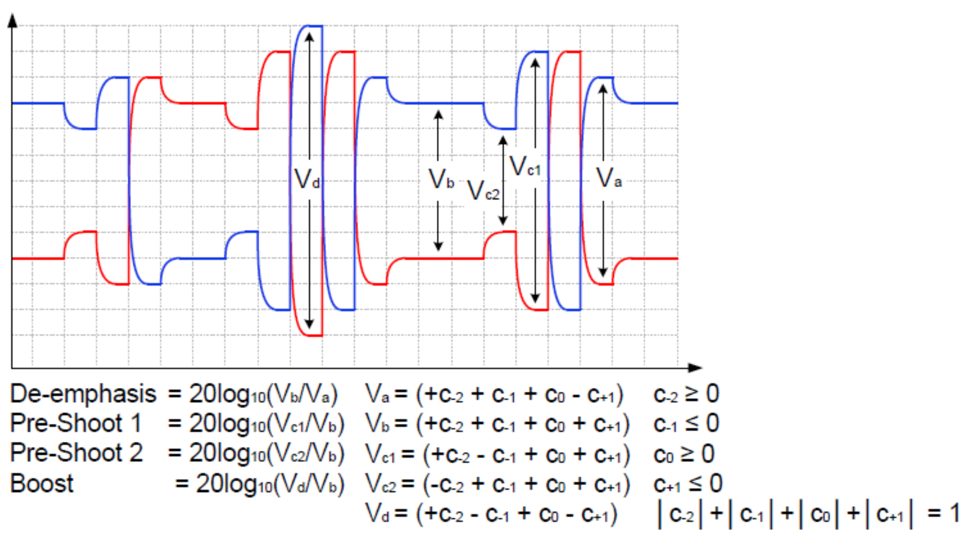


Figure 62 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 76 Preset P3 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P3	0.0	0.0 ±1 dB	-2.5 ±1 dB	0.000	0.000	-0.125	1.000	0.750	0.750	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P3.
14 Reports the measurement of Vb during preset values P4 and P3.
15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot Test

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 77 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

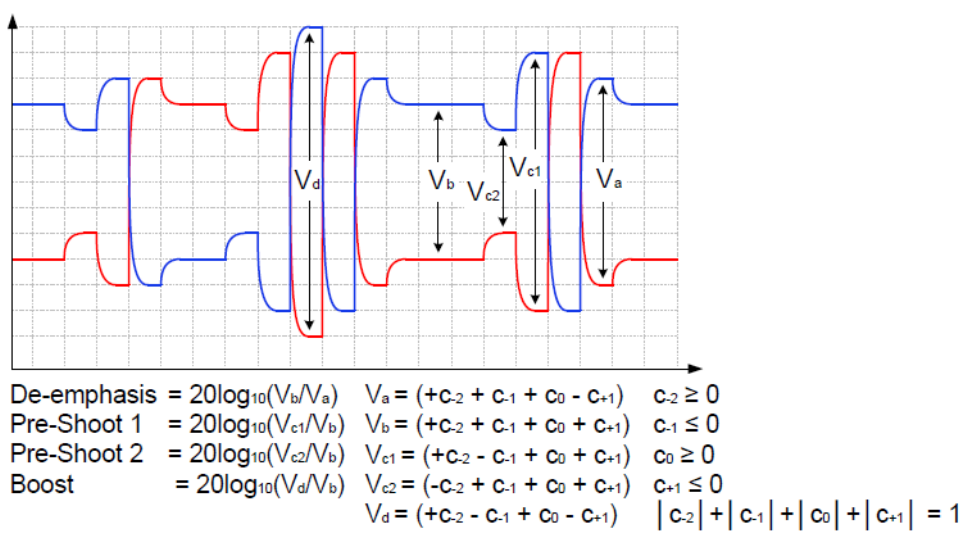


Figure 63 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 78 Preset P5 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P5	0.0	1.9 ±1 dB	0.0 ±1 dB	0.000	-0.100	0.000	0.800	0.800	1.000	0.800

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P5.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of vs, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P5 signal in *.bin format.

12 Inputs the P4 and P5 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P5.

14 Reports the measurement of Vb during preset values P4 and P5.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

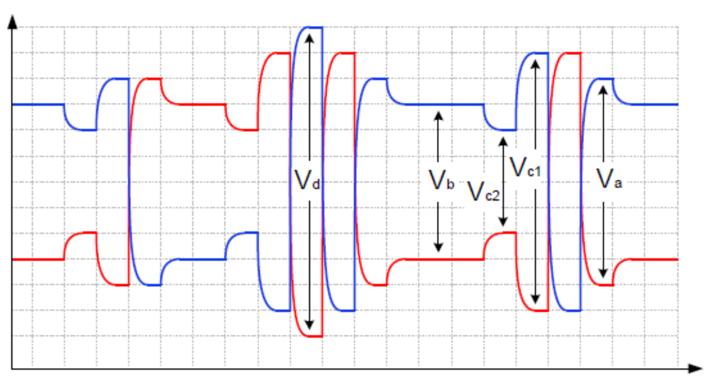
Preset #6 Measurement (P6), Preshoot Test

This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 79 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 64 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 80 Preset P6 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P6	0.0	2.5 ±1 dB	0.0 ±1 dB	0.000	-0.125	0.000	0.750	0.750	1.000	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate in preset value #P6.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P6 signal in *.bin format.
12. Inputs the P4 and P6 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P6.
14. Reports the measurement of Vb during preset values P6 and P4.
15. Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

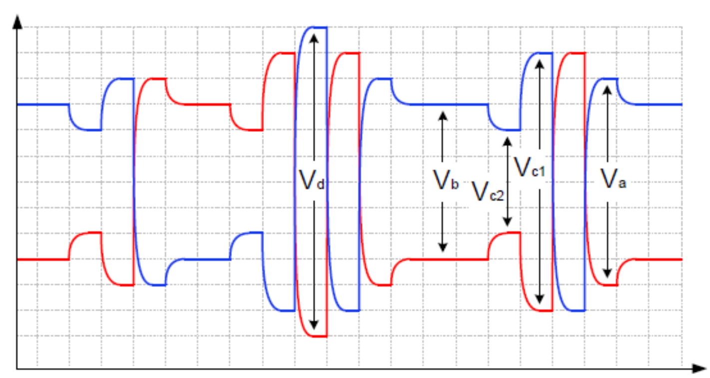
Preset #7 Measurement (P7), Preshoot Test

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 81 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \quad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \quad c_{-2} \ge 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \quad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \quad c_{-1} \le 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \quad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \quad c_0 \ge 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \quad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \quad c_{+1} \le 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \quad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 65 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 82 Preset P7 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P7	0.0	3.5 ±1 dB	-6.0 ±1.5 dB	0.000	-0.100	-0.200	0.800	0.400	0.600	0.400

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P2.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P2 signal into *.bin format.
7. Configures the DUT to operate in preset value #P7.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9. Sets the **Horizontal Domain Scale** to 20.0 µs.
10. Fits and displays all sample data on screen.
11. Saves the P7 signal in *.bin format.
12. Inputs the P2 and P7 saved waveform into SigTest tool.
13. Computes the preshoot at preset value P7.
14. Reports the measurement of Vb during preset values P2 and P7.
15. Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis Test

This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 83 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

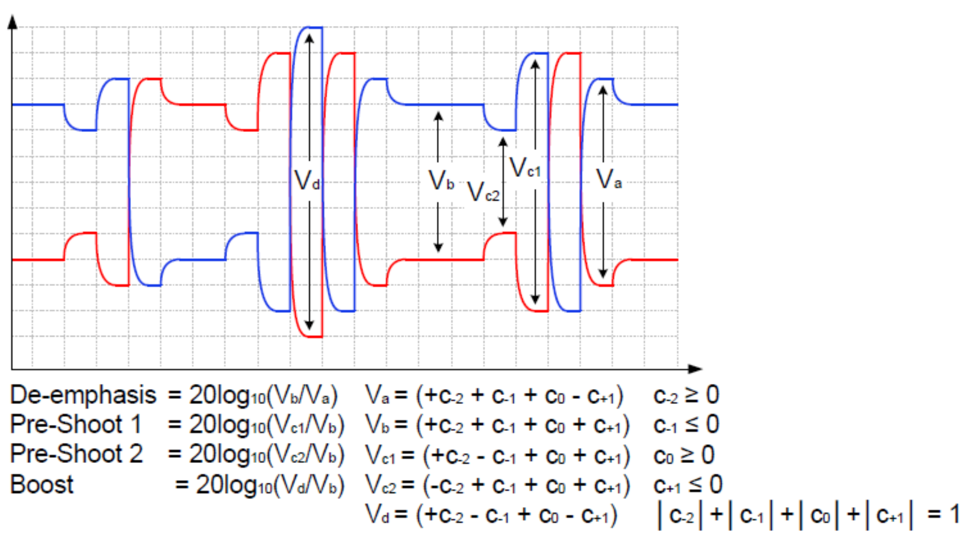


Figure 66 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 84 Preset P7 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P7	0.0	3.5 ±1 dB	-6.0 ±1.5 dB	0.000	-0.100	-0.200	0.800	0.400	0.600	0.400

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P5.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P5 signal into *.bin format.

7 Configures the DUT to operate in preset value #P7.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P7 signal in *.bin format.

12 Inputs the P5 and P7 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P7.

14 Reports the measurement of Vb during preset values P5 and P7.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot Test

This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 85 **Preset Measurement Cross Reference Table**

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

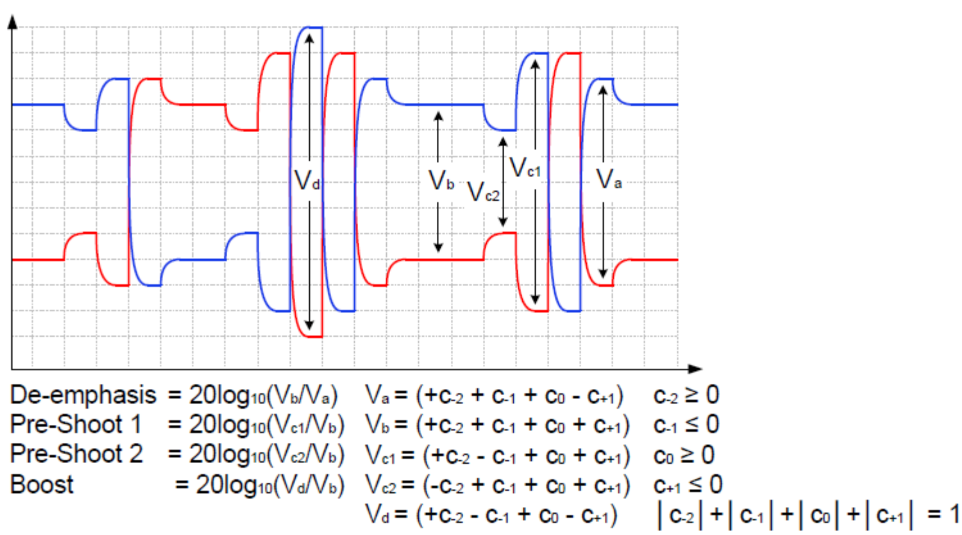


Figure 67 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 86 Preset P8 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P8	0.0	6.0 ±1.0 dB	-3.5 ±1 dB	0.000	-0.125	-0.125	0.750	0.500	0.750	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P3.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P3 signal into *.bin format.

7 Configures the DUT to operate in preset value #P8.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P8 signal in *.bin format.

12 Inputs the P3 and P8 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P8.

14 Reports the measurement of Vb during preset values P3 and P8.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis Test

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 87 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

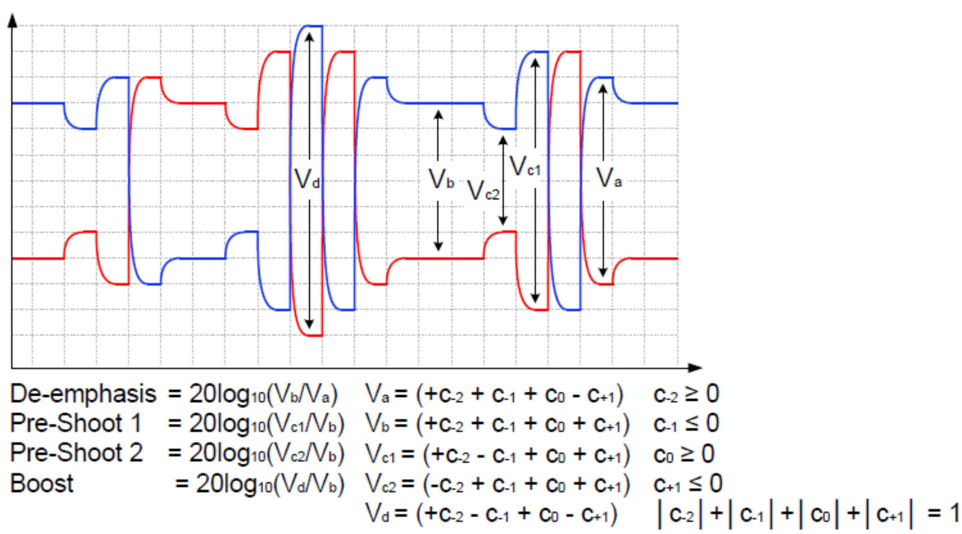


Figure 68 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 88 Preset P8 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P8	0.0	3.5 ±1 dB	-3.5 ±1 dB	0.000	-0.125	-0.125	0.750	0.500	0.750	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P6.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P6 signal into *.bin format.

7 Configures the DUT to operate in preset value #P8.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P8 signal in *.bin format.

12 Inputs the P6 and P8 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P8.

14 Reports the measurement of Vb during preset values P6 and P8.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot Test

This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 89 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

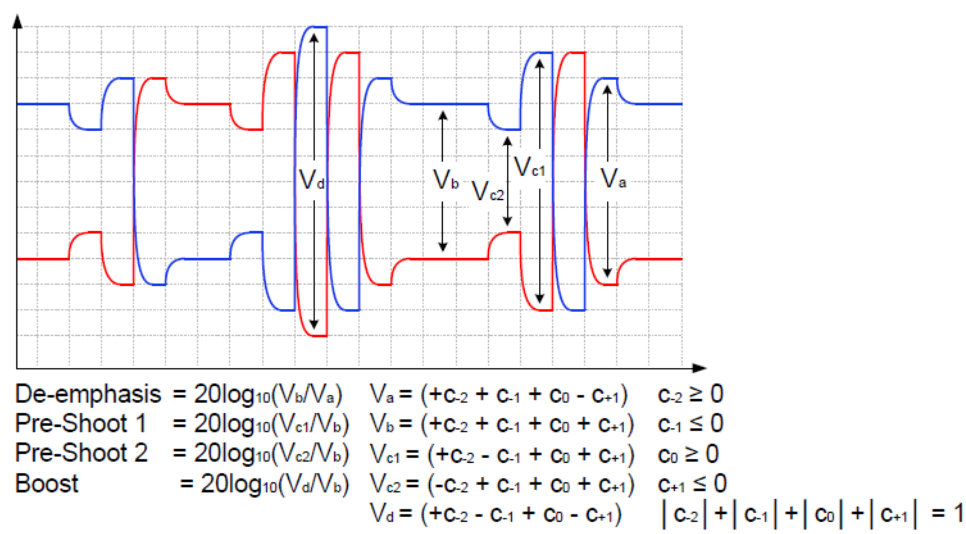


Figure 69 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 90 Preset P9 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P9	0.0	3.5 ±1 dB	0.0 ± 1 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P9.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P9 signal in *.bin format.

12 Inputs the P4 and P9 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P9.

14 Reports the measurement of Vb during preset values P9 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis Test

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in PCIE Base Specification.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 91 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

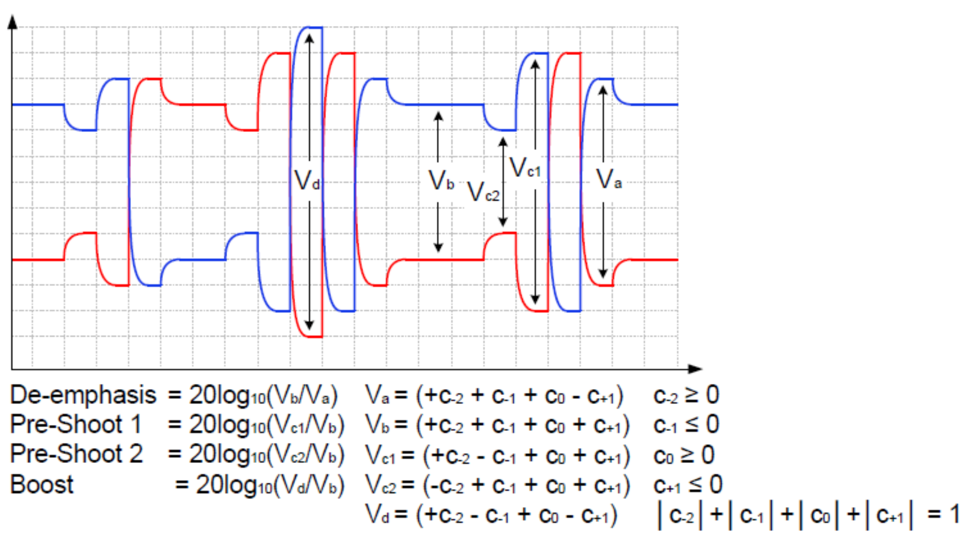


Figure 70 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 92 Preset P10 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P10	0.0	0.0 ±1 dB	Note 2	0.000	0.000	Note2	1.000	Note2	Note2	Note2

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.9 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P10 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P10.
14 Reports the measurement of Vb during preset values P10 and P4.
15 Compares the de-emphasis value to the compliance test limits.

> **NOTE** Base - Transmitter Tests:
> MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

30 Reference Clock Tests, 8.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 8.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

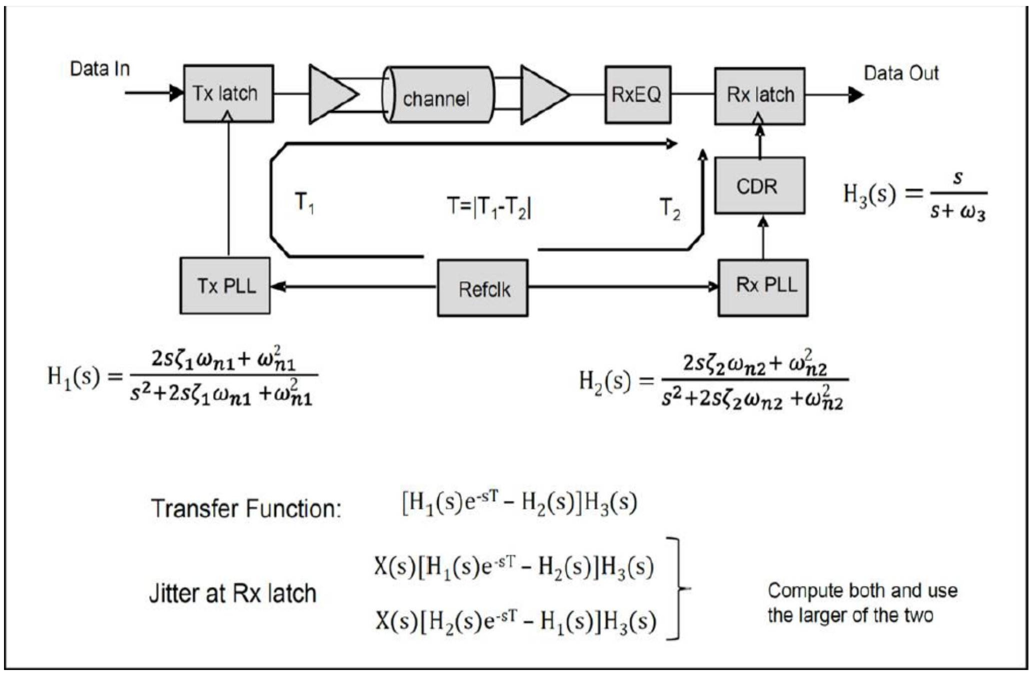
NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 8.0 GT/s, PCI-E 6.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

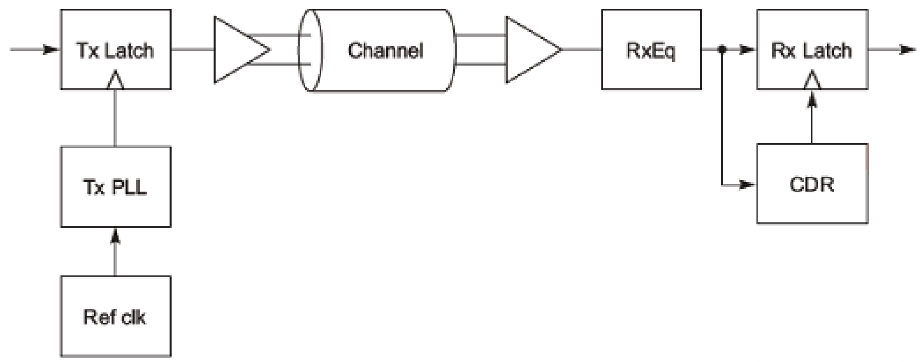
Common Clock Architecture

This section describes the common Refclk Rx architecture.



Data Clock Architecture

This section describes the data driving architecture.



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1}^2 + \omega_{n1}^2}\right] \qquad H_3(s) = \left[\frac{2s\zeta_3\omega_{n3} + \omega_{n3}^2}{s^2 + 2s\zeta_3\omega_{n3}^2 + \omega_{n3}^2}\right]$$

$$H(s) = H_1(s)[1 - H_3(s)]$$

	0.01 dB Peaking	2.0 dB Peaking
$BW_{PLL}(min) =$ 2.0 MHz	$\omega_{n1} = 0.448$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 6.02$ Mrad/s $\zeta_1 = 0.73$
$BW_{PLL}(max) =$ 4.0 MHz	$\omega_{n1} = 0.896$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 12.04$ Mrad/s $\zeta_1 = 0.73$

	0.01 dB Peaking	1.0 dB Peaking
$BW_{PLL}(min) =$ 2.0 MHz	$\omega_{n2} = 0.448$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 4.62$ Mrad/s $\zeta_2 = 1.15$
$BW_{PLL}(max) =$ 5.0 MHz	$\omega_{n2} = 1.12$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 11.53$ Mrad/s $\zeta_2 = 1.15$

	0.5 dB Peaking	2.0 dB Peaking
$BW_{CDR}(min) =$ 10 MHz	$\omega_{n3} = 16.57$ Mrad/s $\zeta_3 = 1.75$	$\omega_{n3} = 33.8$ Mrad/s $\zeta_3 = 0.73$

A-0843

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

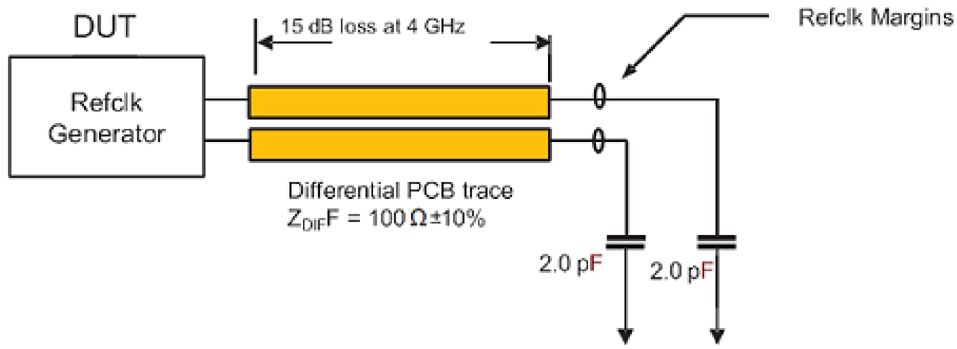


Figure 71 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 8.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

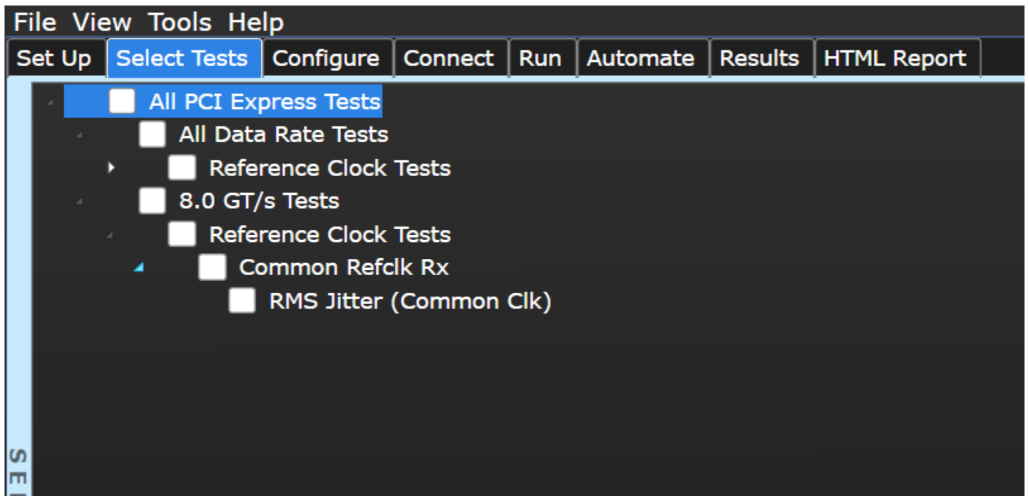


Figure 72 Selecting Reference Clock Tests when Clean Clock or SSC is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 93 RMS Jitter Test Details

Symbol	Description	Value
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	1.0 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal frequency is ~100 MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

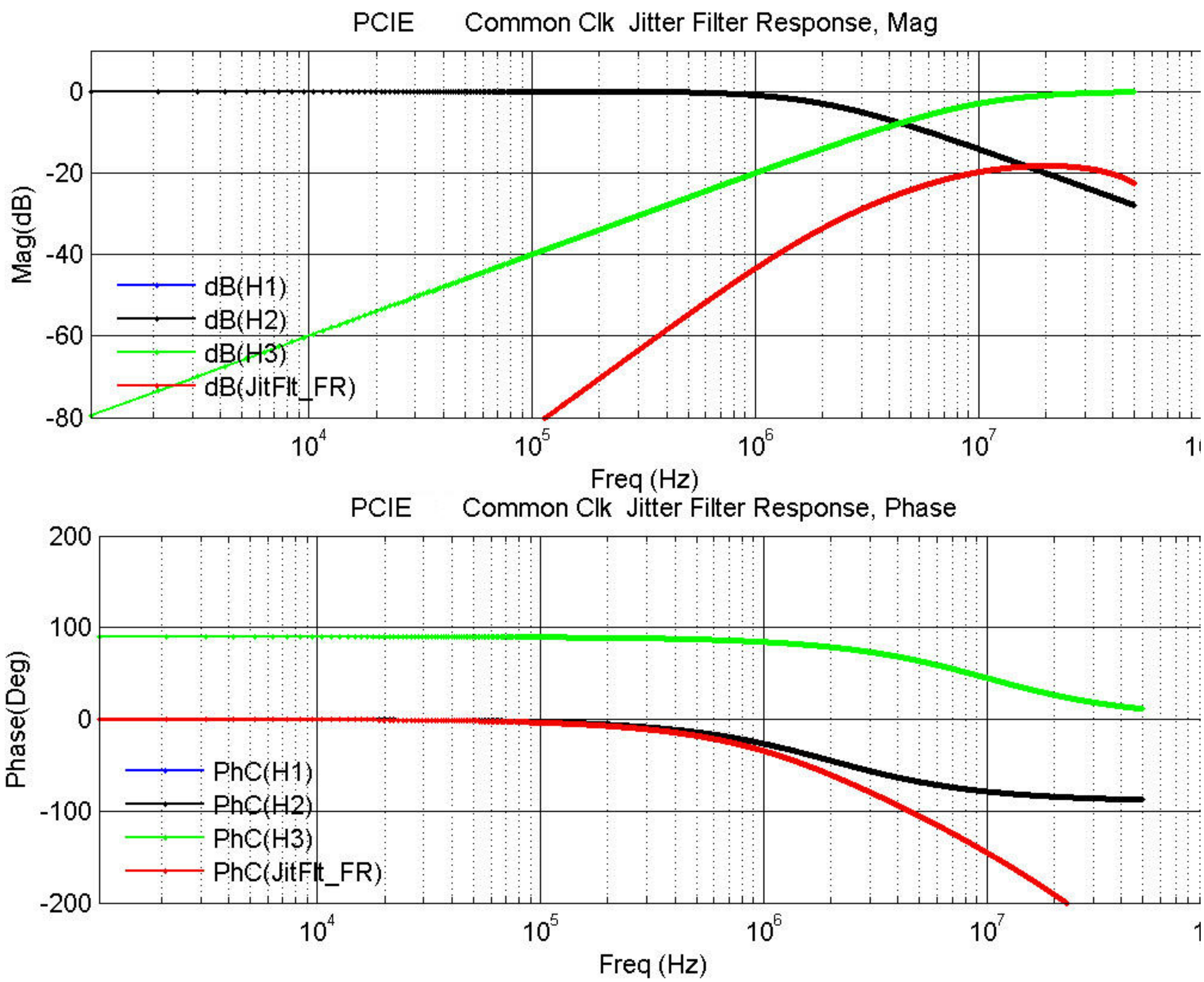


Figure 73 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

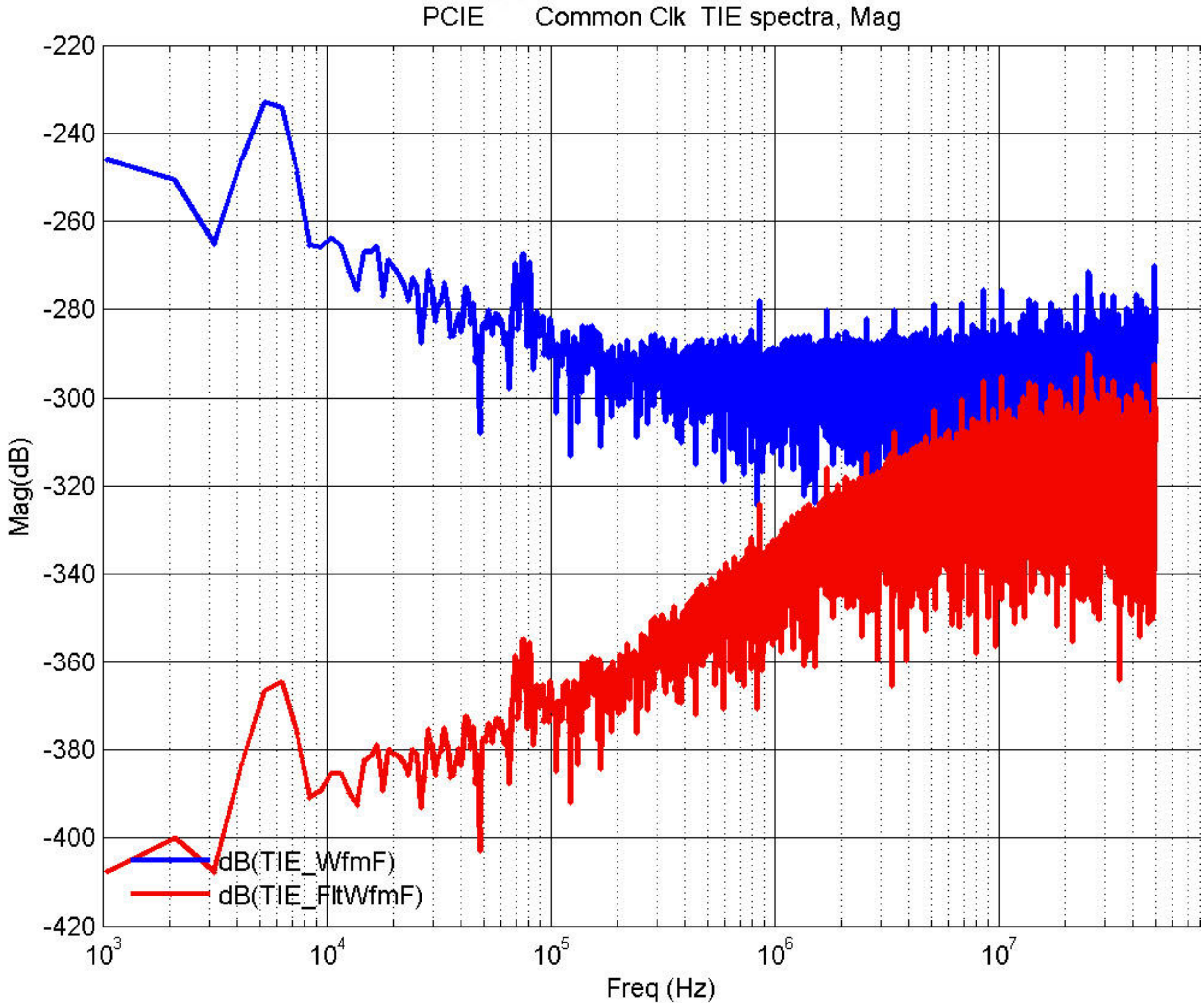


Figure 74 Reference Image for Common Clock TIE Spectra RMS Jitter Test

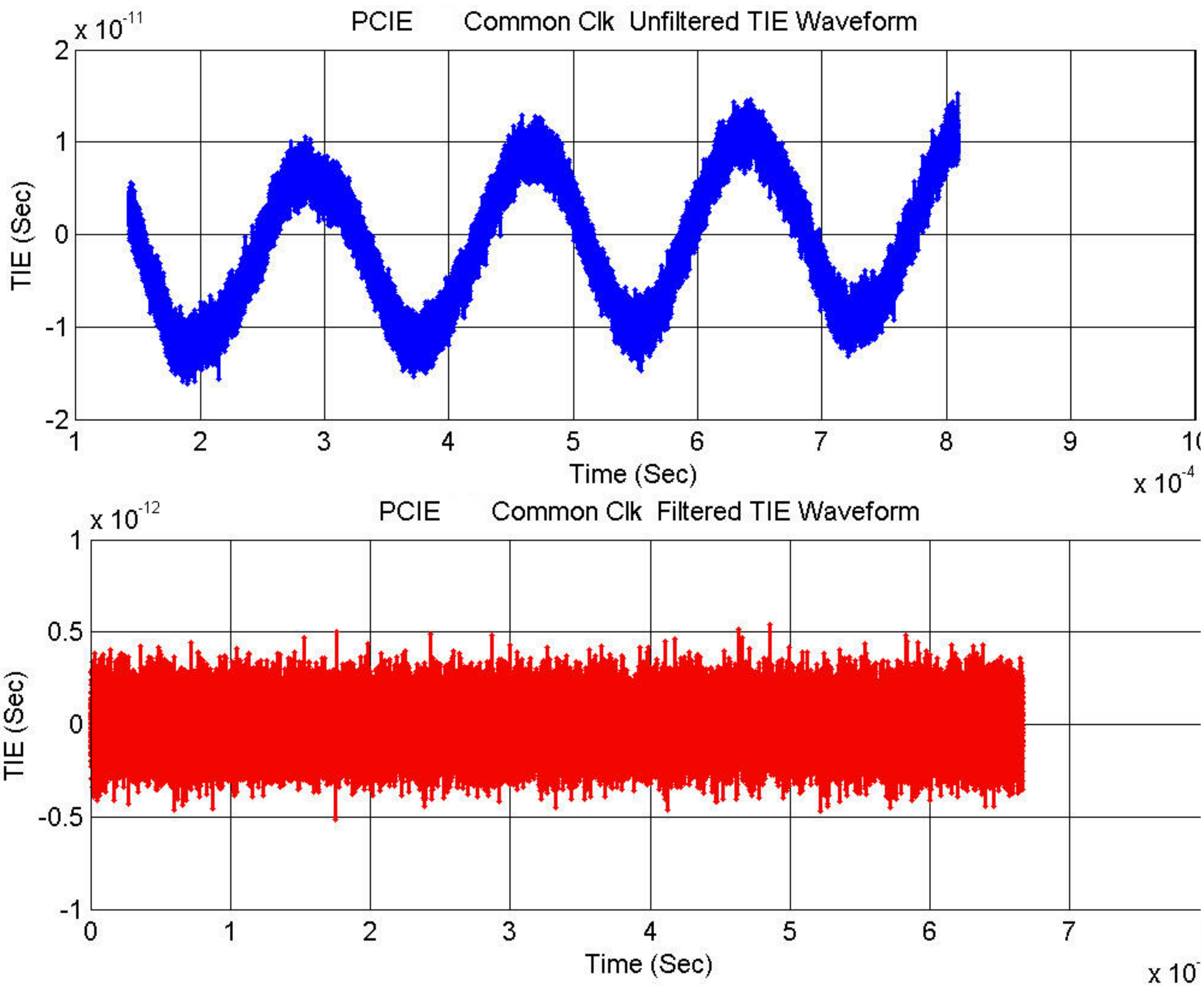


Figure 75 Reference Image for TIE Waveform RMS Jitter Test

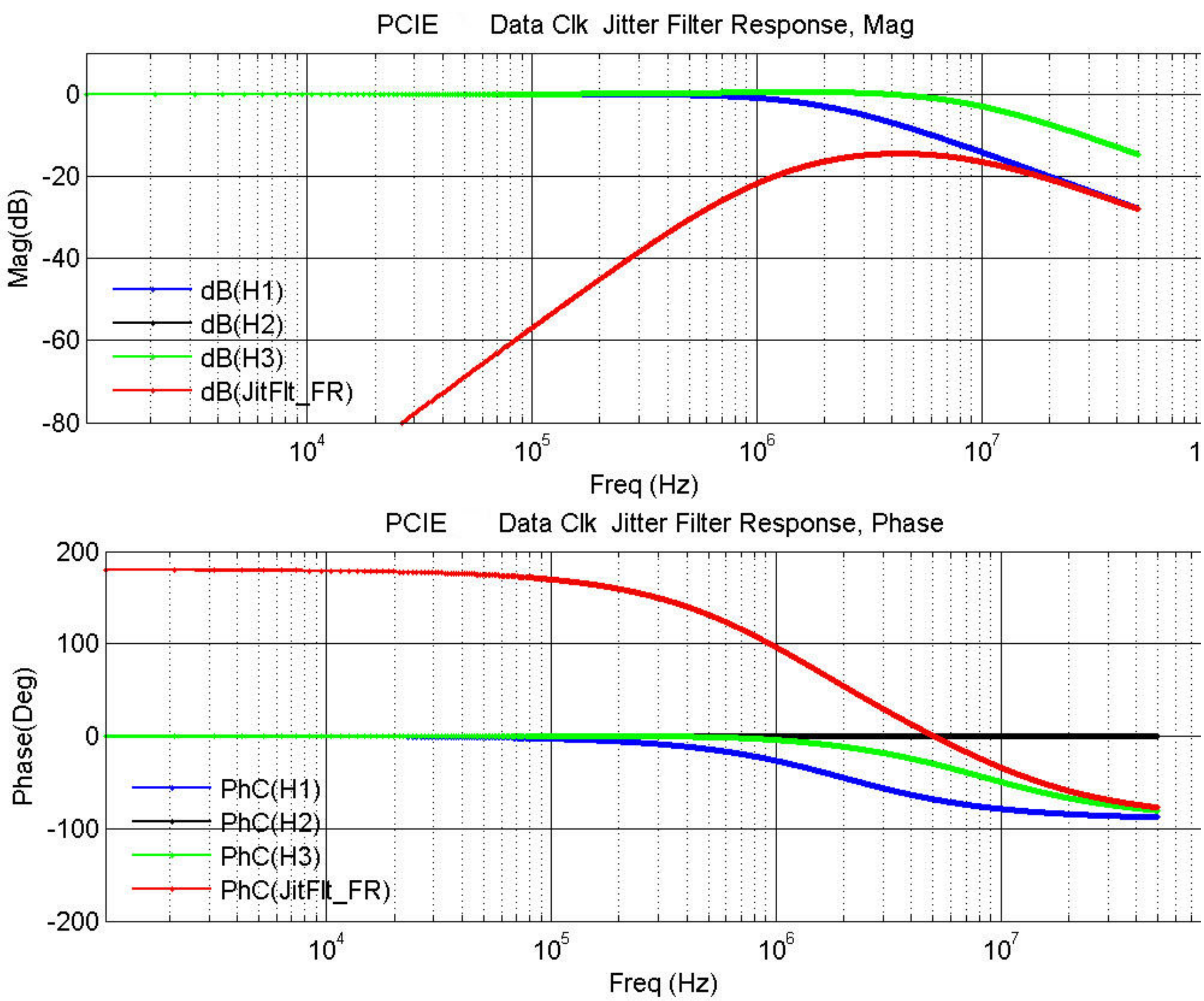


Figure 76 Reference Image for Jitter Filter Response (Data Clock) RMS Jitter Test

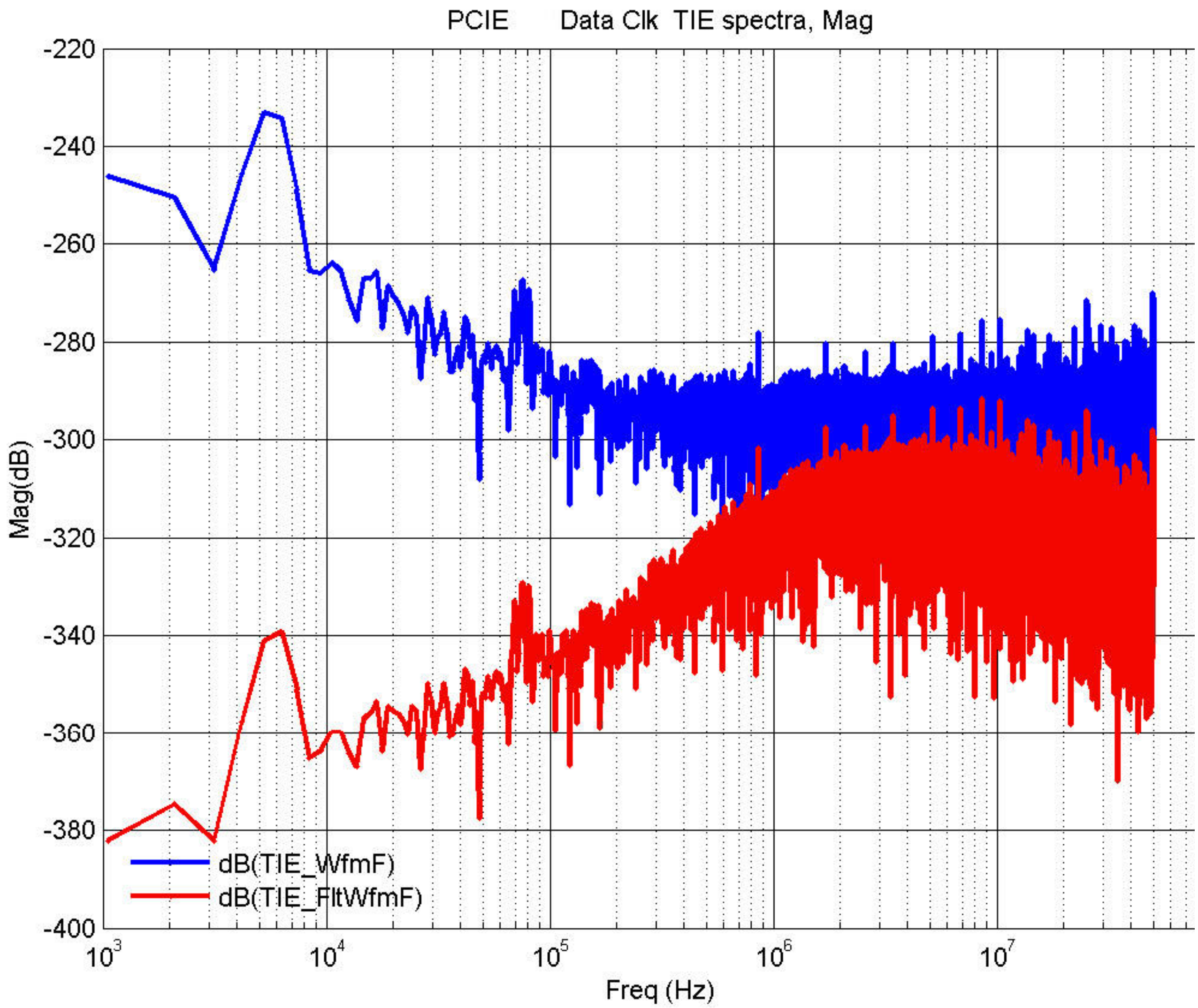


Figure 77 Reference Image for Data Clock TIE Spectra RMS Jitter Test

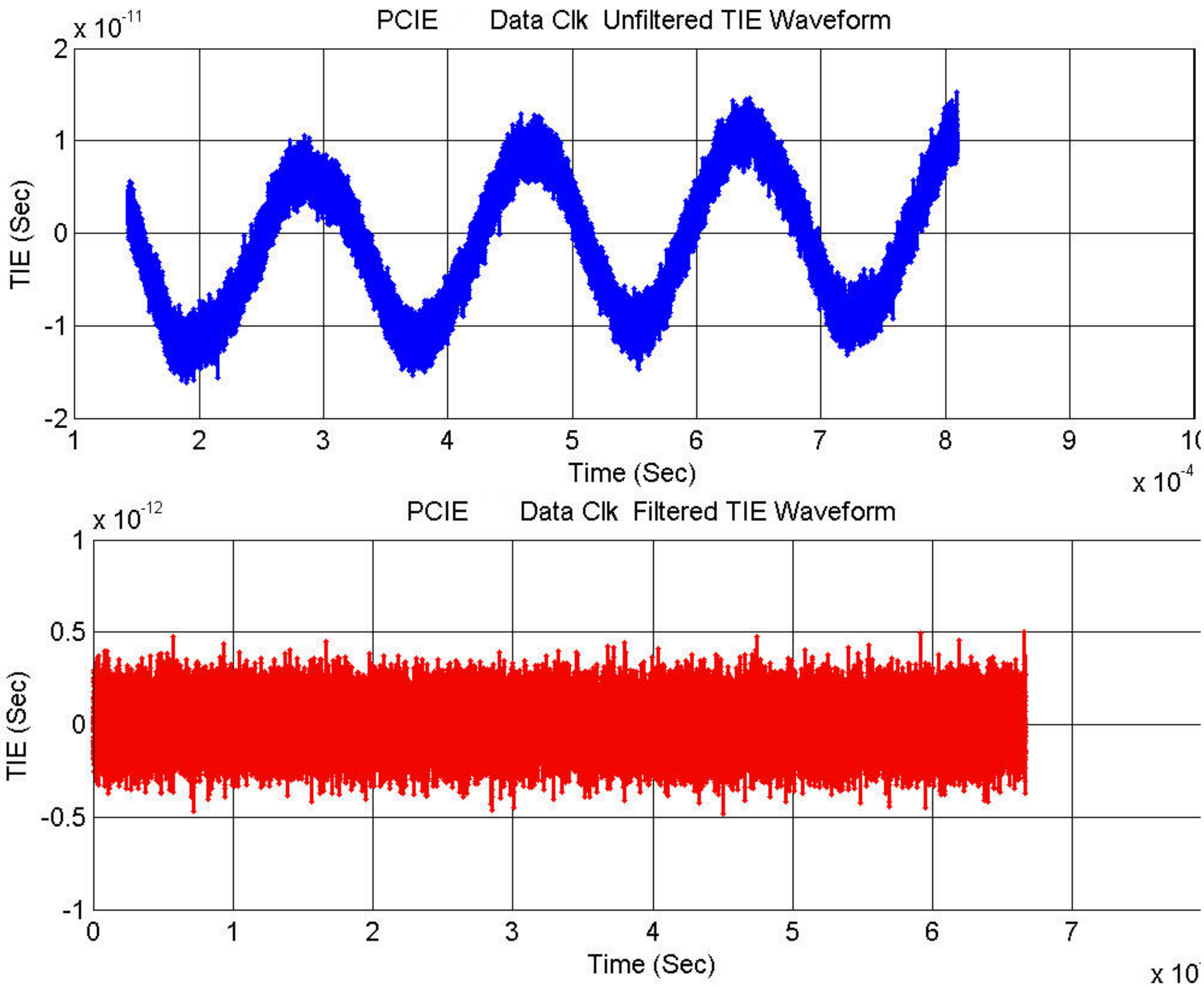


Figure 78 Reference Image for TIE Waveform RMS Jitter Test

Part XII
PCI-Express Gen6 16.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

31 Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 16.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE **It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.**

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

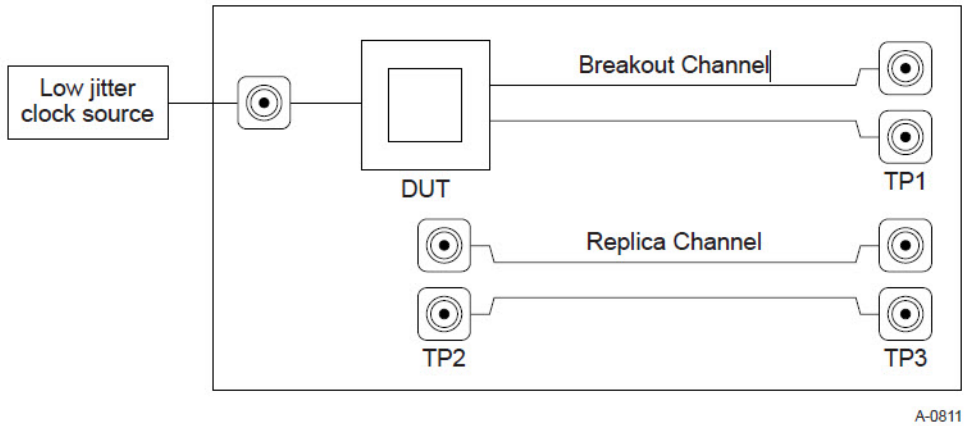


Figure 79 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 16.0 GT/s Tests > Transmitter (Tx) Tests**.

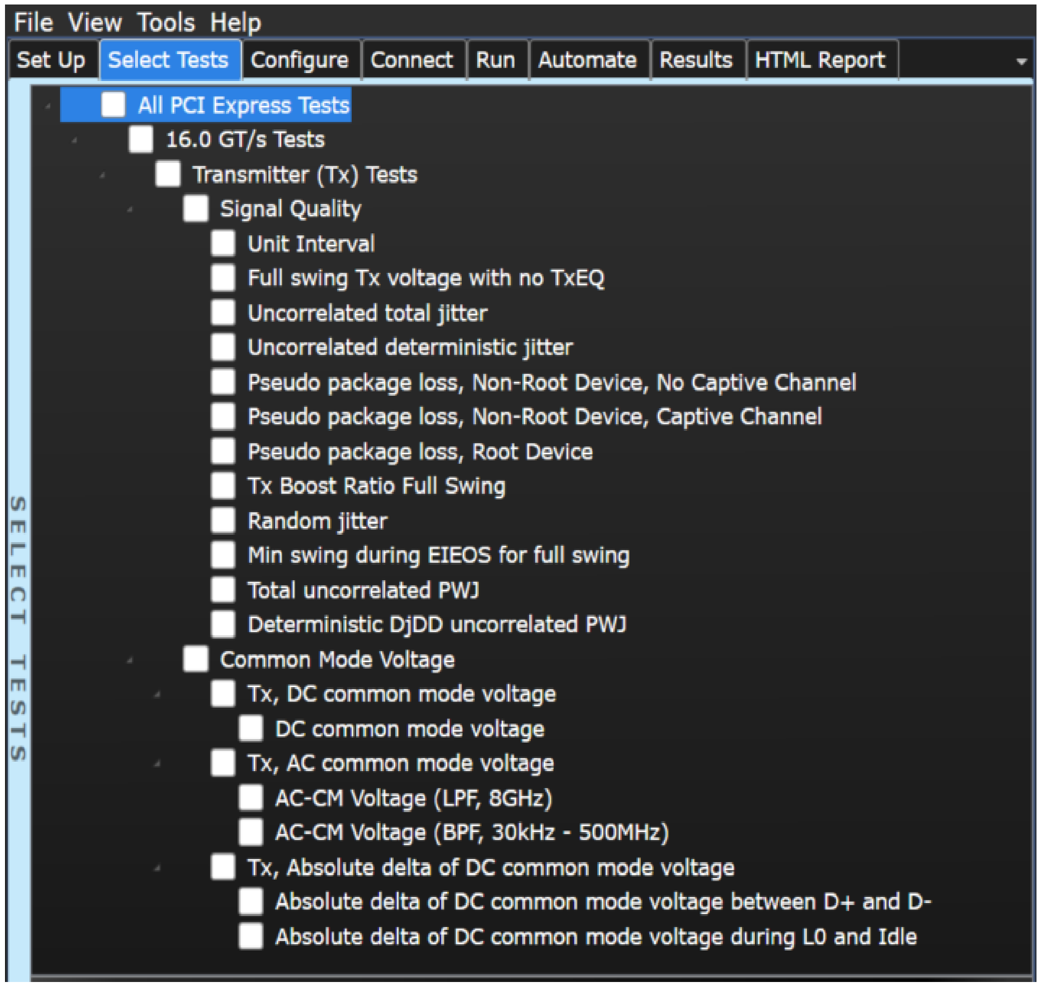


Figure 80 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 94 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	62.48125 ps	62.51875 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
  a Selects **Unit Interval** as data measurement analysis unit.
  b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

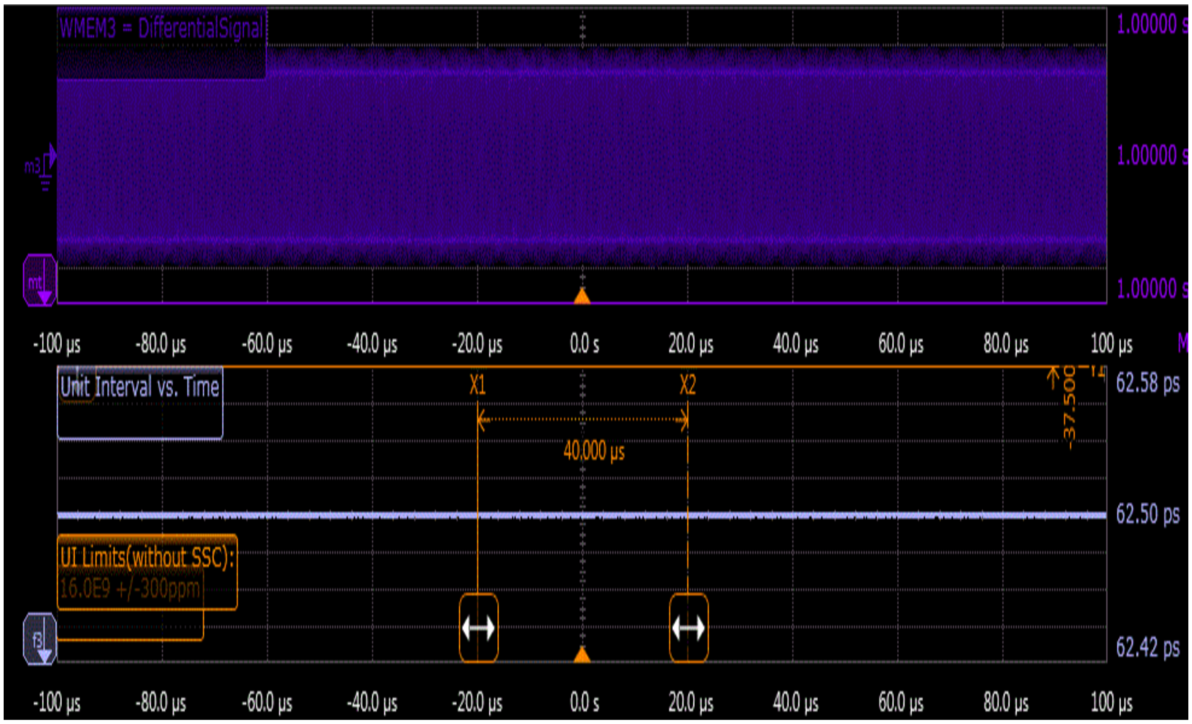


Figure 81 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 82. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP}$ is used as reference to check the compliance of the DUT.

Table 95 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$	Full swing Tx voltage with no TxEQ	800 mV	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as 2 × $|V_{TXD+} - V_{TXD-}|$
- See section 8.3.3.6 and section 8.3.3.7 for measurement details.

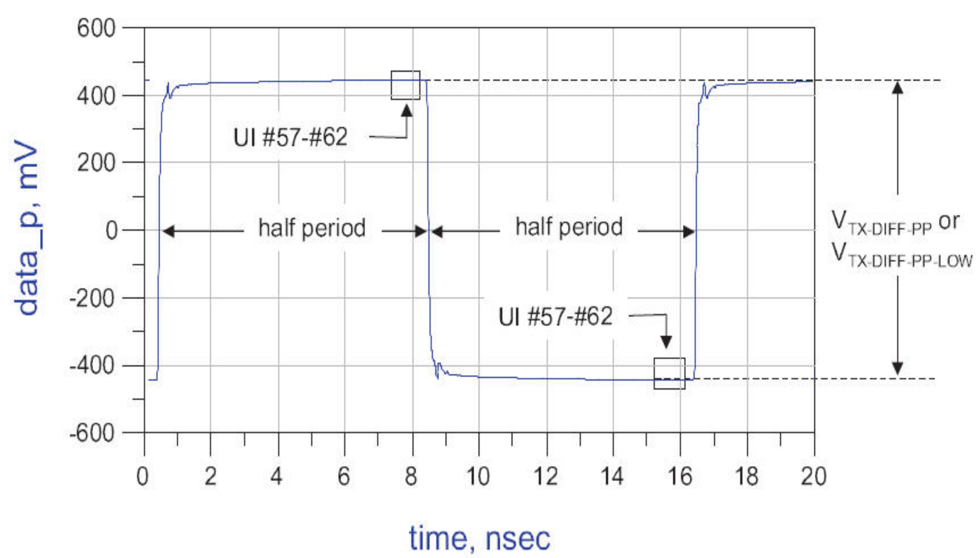


Figure 82 $V_{TX\text{-}DIFF\text{-}PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

> **NOTE** Base - Transmitter Tests:
> MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 83. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 96 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times |V_{TXD+}-V_{TXD-}|$
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

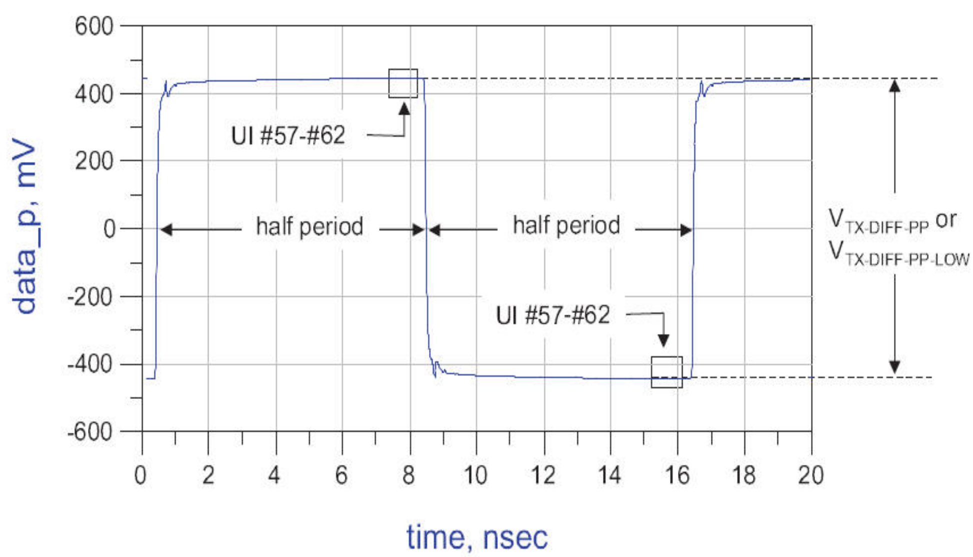


Figure 83 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 97 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	11.8 ps PP at 10^{-12}

Test Definition Notes from the Specification

See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 98 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	6.25 ps PP

Test Definition Notes from the Specification

See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

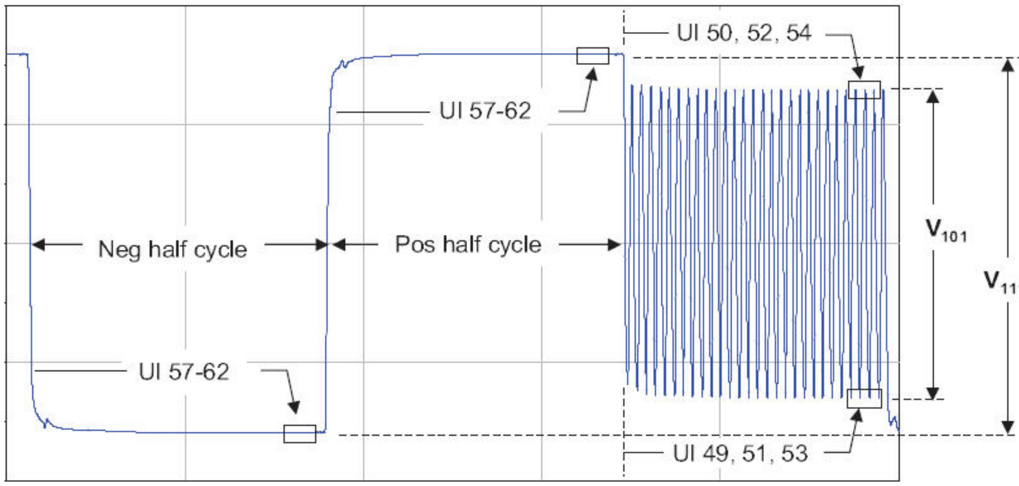
PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 99 Pseudo Package Loss Test Details

Symbol	Parameter	Min
$ps21_{TX-ROOT-DEVICE-CAPTIVE-CHANNEL}$	Pseudo package loss for a device containing root ports	-3.0 dB
$ps21_{TX-ROOT-DEVICE-NO-CAPTIVE-CHANNEL}$	Pseudo package loss for a device containing root ports	Info Only
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss for all devices not containing root ports	Info Only

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 84 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX\text{-}BOOST\text{-}FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 100 Tx Boost Ratio Full Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}BOOST\text{-}FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate at preset value #P4.
3. Configures optimum values for Scale and Offset using Channel Setup.
4. Configures memory depth and sampling rate as per the data rate.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate at preset value #P10.
8. Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9. Configures optimum values for Scale and Offset using Channel Setup.
10. Configures memory depth and sampling rate as per the data rate.
11. Fits and displays all sample data on screen.
12. Saves the P10 signal in *.bin format.
13. Inputs the P10 and P4 saved waveform into SigTest tool.
14. Computes the de-emphasis at preset value P10.
15. Reports the measurement of Vb during preset values P10 and P4.
16. Computes the Vtx boost from the Vb and de-emphasis values.
17. Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 101 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 6.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 102 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	Info Only

Test Definition Notes from the Specification

- Informative parameter only. Range of Rj possible with zero to maximum allowed TTX-UDJDD.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14 at 16.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 103 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0. 32.0, and 64.0 GT/s that ensures that these parameters are met.

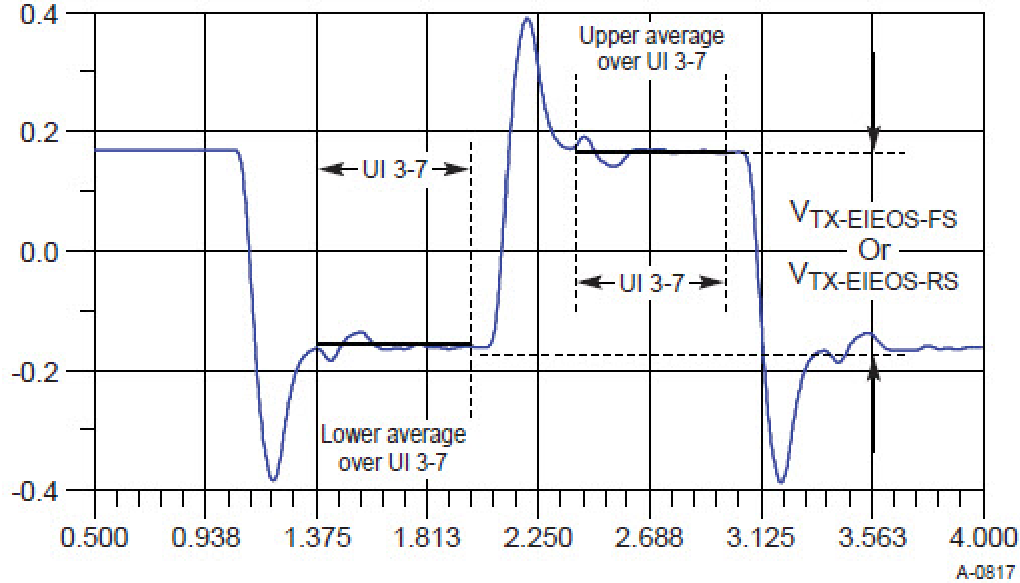


Figure 85 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX\text{-}EIEOS\text{-}RS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 104 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

$V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0. 32.0, and 64.0 GT/s that ensures that these parameters are met.

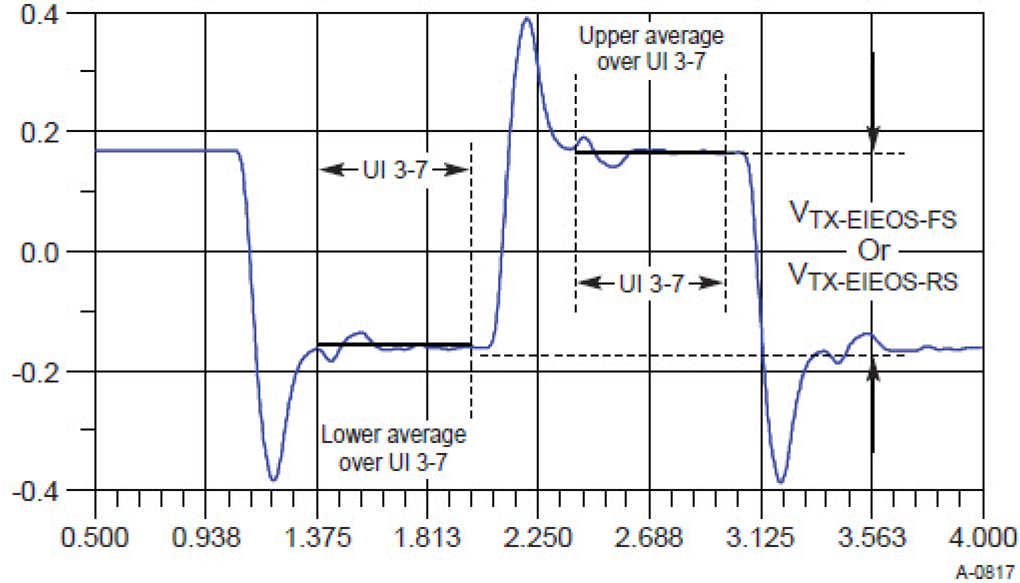


Figure 86 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 105 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	12.5 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See and § Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).b
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 106 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	5 ps PP

Test Definition Notes from the Specification

- See and section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 107 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 16.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Sets the scale and offset of the input channels to their optimum values.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures the frequency of the jitter TREND on WMEM1.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 108 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.03%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 16.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 109 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.53%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 16.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC df/dt (Max) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 110 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate.
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   - *a* Generates a differential plot (x_n - x_{n-1}).
   - *b* The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE
Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

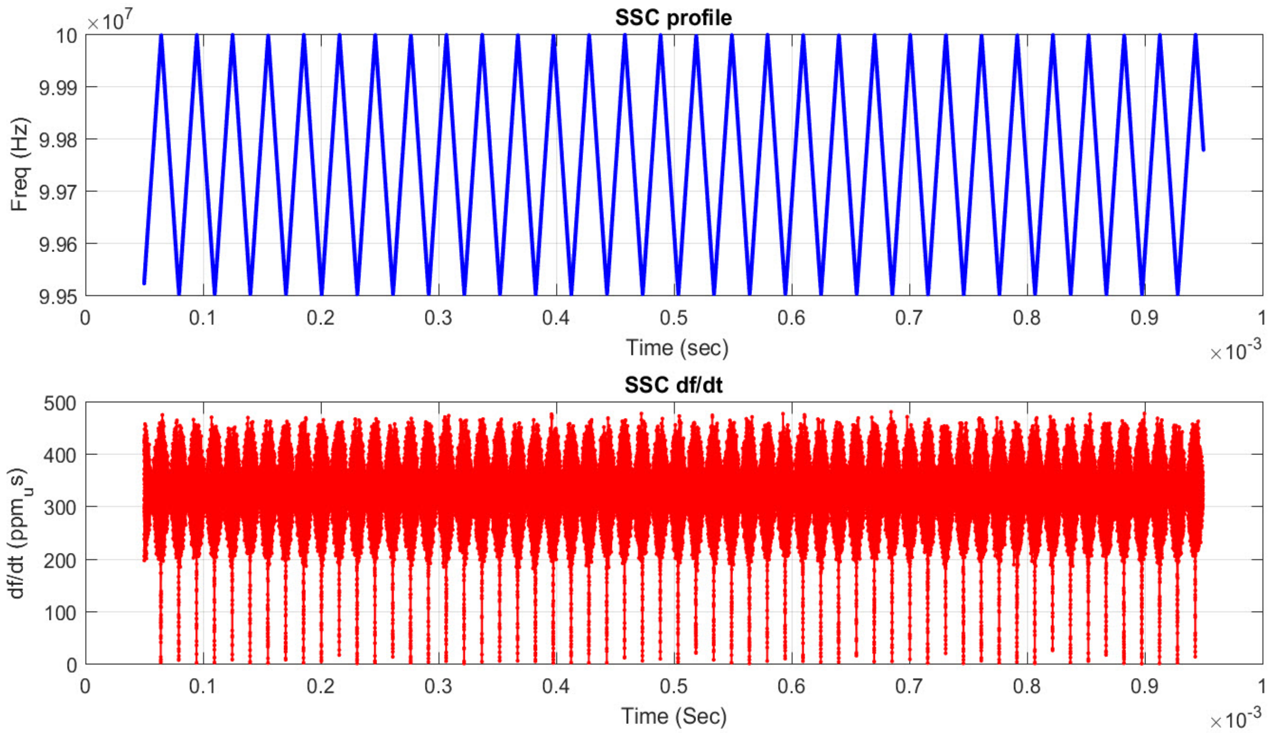


Figure 87 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 111 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

   a Enables and displays common mode measurements.

   b Loads common mode signal to waveform memory.

   c Loads and enhance dynamic range D+ signal and D- signal.

   d Enables the average common mode measurement.

   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, as $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 8 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 112 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4. Measures the VPP of the filtered signal.
5. Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 113 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	50 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 8 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25$ mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 114 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Test Definition Notes from the Specification

$| V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}\ [during\ L0]} | \leq 25$mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $| V_{TX\text{-}D+\ [during\ L0]} |$

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $| V_{TX\text{-}D\text{-}\ [during\ L0]} |$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

> **NOTE** This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT..

Table 115 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Test Definition Notes from the Specification

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

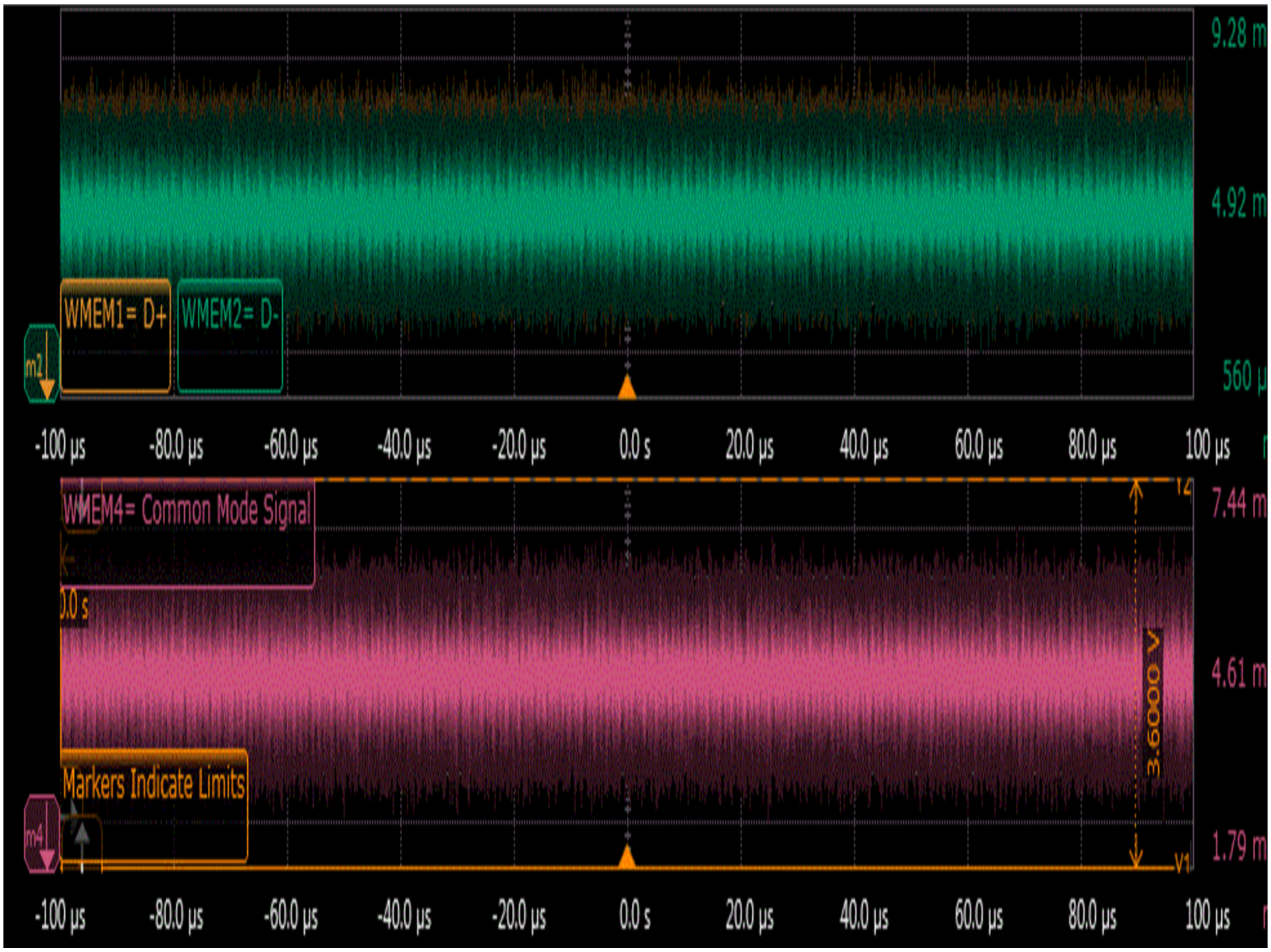


Figure 88 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Running Equalization Presets Tests

Please refer to section: "Running Equalization Presets Tests" on page 829 in Chapter 29, "Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 6.0".

32 Reference Clock Tests, 16.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 16.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

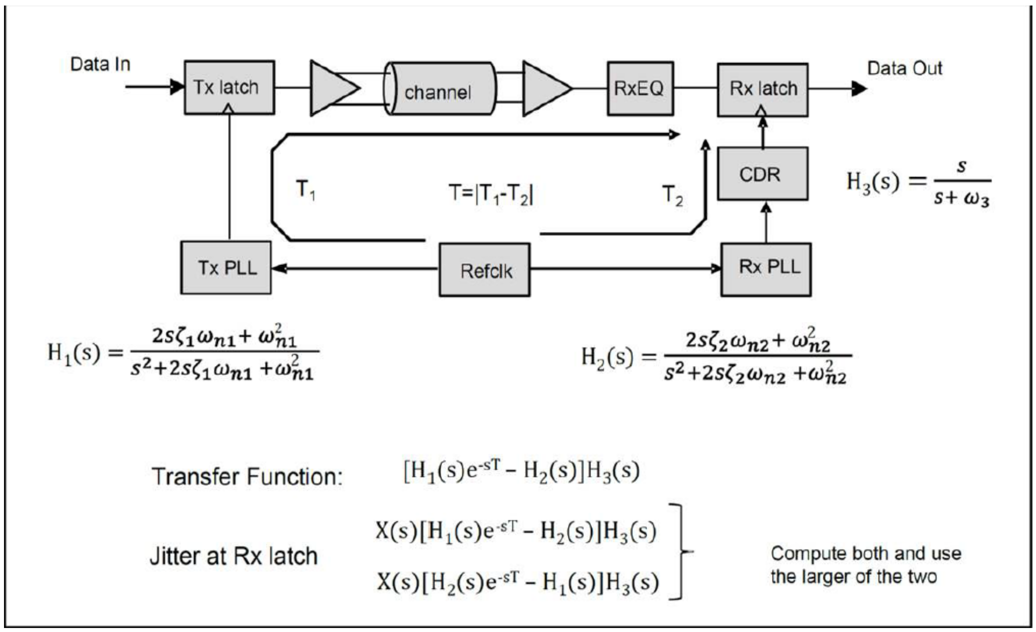
NOTE It is recommended to use normal or non real edge channels on the scope for data rates up to 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 16.0 GT/s, PCI-E 6.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations				8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

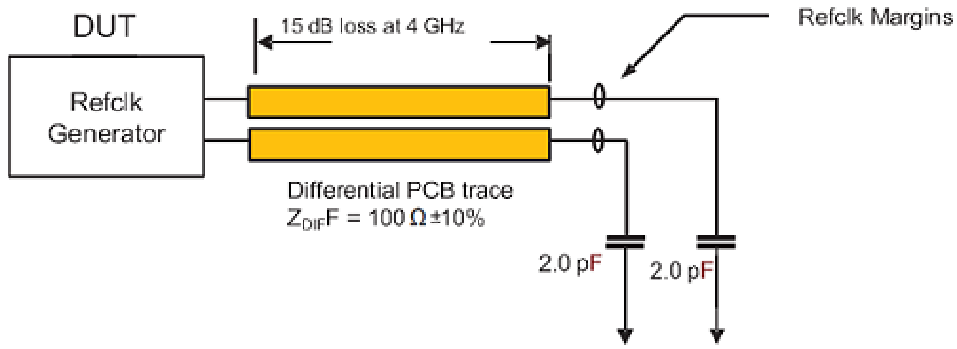


Figure 89 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 16.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

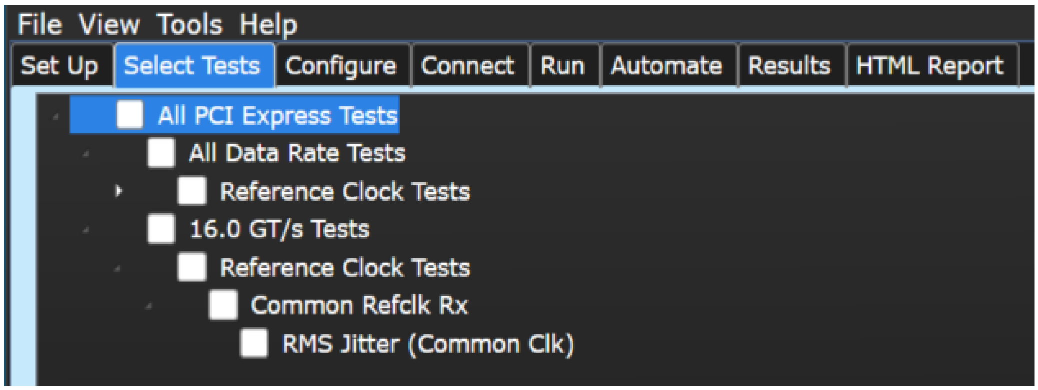


Figure 90 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 116 RMS Jitter Test Details

Symbol	Description	Value
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.5 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.
- For the 16.0, 32.0, and 64.0 GT/s CC measurements SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
- Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

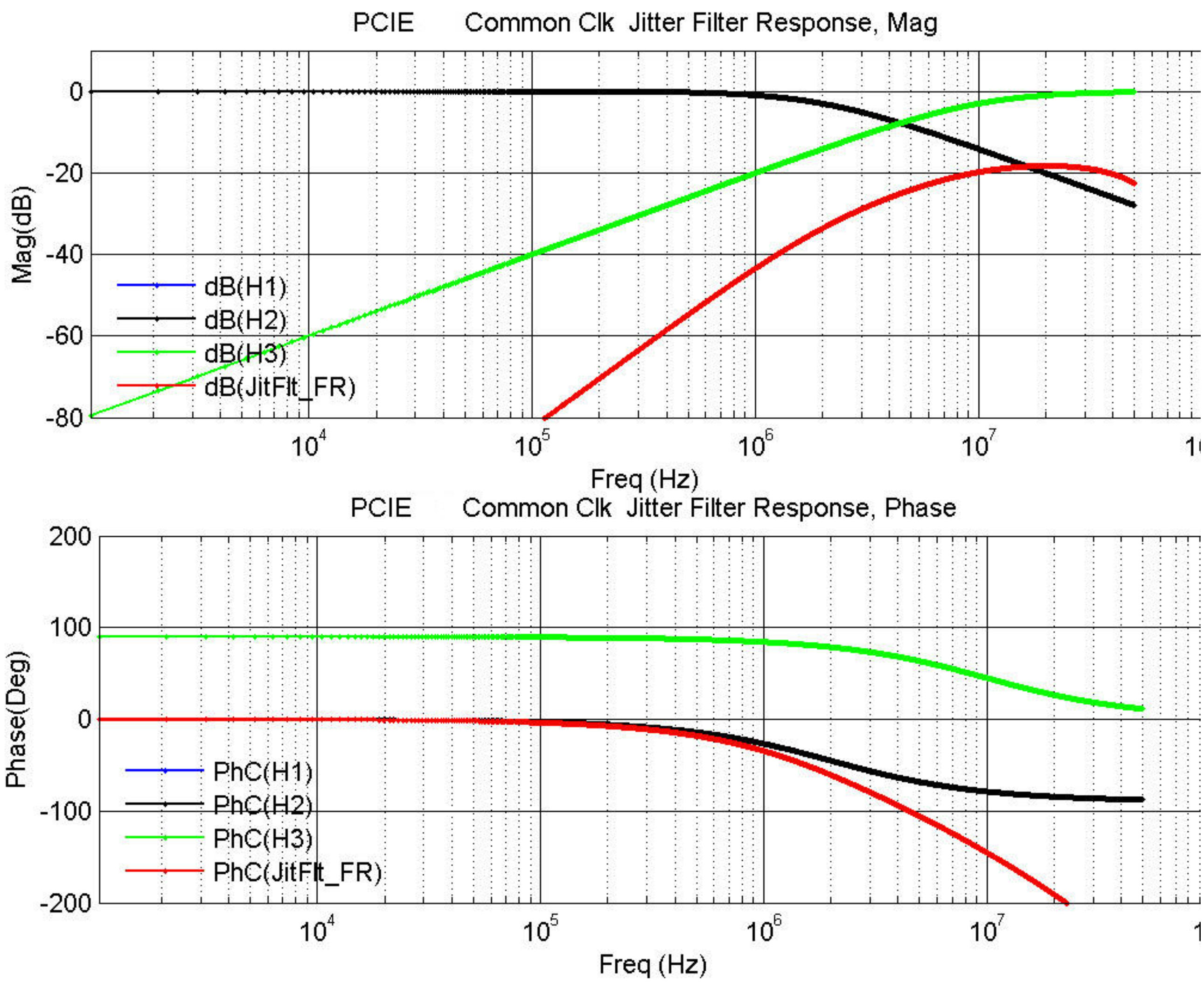


Figure 91 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

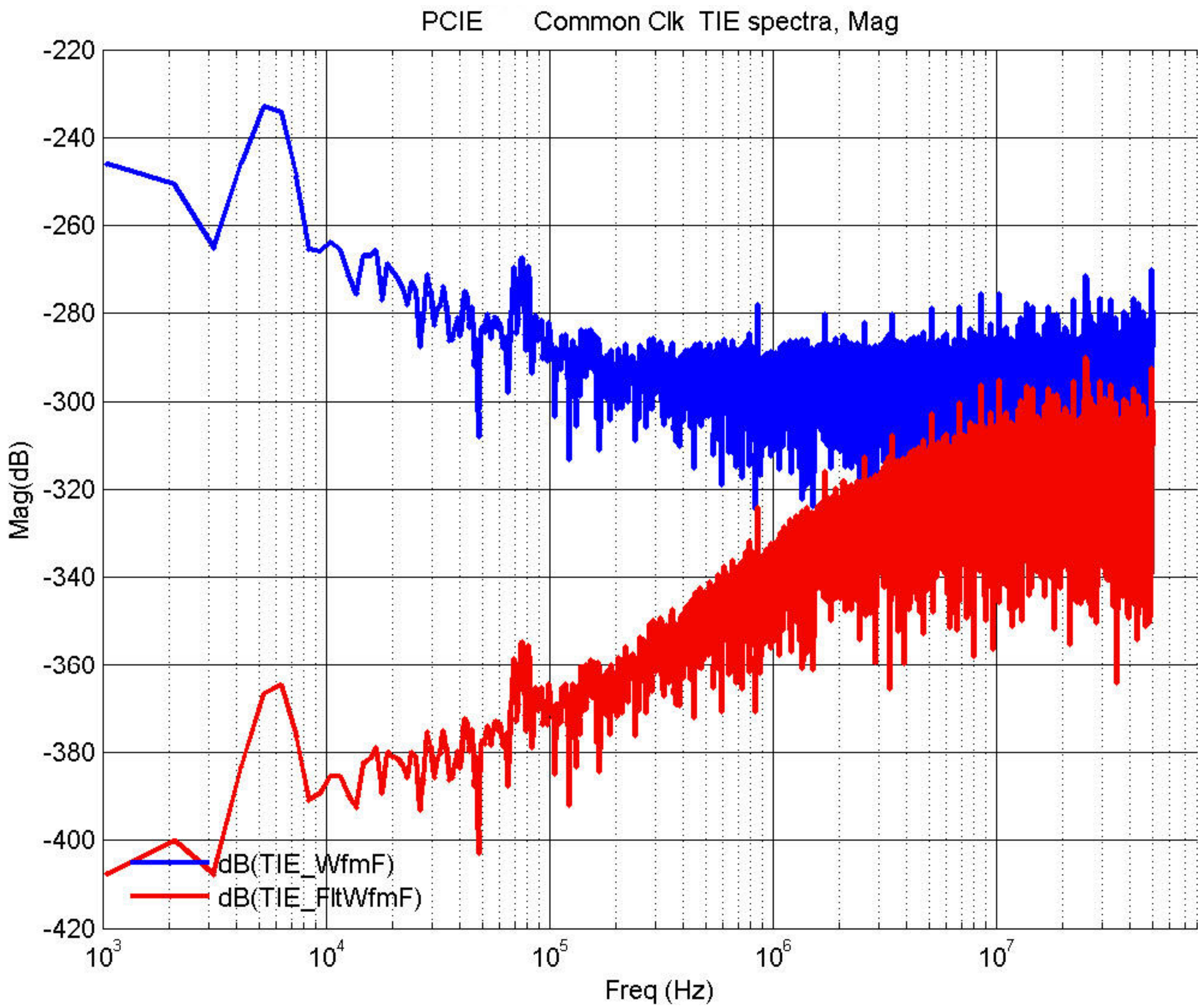


Figure 92 Reference Image for Common Clock TIE Spectra RMS Jitter Test

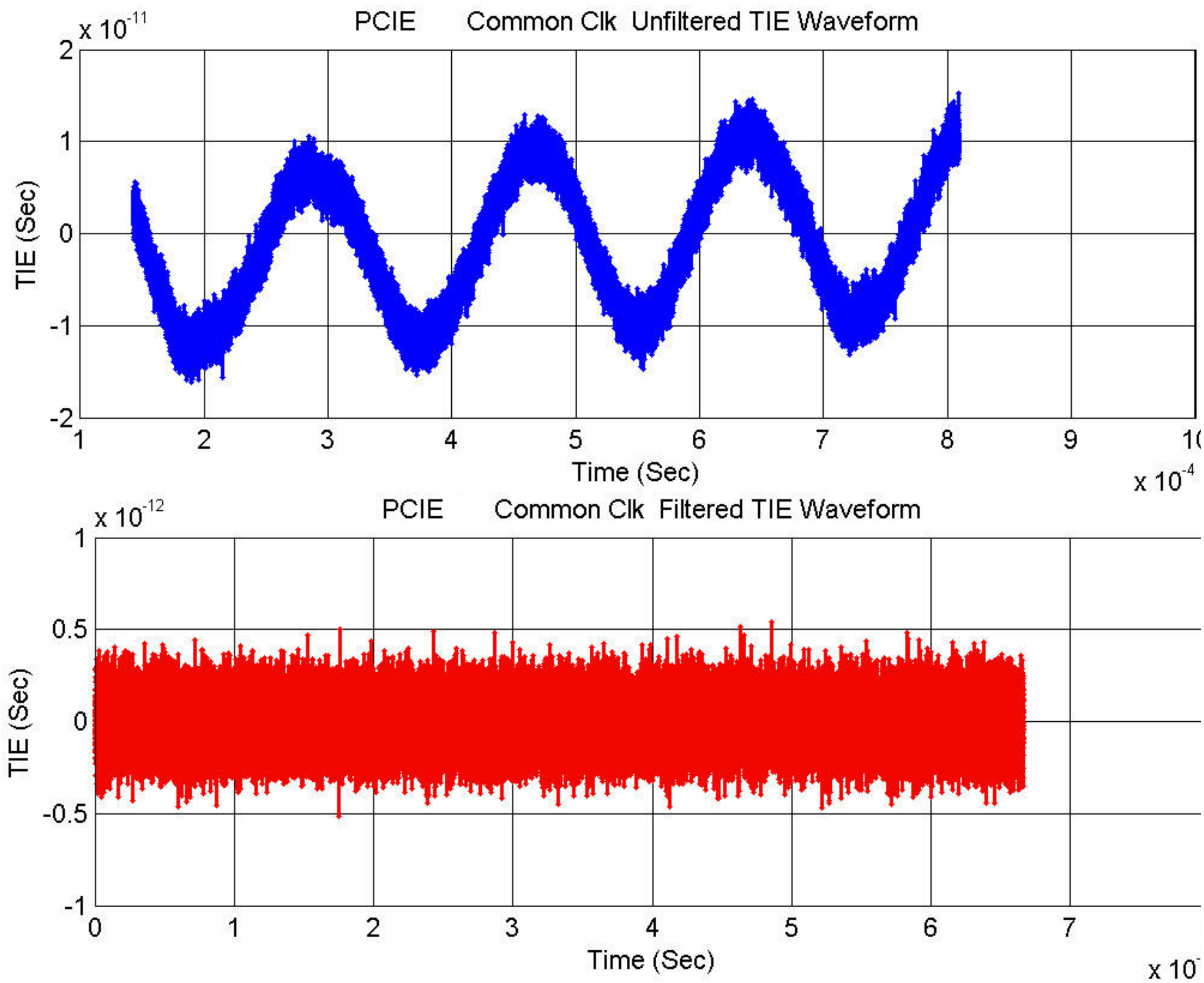


Figure 93 Reference Image for TIE Waveform RMS Jitter Test

Part XIII
PCI Express Gen6 32.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

33 Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 32.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

NOTE **In case of Z-series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 6.0 compliance testing.**

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

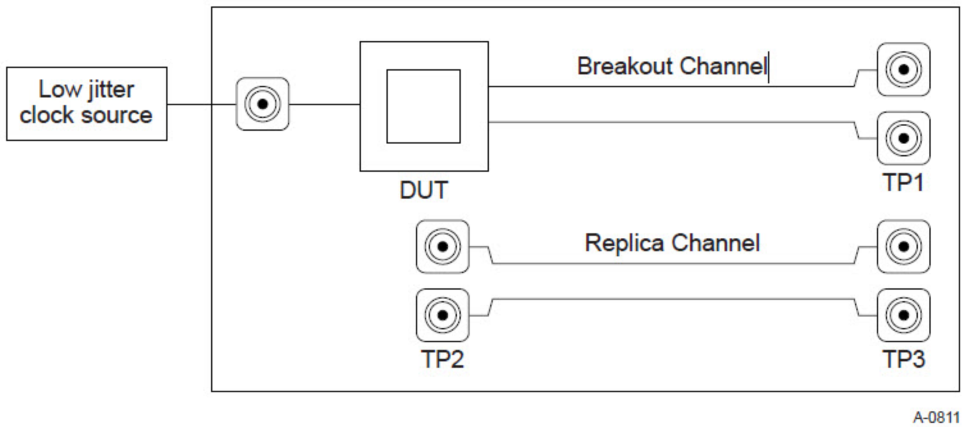


Figure 94 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 32.0 GT/s Tests > Transmitter (Tx) Tests**.

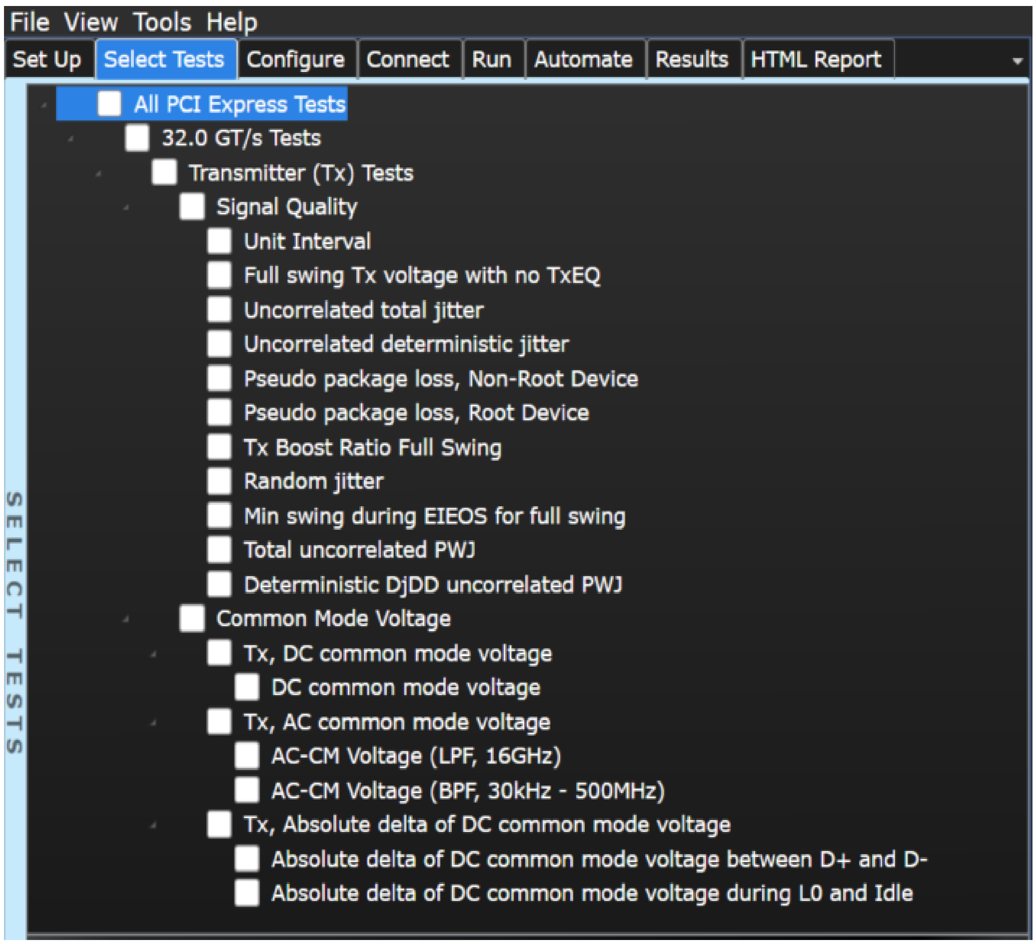


Figure 95 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 117 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.246875 ps	31.253125 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

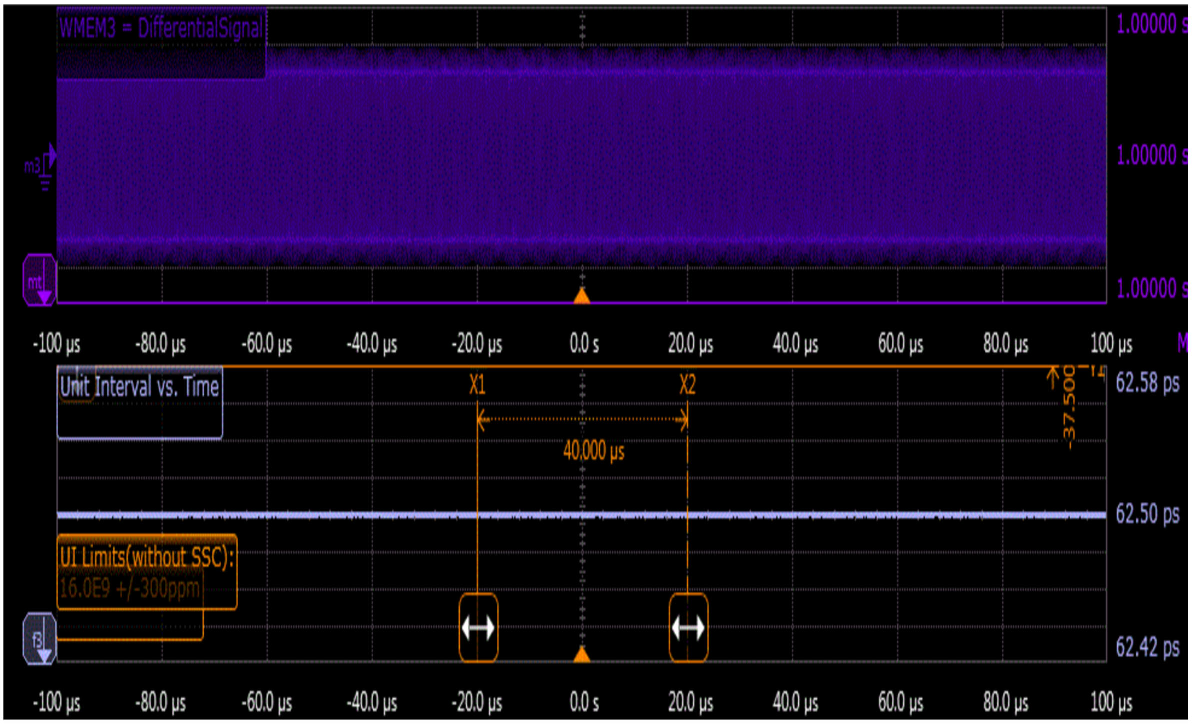


Figure 96 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 97. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP}$ is used as reference to check the compliance of the DUT.

Table 118 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DIFF\text{-}PP}$	Full swing Tx voltage with no TxEQ	800 mV	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times |V_{TXD+} - V_{TXD-}|$
- See section 8.3.3.6 and section 8.3.3.7 for measurement details.

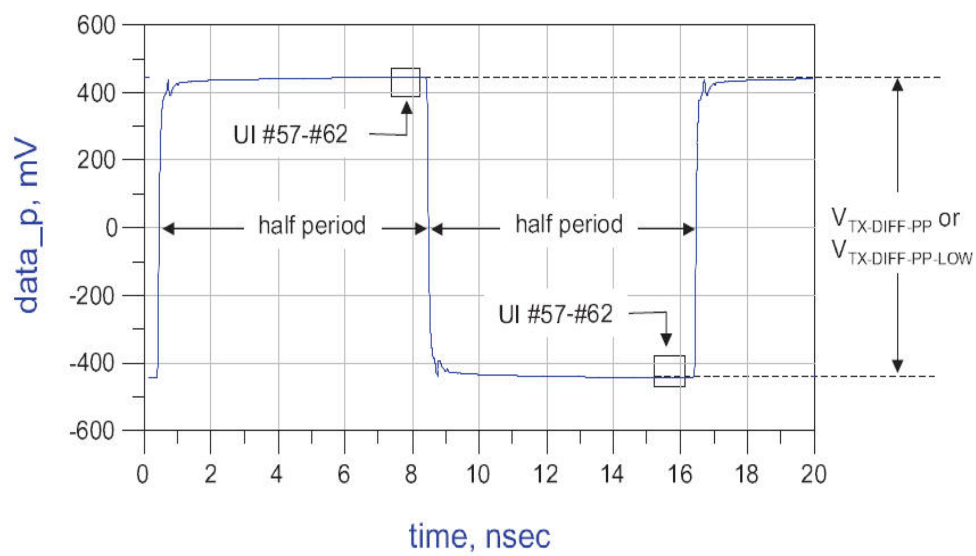


Figure 97 $V_{TX\text{-}DIFF\text{-}PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 98. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 119 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP-LOW}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times | V_{TXD+}-V_{TXD-}|$
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

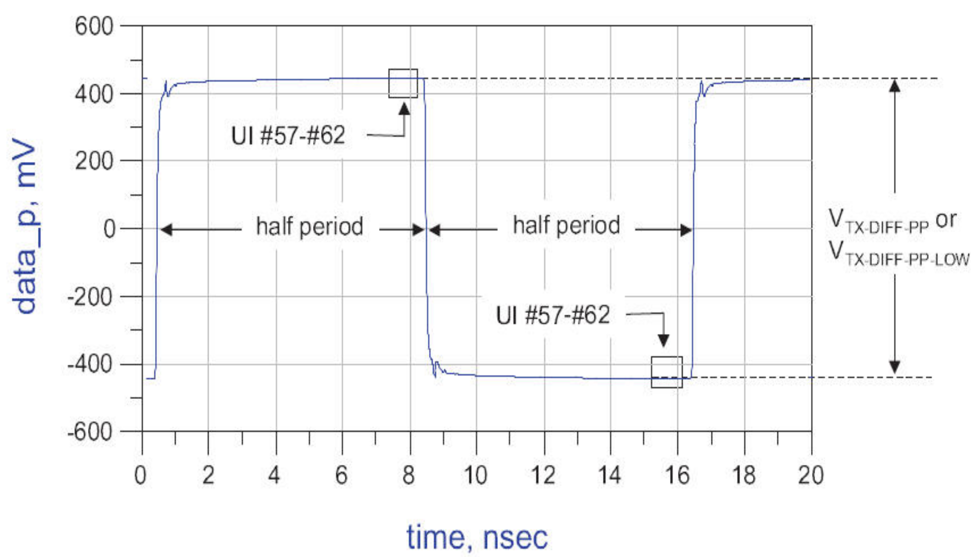


Figure 98 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #P4.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0µs.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Inputs the P4 saved waveform into SigTest tool.
8. Computes the measurement of Vb at preset value P4.
9. Reports the measurement of Vb during preset values P4.
10. Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI; at 32.0 GT/s the pattern is repeated for two consecutive blocks. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28 at 32.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages.
UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 120 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

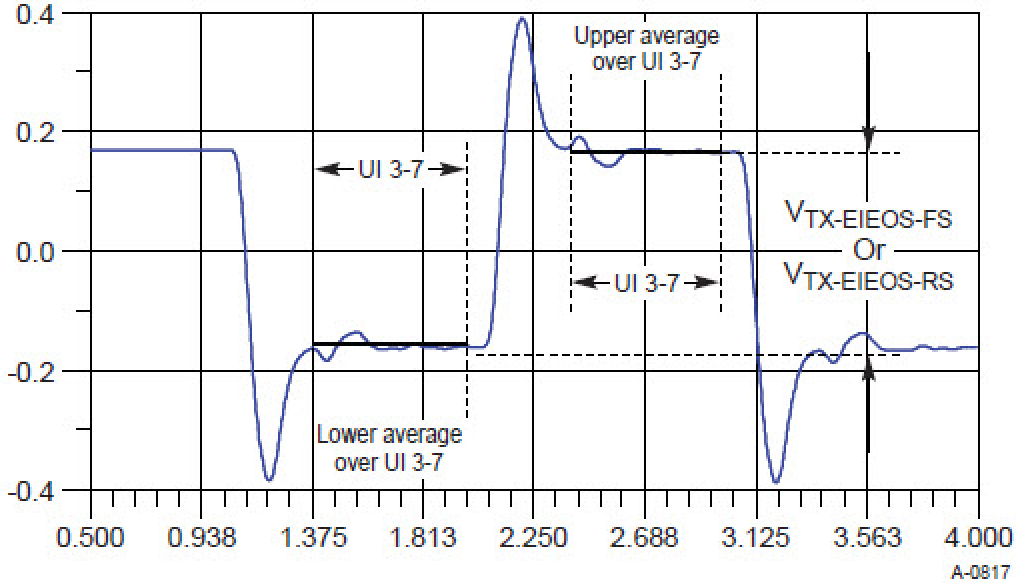


Figure 99 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX\text{-}EIEOS\text{-}RS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX\text{-}EIEOS\text{-}FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 121 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

$V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

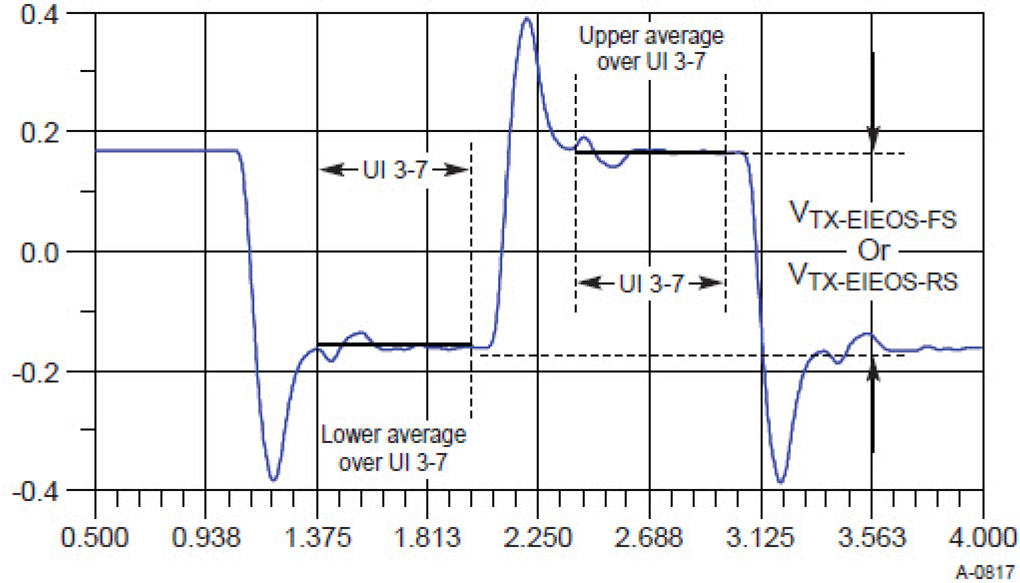


Figure 100 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 122 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 123 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	3.125 ps PP

Test Definition Notes from the Specification

See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX\text{-}UPW\text{-}TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 124 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UPW\text{-}TJ}$	Total uncorrelated PWJ	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 125 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	2.5 ps PP

Test Definition Notes from the Specification

- See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

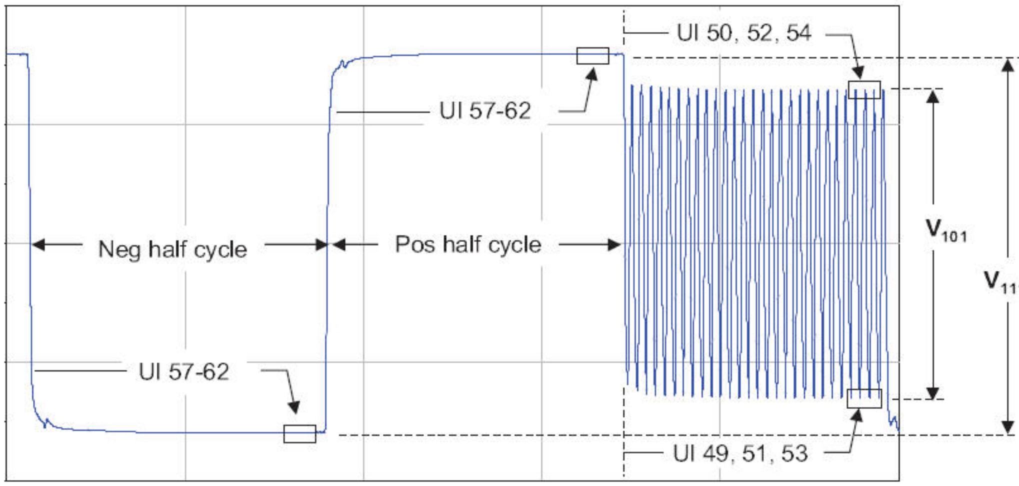
PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 126 Pseudo Package Loss Test Details

Symbol	Parameter	Min
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	-8.5 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	-3.7 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 101 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX-BOOST-FS}$ is within the allowed range. This test required Preset 04 and Preset 10.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 127 Tx Boost Ratio Full Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate at preset value #P4.
3. Configures optimum values for Scale and Offset using Channel Setup.
4. Configures memory depth and sampling rate as per the data rate.
5. Fits and displays all sample data on screen.
6. Saves the P4 signal into *.bin format.
7. Configures the DUT to operate at preset value #P10.
8. Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9. Configures optimum values for Scale and Offset using Channel Setup.
10. Configures memory depth and sampling rate as per the data rate.
11. Fits and displays all sample data on screen.
12. Saves the P10 signal in *.bin format.
13. Inputs the P10 and P4 saved waveform into SigTest tool.
14. Computes the de-emphasis at preset value P10.
15. Reports the measurement of Vb during preset values P10 and P4.
16. Computes the Vtx boost from the Vb and de-emphasis values.
17. Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset 04 and Preset 01.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 128 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 6.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #P4.
3 Configures optimum values for Scale and Offset using Channel Setup.
4 Configures memory depth and sampling rate as per the data rate.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate at preset value #P1.
8 Configures the value of the test parameters as the values configured for the Number of UI and Sample Rate configuration parameters using Automated Test Engine.
9 Configures optimum values for Scale and Offset using Channel Setup.
10 Configures memory depth and sampling rate as per the data rate.
11 Fits and displays all sample data on screen.
12 Saves the P1 signal in *.bin format.
13 Inputs the P1 and P4 saved waveform into SigTest tool.
14 Computes the de-emphasis at preset value P1.
15 Reports the measurement of Vb during preset values P1 and P4.
16 Computes the Vtx boost from the Vb and de-emphasis values.
17 Compares the Vtx boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter (Information Only)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 129 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	Info Only

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJDD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 130 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage as follows:
   - *a* Enables and displays common mode measurements.
   - *b* Loads common mode signal to waveform memory.
   - *c* Loads and enhance dynamic range D+ signal and D- signal.
   - *d* Enables the average common mode measurement.
   - *e* Uses markers to indicate compliance test limit boundaries (0 V to 3.6 V).
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100 mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 16 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 131 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 132 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	50 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 16 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during L0]} - V_{TX-CM-DC-D-[during L0]}| \leq 25$ mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 133 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Test Definition Notes from the Specification

$| V_{TX-CM-DC-D+ [during L0]} - V_{TX-CM-DC-D- [during L0]} | \leq 25$mV

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $| V_{TX-D+ [during L0]} |$

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $| V_{TX-D- [during L0]} |$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 134 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Test Definition Notes from the Specification

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D-}|/2$ [electrical idle]

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

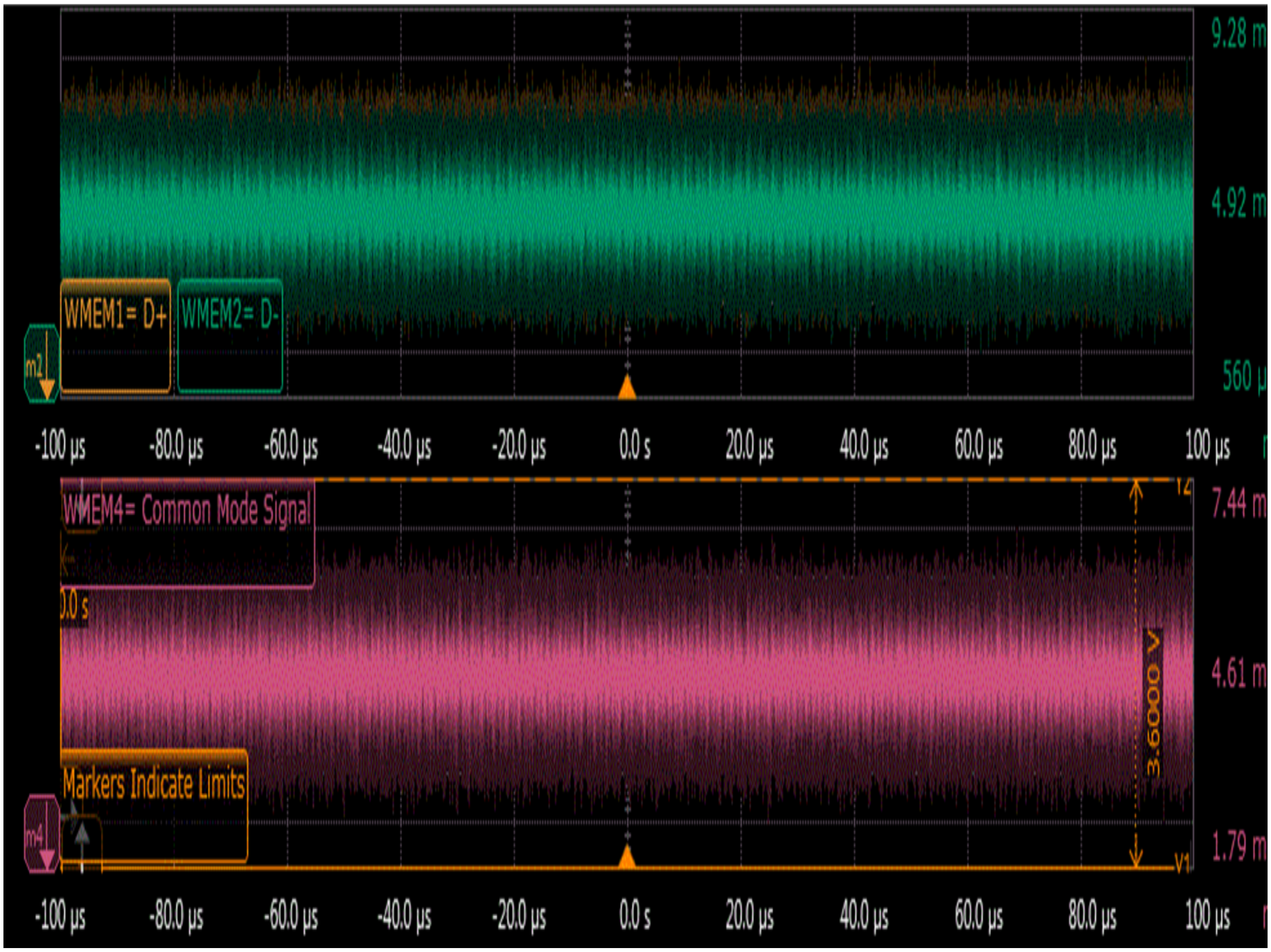


Figure 102 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 135 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 32.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 136 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	0.01%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 32.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-1 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 137 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC-FREQ-DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.31%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the data signal.
2. Verifies that the data rate is 32.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 138 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate..
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   a. Generates a differential plot (x_n - x_{n-1}).
   b. The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

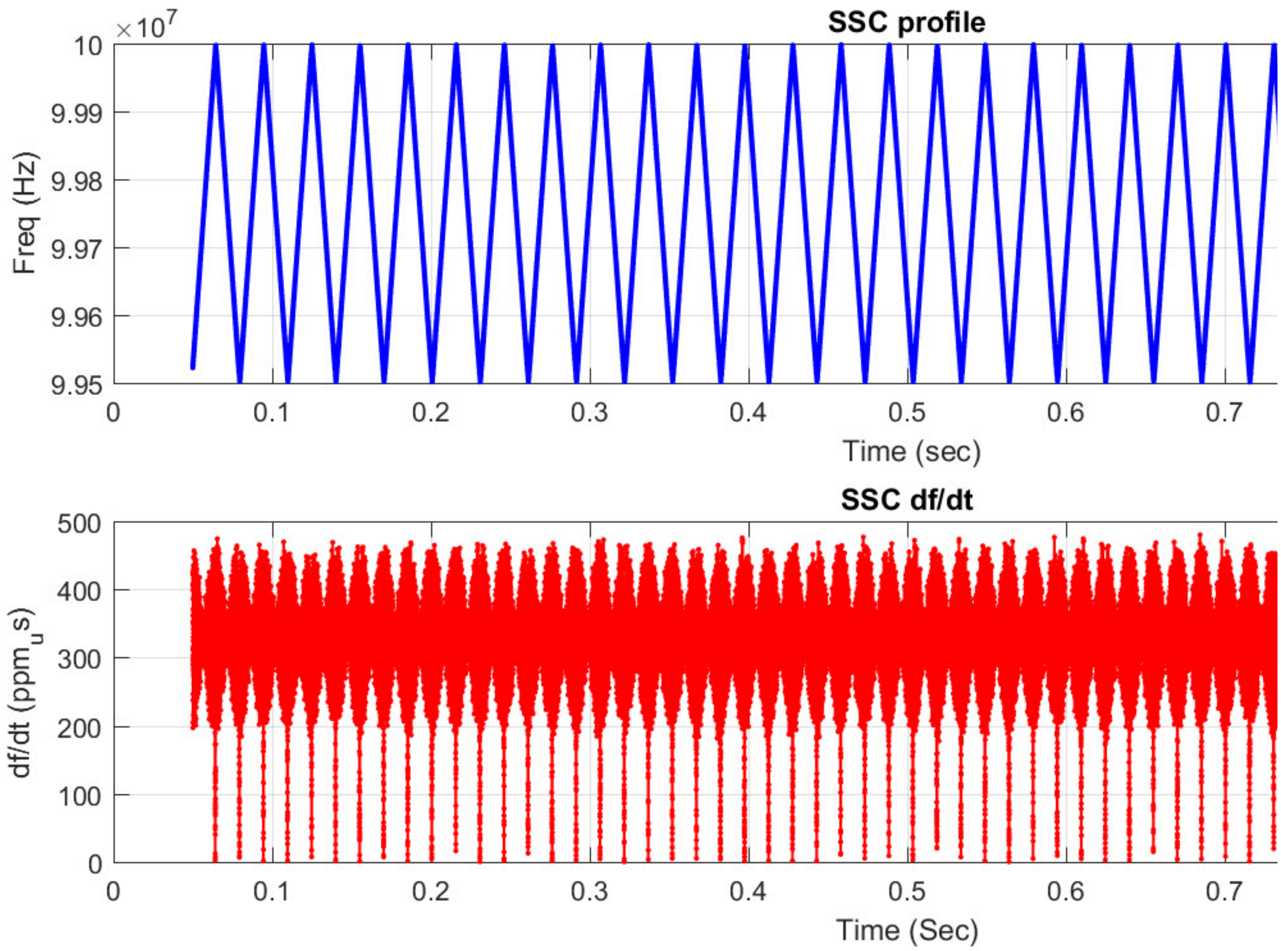


Figure 103 Maximum SSC Slew Rate

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to "Equalization Presets Tests".

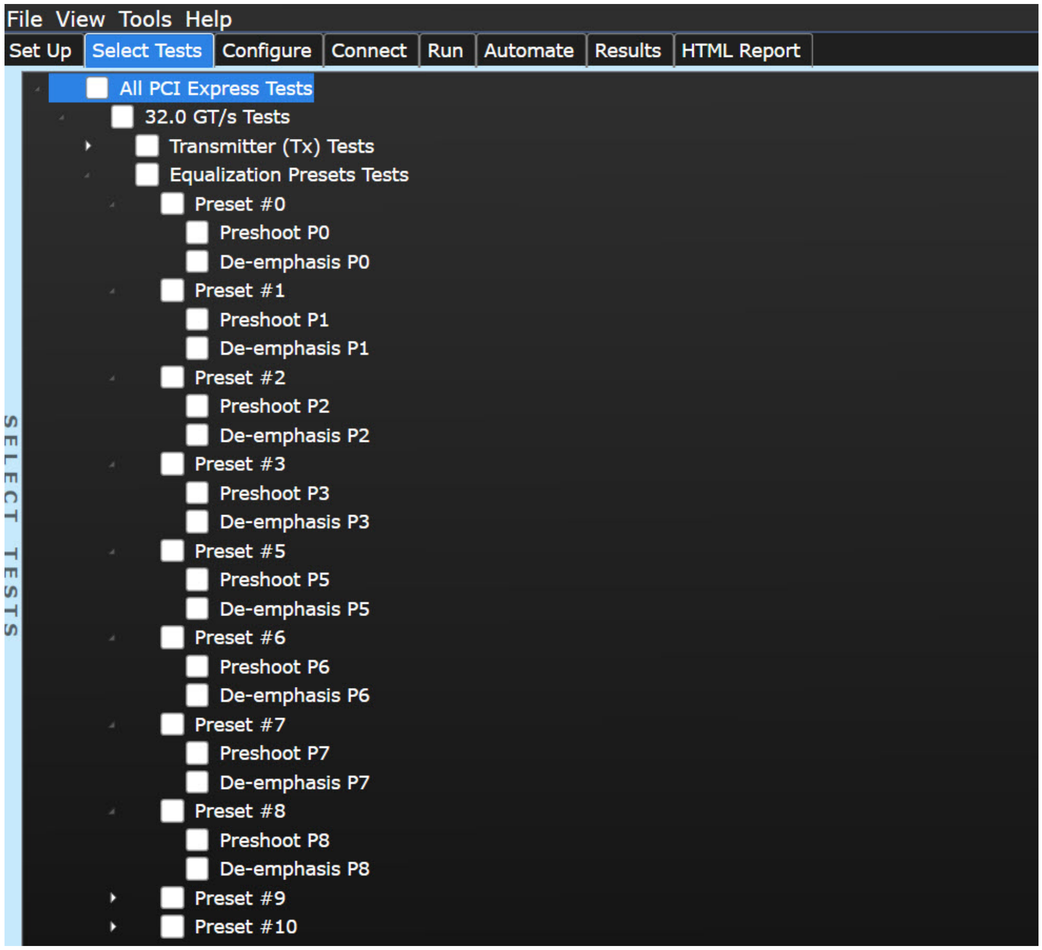


Figure 104 Selecting Equalization Presets Tests

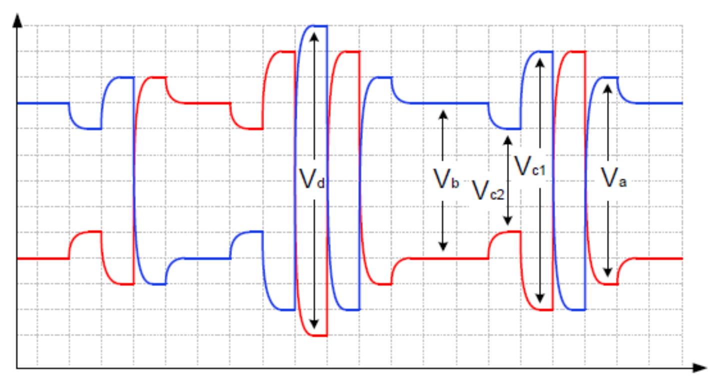
Preset #0 Measurement (P0), Preshoot Test

This test verifies that the preshoot of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 139 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A



De-emphasis $= 20\log_{10}(V_b/V_a)$ $\quad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $\quad c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $\quad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $\quad c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $\quad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $\quad c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $\quad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $\quad c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $\quad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 105 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 140 Preset P0 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P0	0.0	0.0 ±1 dB	–6.0 ± 1.5 dB	0.000	0.000	–0.250	1.000	0.500	0.500	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P0.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P0 signal in *.bin format.

12 Inputs the P4 and P0 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P0.

14 Reports the measurement of Vb during preset values P0 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #0 Measurement (P0), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 141 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

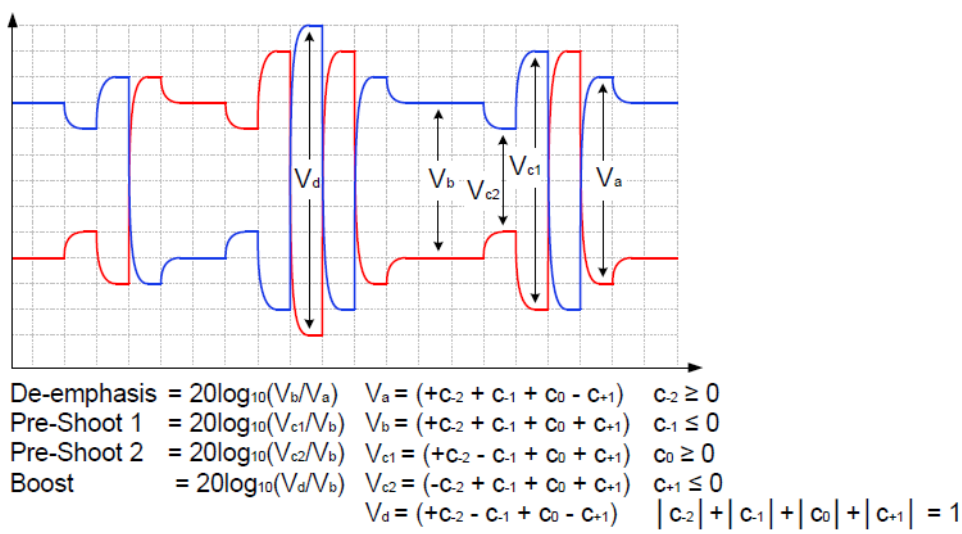


Figure 106 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 142 Preset P0 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P0	0.0	0.0 ±1 dB	−6.0 ± 1.5 dB	0.000	0.000	−0.250	1.000	0.500	0.500	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P0.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P0 signal in *.bin format.

12 Inputs the P4 and P0 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P0.

14 Reports the measurement of Vb during preset values P0 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

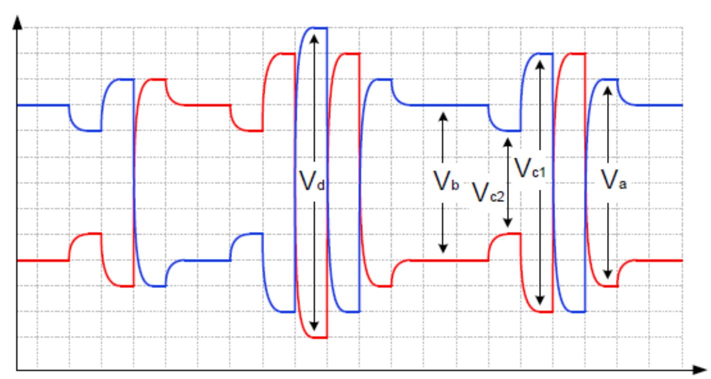
Preset #1 Measurement (P1), Preshoot Test

This test verifies that the preshoot of the preset number P1 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 143 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \quad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \quad c_{-2} \geq 0$$
$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \quad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \quad c_{-1} \leq 0$$
$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \quad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \quad c_0 \geq 0$$
$$\text{Boost} = 20\log_{10}(V_d/V_b) \quad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \quad c_{+1} \leq 0$$
$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \quad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 107 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 144 Preset P1 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P1	0.0	0.0 ±1 dB	–3.5 ± 1 dB	0.000	0.000	–0.167	1.000	0.666	0.666	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P1.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P1 signal in *.bin format.

12 Inputs the P4 and P1 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P1.

14 Reports the measurement of Vb during preset values P1 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (P1), De-emphasis Test

This test verifies that the de-emphasis of the preset number P1 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 145 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

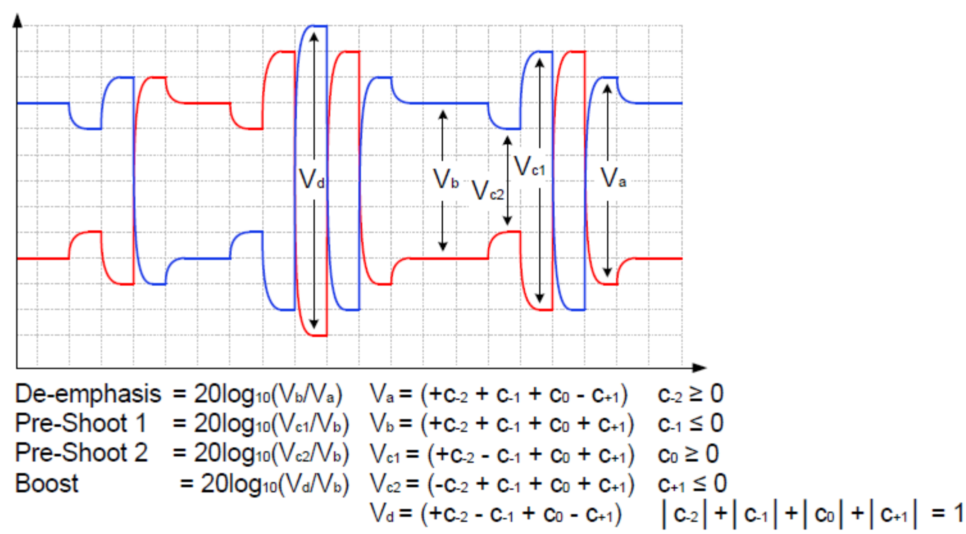


Figure 108 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 146 Preset P1 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P1	0.0	0.0 ±1 dB	–3.5 ± 1 dB	0.000	0.000	–0.167	1.000	0.666	0.666	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P1.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P1 signal in *.bin format.

12 Inputs the P4 and P1 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P1.

14 Reports the measurement of Vb during preset values P1 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), Preshoot Test

This test verifies that the preshoot of the preset number P2 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 147 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

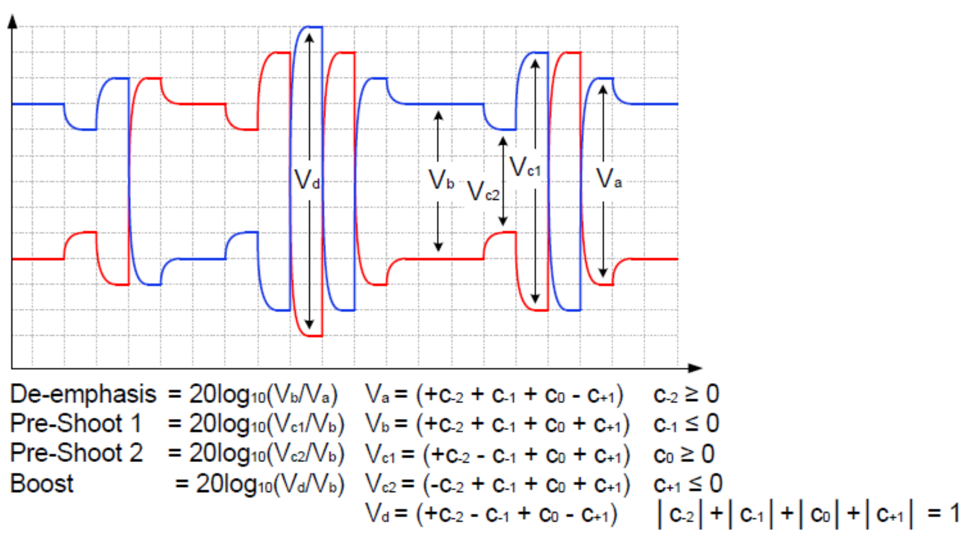


Figure 109 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 148 Preset P2 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P2	0.0	0.0 ±1 dB	-4.4 ±1.5 dB	0.000	0.000	-0.200	1.000	0.600	0.600	0.600

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P2.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P2 signal in *.bin format.

12 Inputs the P4 and P2 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P2.

14 Reports the measurement of Vb during preset values P2 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis Test

This test verifies that the de-emphasis of the preset number P2 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 149 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

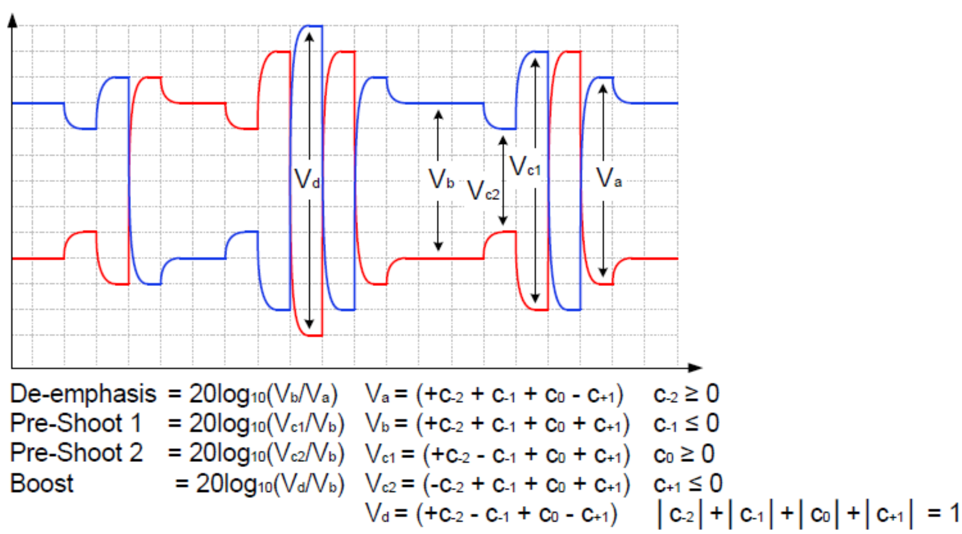


Figure 110 Definition of Tx Voltage Levels and Equalization Ratios

less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 150 Preset P2 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P2	0.0	0.0 ±1 dB	-4.4 ±1.5 dB	0.000	0.000	-0.200	1.000	0.600	0.600	0.600

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain** Scale to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P2.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P2 signal in *.bin format.

12 Inputs the P4 and P2 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P2.

14 Reports the measurement of Vb during preset values P2 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), Preshoot Test

This test verifies that the preshoot of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 151 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

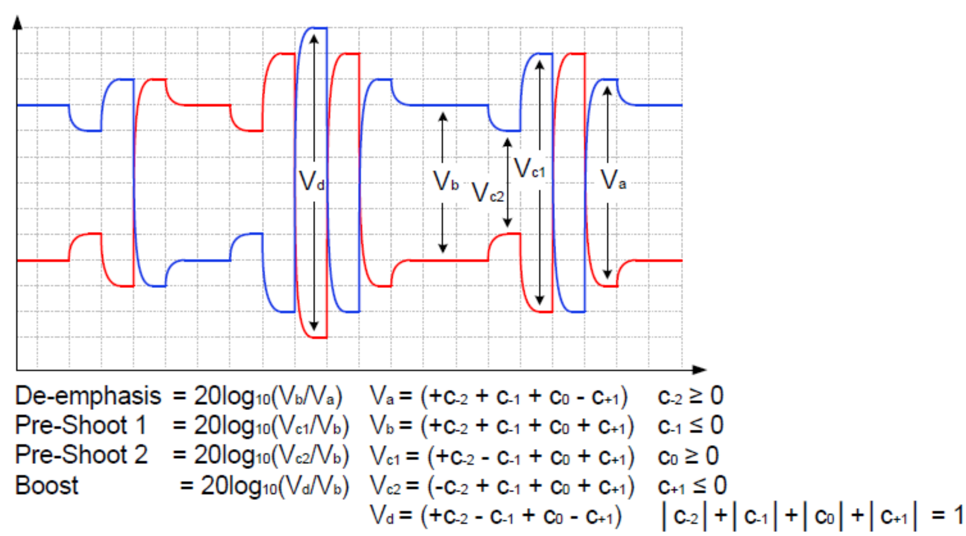


Figure 111 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 152 Preset P3 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P3	0.0	0.0 ±1 dB	-2.5 ±1 dB	0.000	0.000	-0.125	1.000	0.750	0.750	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P3.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P3 signal in *.bin format.

12 Inputs the P4 and P3 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P3.

14 Reports the measurement of Vb during preset values P4 and P3.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

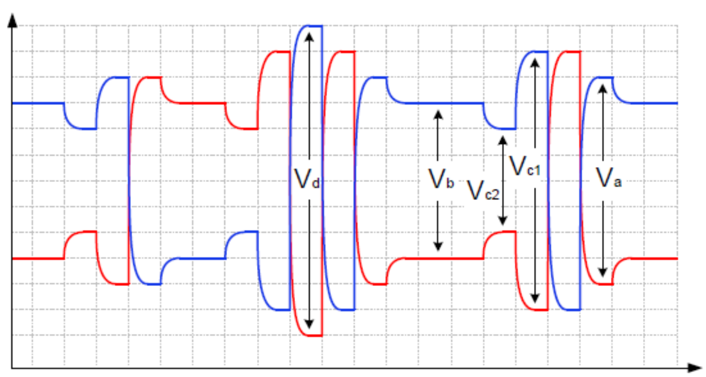
Preset #3 Measurement (P3), De-emphasis Test

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 153 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 112 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 154 Preset P3 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P3	0.0	0.0 ±1 dB	-2.5 ±1 dB	0.000	0.000	-0.125	1.000	0.750	0.750	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P3.
14 Reports the measurement of Vb during preset values P4 and P3.
15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot Test

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 155 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

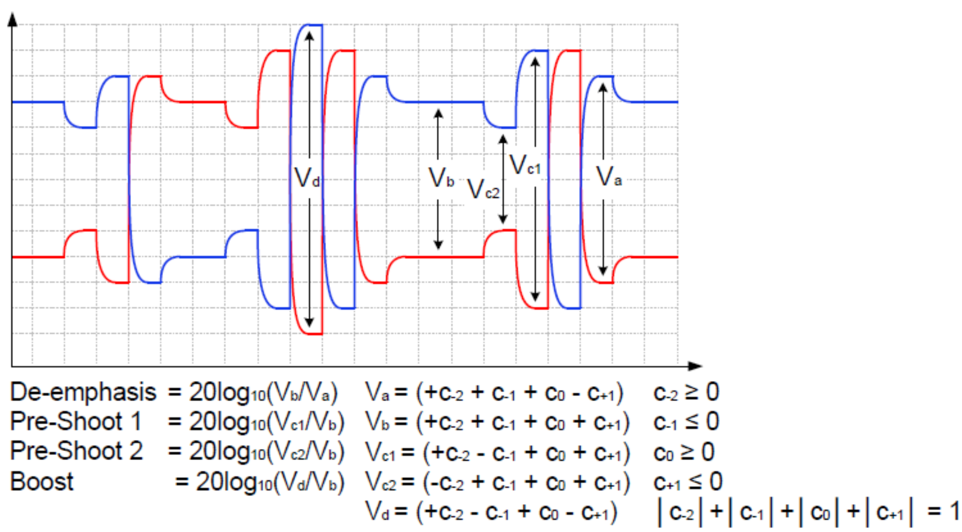


Figure 113 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 156 Preset P5 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P5	0.0	1.9 ±1 dB	0.0 ±1 dB	0.000	-0.100	0.000	0.800	0.800	1.000	0.800

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P5.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P5 signal in *.bin format.

12 Inputs the P4 and P5 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P5.

14 Reports the measurement of Vb during preset values P4 and P5.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), De-emphasis Test

This test verifies that the de-emphasis of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 157 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 158 Preset P5 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P5	0.0	1.9 ±1 dB	0.0 ±1 dB	0.000	-0.100	0.000	0.800	0.800	1.000	0.800

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P5.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P5 signal in *.bin format.

12 Inputs the P4 and P5 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P5.

14 Reports the measurement of Vb during preset values P4 and P5.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot Test

This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 159 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

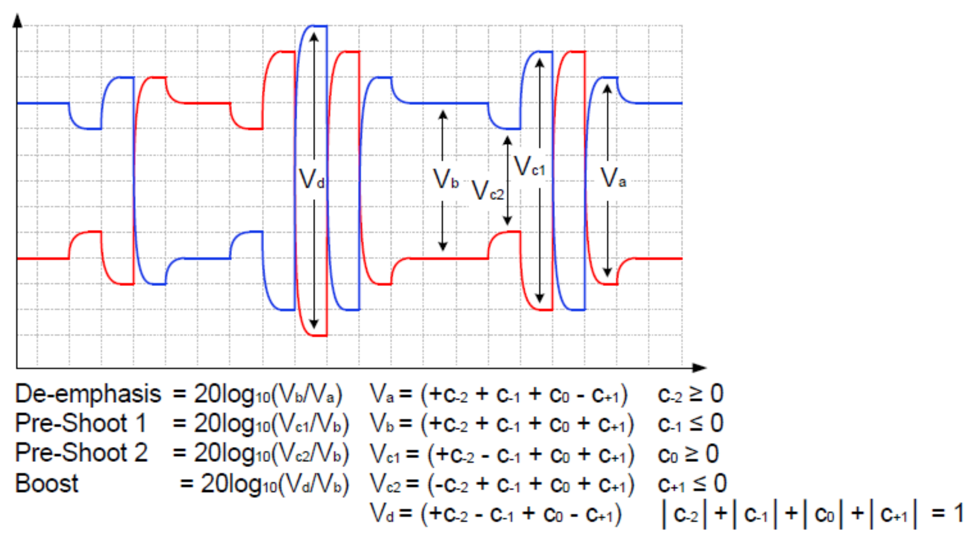


Figure 114 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 160 Preset P6 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P6	0.0	2.5 ±1 dB	0.0 ±1 dB	0.000	-0.125	0.000	0.750	0.750	1.000	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P6.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P6 signal in *.bin format.

12 Inputs the P4 and P6 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P6.

14 Reports the measurement of Vb during preset values P6 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), De-emphasis Test

This test verifies that the de-emphasis of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 161 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

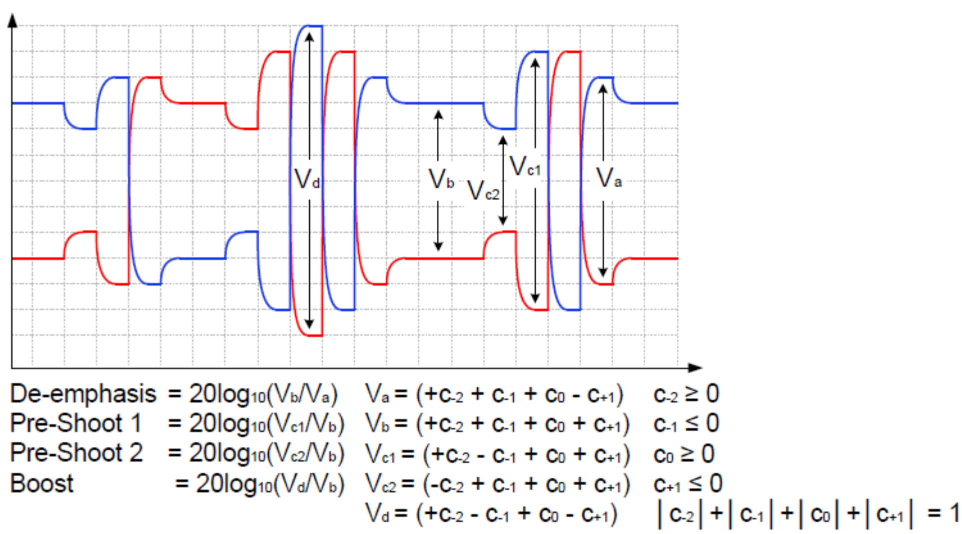


Figure 115 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 162 Preset P6 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P6	0.0	2.5 ±1 dB	0.0 ±1 dB	0.000	-0.125	0.000	0.750	0.750	1.000	0.750

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P6.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P6 signal in *.bin format.

12 Inputs the P4 and P6 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P6.

14 Reports the measurement of Vb during preset values P6 and P4.

15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot Test

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 163 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

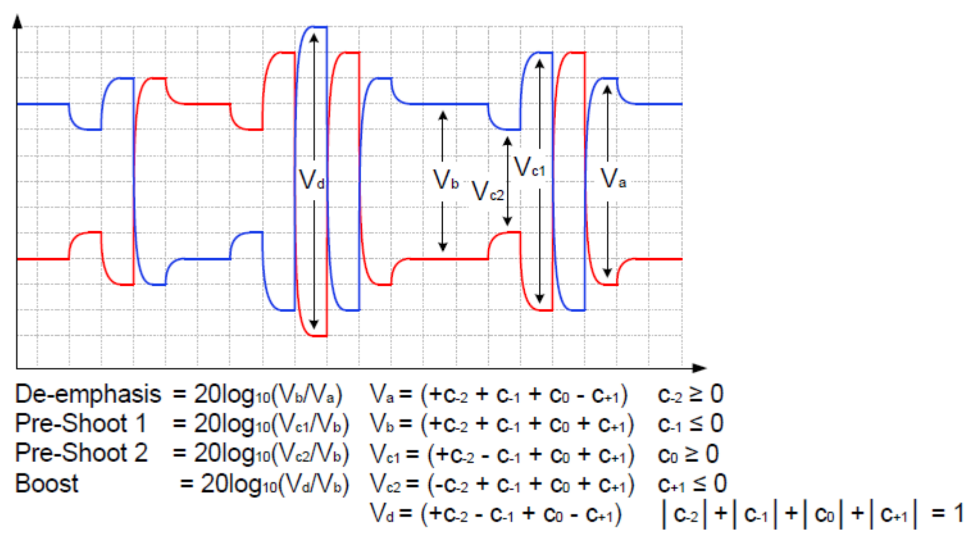


Figure 116 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 164 Preset P7 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P7	0.0	3.5 ±1 dB	-6.0 ±1.5 dB	0.000	-0.100	-0.200	0.800	0.400	0.600	0.400

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P2.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P2 signal into *.bin format.

7 Configures the DUT to operate in preset value #P7.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P7 signal in *.bin format.

12 Inputs the P2 and P7 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P7.

14 Reports the measurement of Vb during preset values P2 and P7.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis Test

This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 165 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

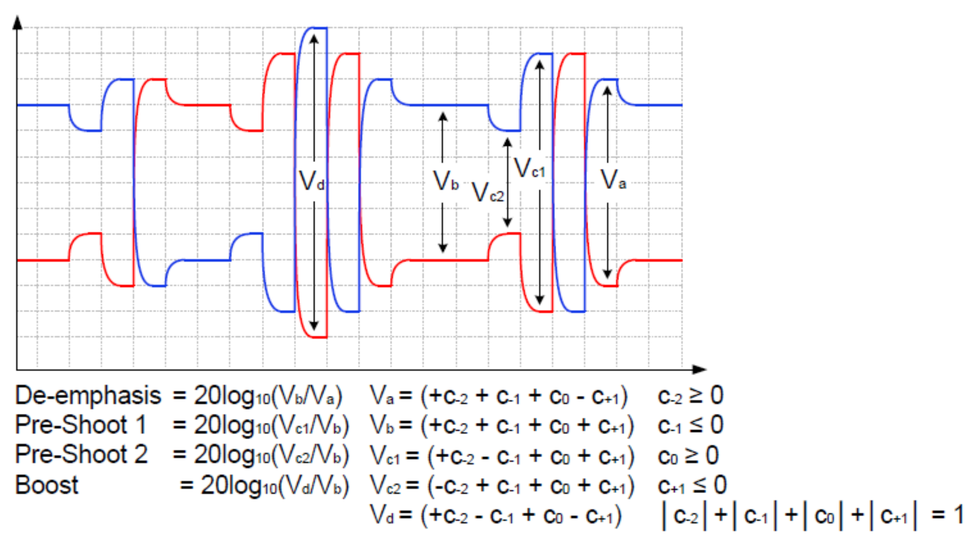


Figure 117 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 166 Preset P7 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P7	0.0	3.5 ±1 dB	-6.0 ±1.5 dB	0.000	-0.100	-0.200	0.800	0.400	0.600	0.400

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P5.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P5 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P5 and P7 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P7.
14 Reports the measurement of Vb during preset values P5 and P7.
15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot Test

This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 167 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

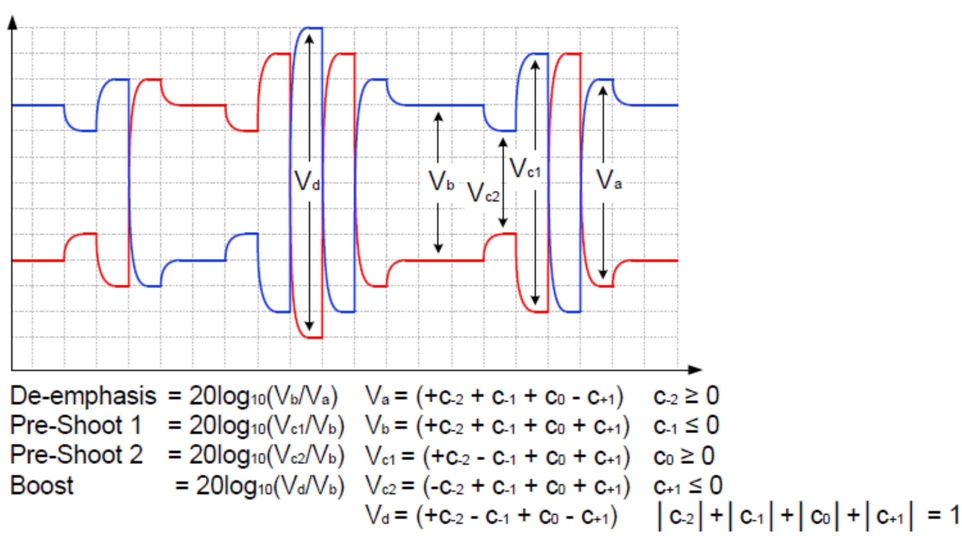


Figure 118 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 168 Preset P8 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P8	0.0	6.0 ±1.0 dB	-3.5 ±1 dB	0.000	-0.125	-0.125	0.750	0.500	0.750	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P3.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P3 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P3 and P8 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P8.
14 Reports the measurement of Vb during preset values P3 and P8.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

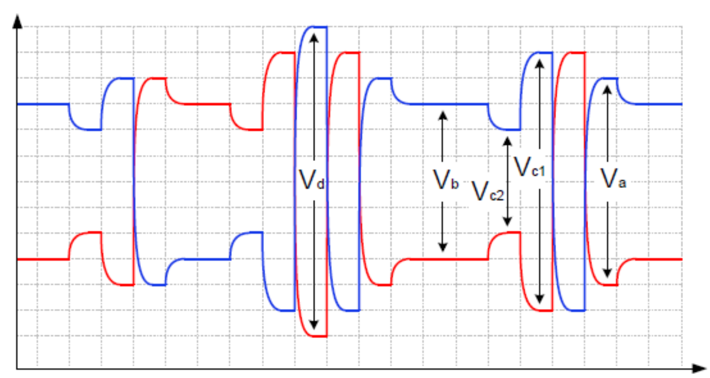
Preset #8 Measurement (P8), De-emphasis Test

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 169 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 119 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 170 Preset P8 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P8	0.0	6.0 ±1.0 dB	-3.5 ±1 dB	0.000	-0.125	-0.125	0.750	0.500	0.750	0.500

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P6.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P6 signal into *.bin format.

7 Configures the DUT to operate in preset value #P8.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P8 signal in *.bin format.

12 Inputs the P6 and P8 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P8.

14 Reports the measurement of Vb during preset values P6 and P8.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

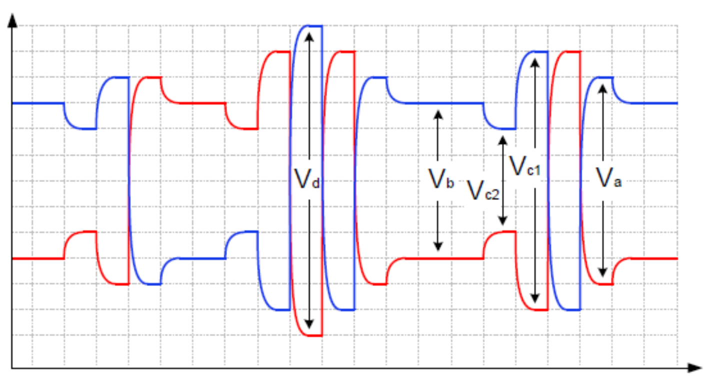
Preset #9 Measurement (P9), Preshoot Test

This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 171 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9



De-emphasis	$= 20\log_{10}(V_b/V_a)$	$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$	$c_{-2} \geq 0$
Pre-Shoot 1	$= 20\log_{10}(V_{c1}/V_b)$	$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$	$c_{-1} \leq 0$
Pre-Shoot 2	$= 20\log_{10}(V_{c2}/V_b)$	$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$	$c_0 \geq 0$
Boost	$= 20\log_{10}(V_d/V_b)$	$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$	$c_{+1} \leq 0$
		$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$	$\lvert c_{-2}\rvert + \lvert c_{-1}\rvert + \lvert c_0\rvert + \lvert c_{+1}\rvert = 1$

Figure 120 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 172 Preset P9 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P9	0.0	3.5 ±1 dB	0.0 ± 1 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P9.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P9 signal in *.bin format.

12 Inputs the P4 and P9 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P9.

14 Reports the measurement of Vb during preset values P9 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

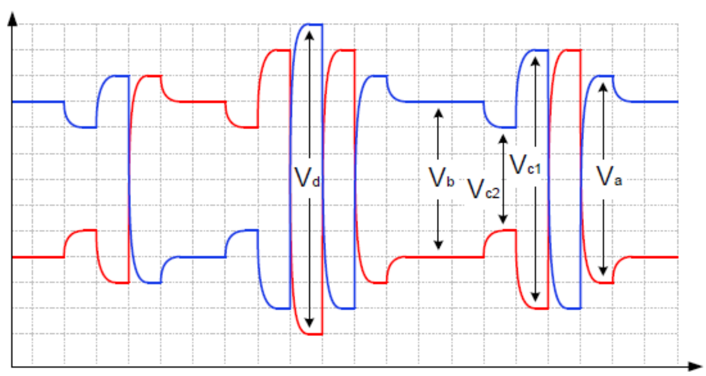
For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), De-emphasis Test

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 173 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 121 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 174 Preset P9 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P9	0.0	3.5 ±1 dB	0.0 ± 1 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.

2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P9.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P9 signal in *.bin format.

12 Inputs the P4 and P9 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P9.

14 Reports the measurement of Vb during preset values P4 and P9.

15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

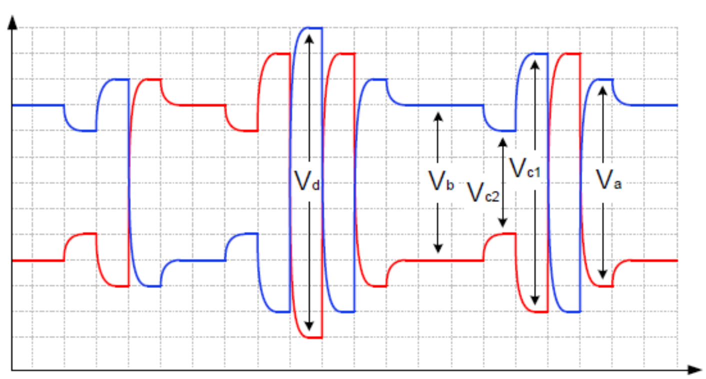
Preset #10 Measurement (P10), Preshoot Test

This test verifies that the preshoot of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 175 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$

Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 122 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 176 Preset P10 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P10	0.0	0.0 ±1 dB	Note 2	0.000	0.000	Note2	1.000	Note2	Note2	Note2

Note 2:
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1is used for testing the boost limit of Transmitter at reduced swing.

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P10 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P10.
14 Reports the measurement of Vb during preset values P4 and P10.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

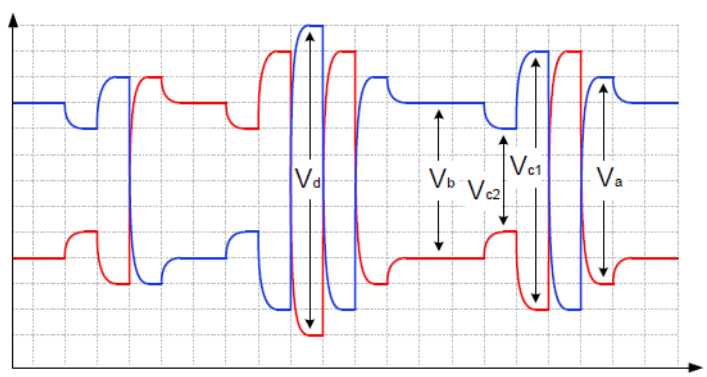
Preset #10 Measurement (P10), De-emphasis Test

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1.

When operating at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s the Tx must support the full range of presets given in Table 8-1 (PCI Express® Base Specification Revision 6.0). When operating at 64.0 GT/s, the Tx must support the full range of presets given in Table 8-2 (PCI Express® Base Specification Revision 6.0). The data rate dependent encoding of presets has been defined in Section 4.2.4.2 of the base spec. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursors (Vc1) and (Vc2) are referred to as pre-shoots, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoots and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when c_{+1}, c_{-2}, and c_{-1} are non-zero, the swing of Va does not reach the maximum as defined by Vd. Figure 8-6 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical.

Table 177 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A



De-emphasis $= 20\log_{10}(V_b/V_a)$ $V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$ $c_{-2} \geq 0$
Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$ $V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{-1} \leq 0$
Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$ $V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$ $c_0 \geq 0$
Boost $= 20\log_{10}(V_d/V_b)$ $V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$ $c_{+1} \leq 0$
$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$ $|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 123 Definition of Tx Voltage Levels and Equalization Ratios

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 178 Preset P10 Ratios and Corresponding Coefficient Values for 8.0, 16.0, and 32.0 GT/s

Preset No.	Preshoot 2 (dB)	Preshoot 1 (dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
P10	0.0	0.0 ±1 dB	Note 2	0.000	0.000	Note2	1.000	Note2	Note2	Note2

Note 2:
P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1is used for testing the boost limit of Transmitter at reduced swing.

Notes from the Specification

1 Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2 P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training (see Section 4.2.4.1 of the base spec). P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-Series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P10 saved waveform into SigTest tool.

13 Computes the de-emphasis at preset value P10.
14 Reports the measurement of Vb during preset values P10 and P4.
15 Compares the de-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

34 Reference Clock Tests, 32.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 32.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

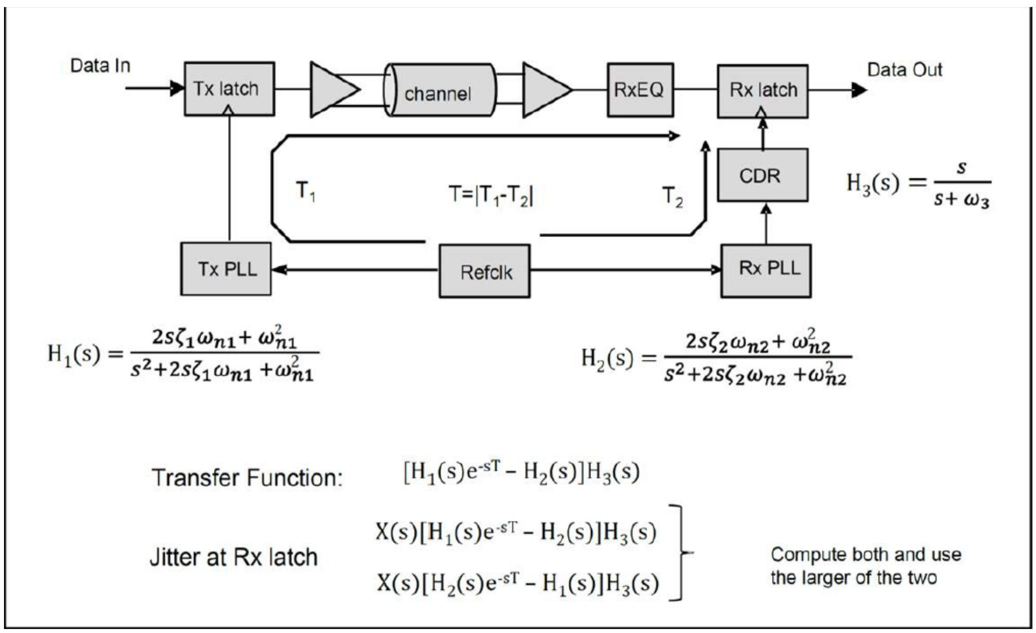
NOTE In case of Z-series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 6.0 compliance testing.

Reference Clock Architectures

For 32.0 GT/s, PCI-E 6.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.
At 32.0 GT/s the only difference in the figure is the “behavioral CDR transfer function” as defined in PCI Express Base Specification.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC	CDR

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

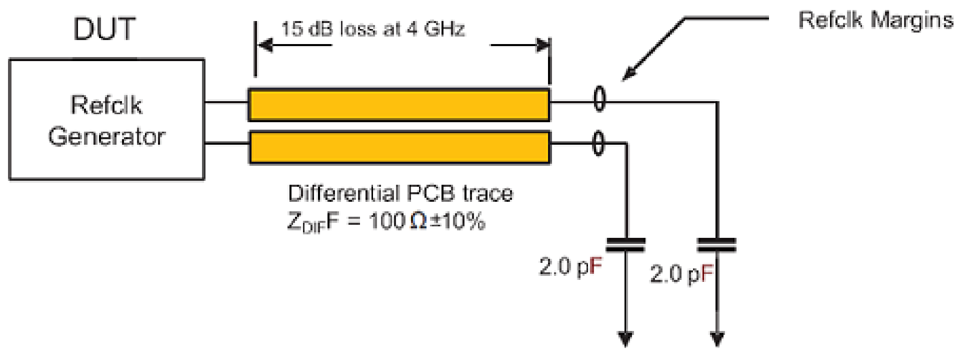


Figure 124 Driver Compliance Test Load

For 32.0 and 64.0 GT/s, the reference clock jitter is measured with an oscilloscope, and is tested with the reference clock terminated by 50 Ohm terminations without a channel.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 32.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

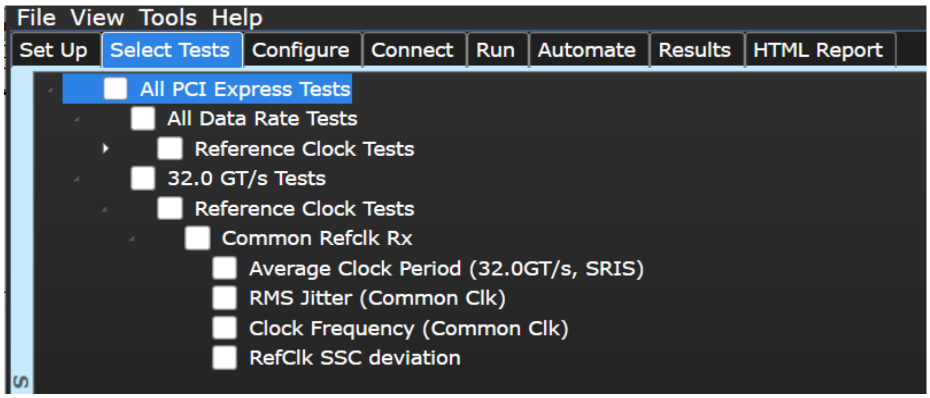


Figure 125 Selecting Reference Clock Tests when SSC is Selected with SRIS mode enabled.

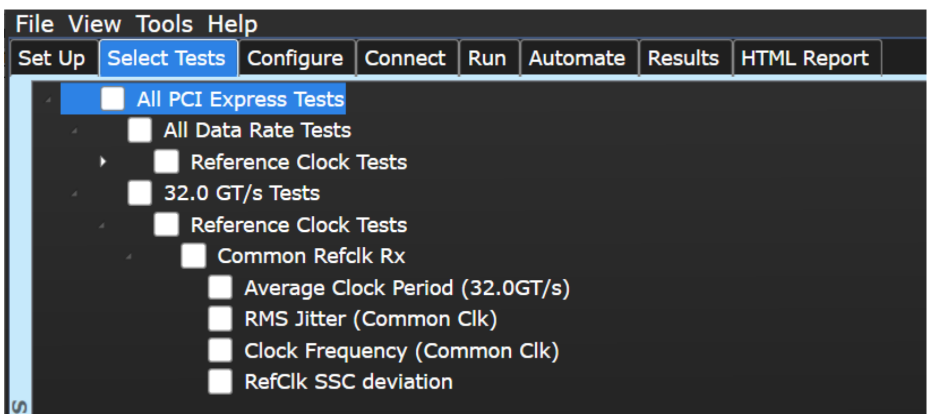


Figure 126 Selecting Reference Clock Tests when SSC Selected without SRIS Mode

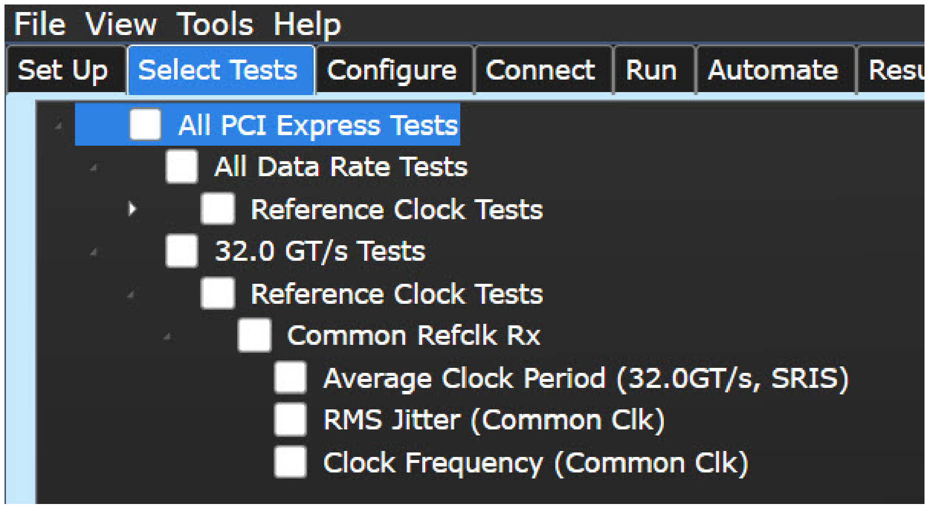


Figure 127 Selecting Reference Clock Tests when Clean Clock is Selected with SRIS Mode enabled.

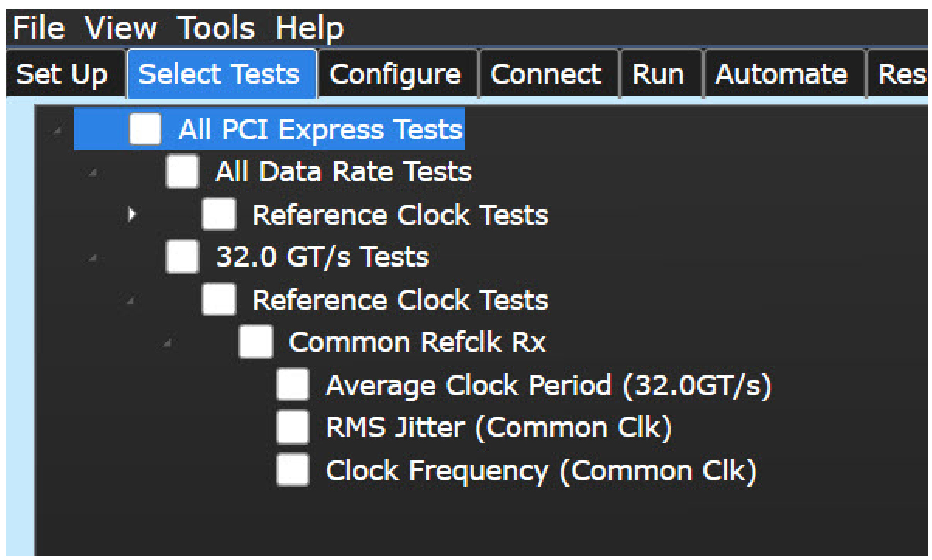


Figure 128 Selecting Reference Clock Tests when Clean Clock is Selected without SRIS Mode.

Average Clock Period Test (32.0 GT/s)

This test verifies that the Refclk Average Clock Period (32 GT/s) is within the conformance limits as specified in PCIE Express Base Specification.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC, there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 32.0GT/s speed.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 (REFCLK DC Specifications and AC Timing Requirements) is used as reference to check the compliance of the DUT.

Table 179 Average Clock Period Test Details

		100 MHz Input	
Symbol	**Parameter**	**Min**	**Max**
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	+2800 ppm
$T_{PERIOD\ AVG\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices that support 32.0 and 64.0 GT/s in CC Mode at any speed	-100 ppm	+2600 ppm
$T_{PERIOD\ AVG\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices that support 32.0 and 64.0 GT/s in SRIS Mode at any speed	-100 ppm	+1600 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Configures memory depth and sampling rate as per the data rate.
4 Fits and displays all sample data on screen.
5 Measures the average voltage using **V average** measurement.
6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7 Measures the average frequency using **Frequency** measurement of **Clock**.
8 Measures the average period using **Period** measurement of **Clock**.
9 Computes the difference between ideal and actual frequency in terms of parts per million of 100 MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

For SSC Mode,

-300 ppm ≤ Average Clock Period Accuracy ≤ +2800 ppm

For Clean Clock,

-100 ppm ≤ Average Clock Period Accuracy ≤ +2600 ppm

For SRIS Mode,

-100 ppm ≤ Average Clock Period Accuracy ≤ +1600 ppm

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

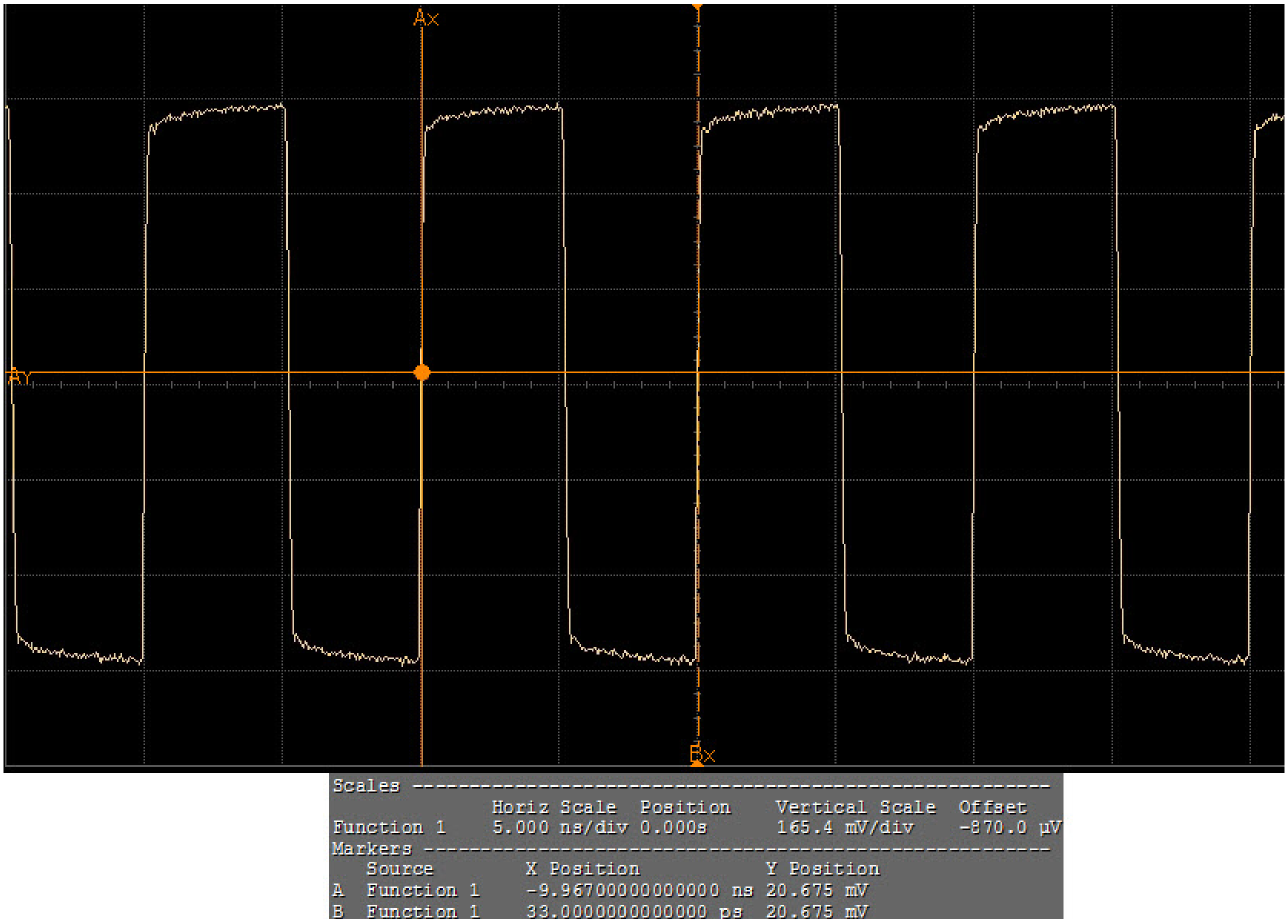


Figure 129 Reference Image for Average Clock Period

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 180 RMS Jitter Test Details

Symbol	Description	Value
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.15 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.
- For the 16.0, 32.0, and 64.0 GT/s CC measurements SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
- Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

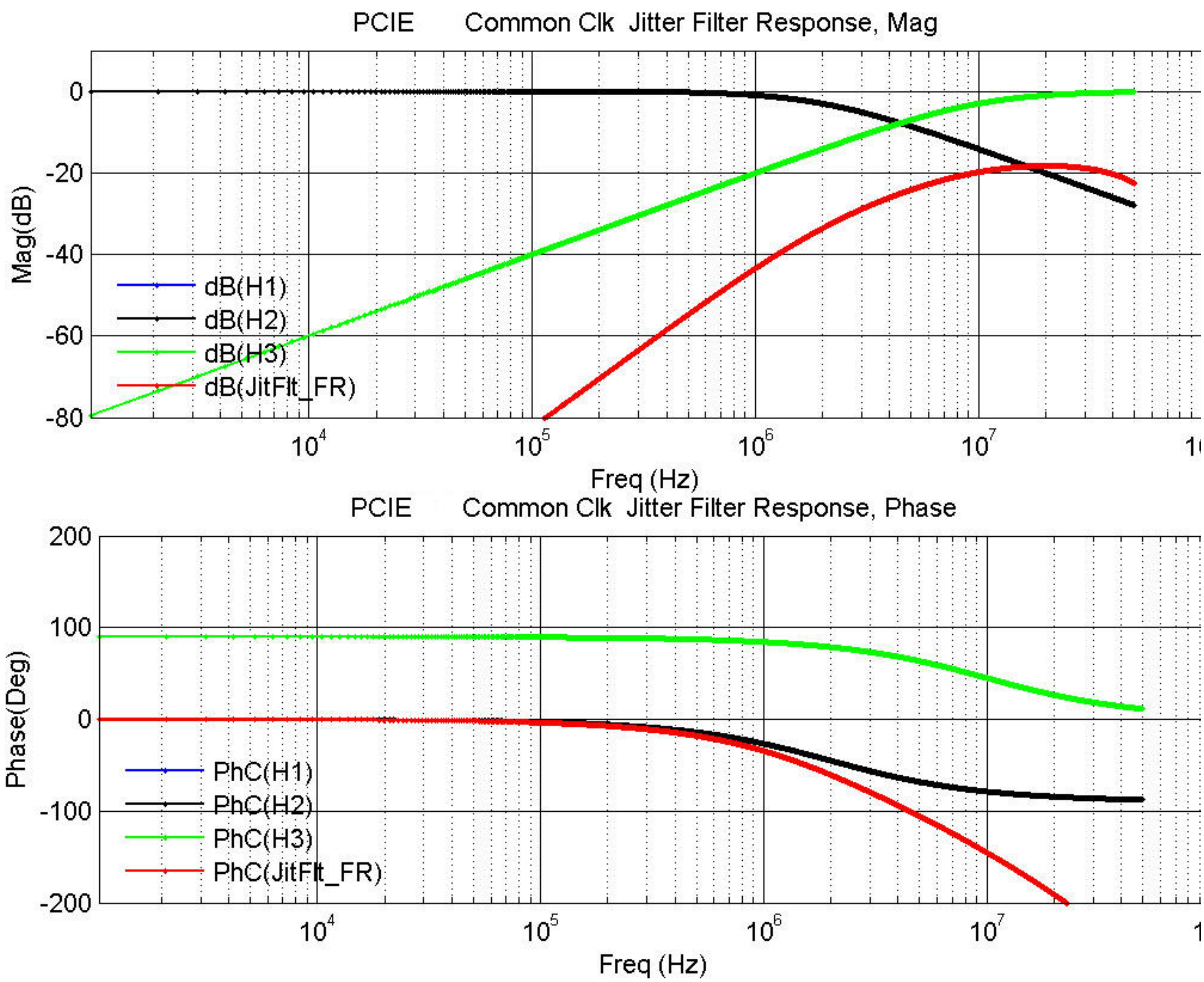


Figure 130 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

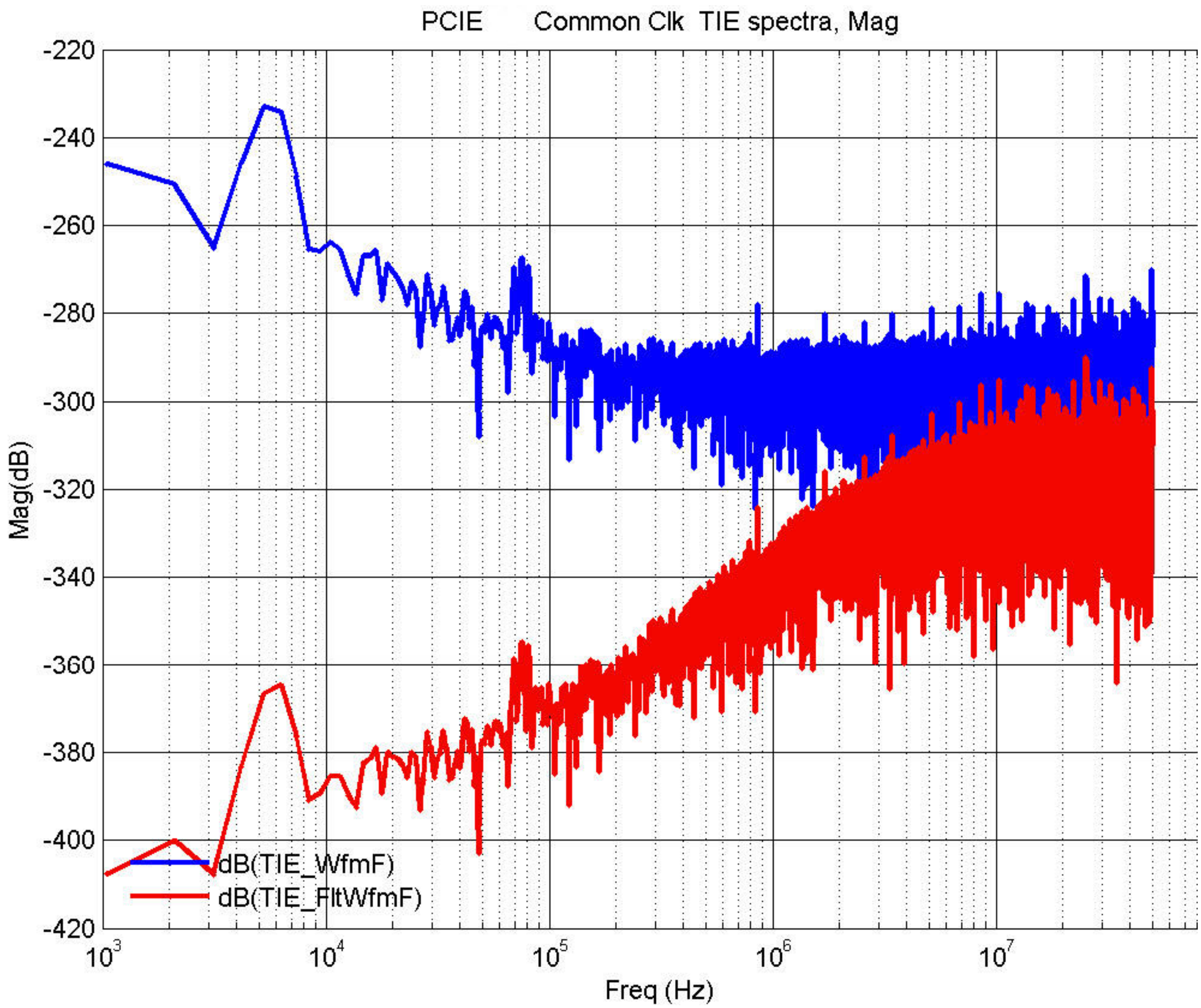


Figure 131 Reference Image for Common Clock TIE Spectra RMS Jitter Test

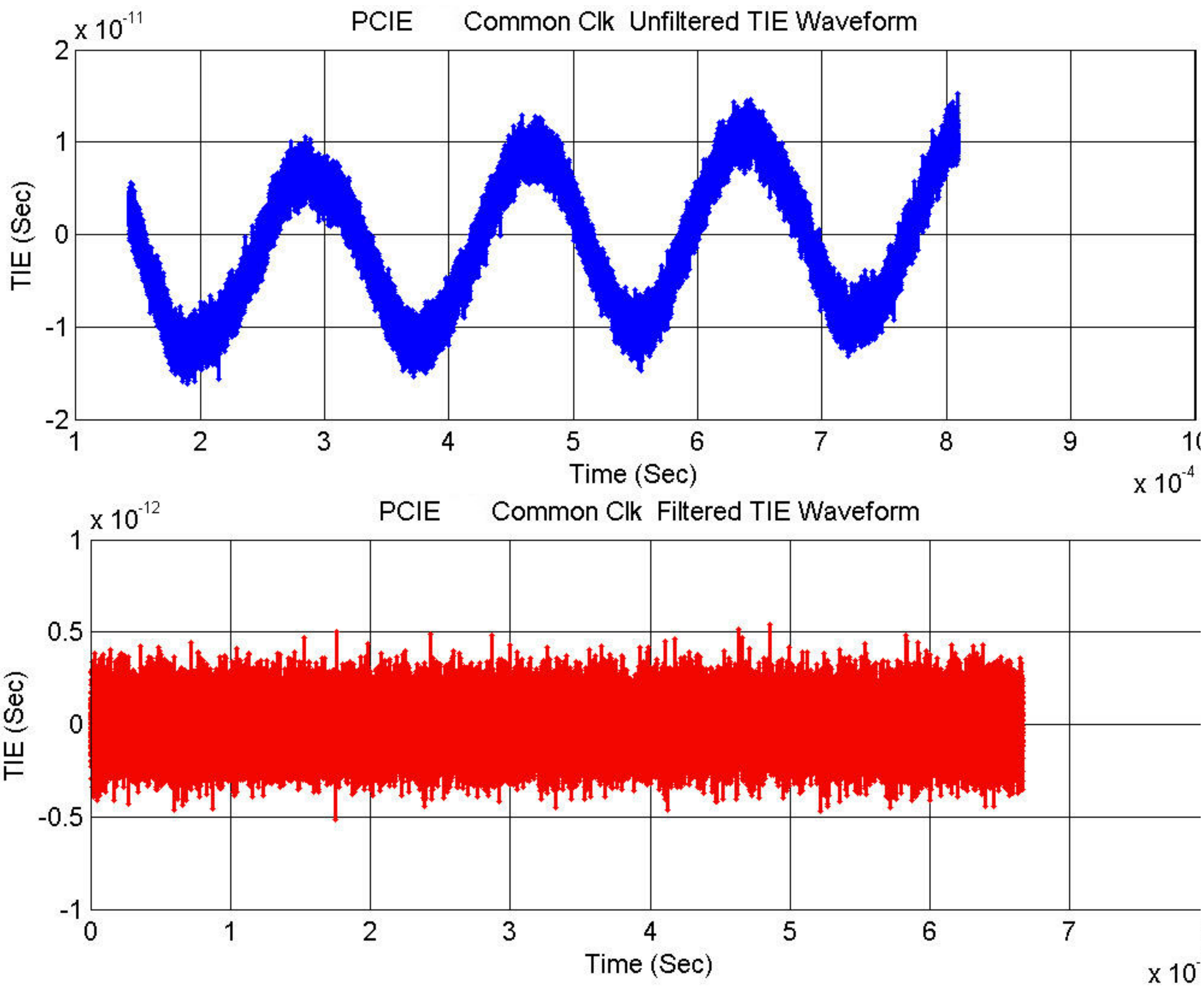


Figure 132 Reference Image for TIE Waveform RMS Jitter Test

Clock Frequency (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in the PCIE Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.3, Table 8-18 is used as reference to check the compliance of the DUT.

Table 181 RMS Jitter Test Details

Symbol	Description	Min	Max
FREFCLK_32G_64G	Ref Clock Frequency (Common Clk)	99.99 MHz	100.01 MHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 1044 and select **Clock Frequency (Common Clk) (Data Clk).**

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Sets the time scale to 5 ns.
5 Fits and displays all sample data on the screen.
6 Enables jitter analysis so that measurements are made on all edges.
7 Measures the clock frequency.
8 Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part XIV
PCI Express Gen6 64.0 GT/s Tests

35 Transmitter (Tx) Tests, 64.0 GT/s, PCI-E 6.0

This section provides the Methods of Implementation (MOIs) for PCI-E 6.0 Transmitter (Tx) tests at 64.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

KEYSIGHT TECHNOLOGIES

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.3.1, Figure 8-1.

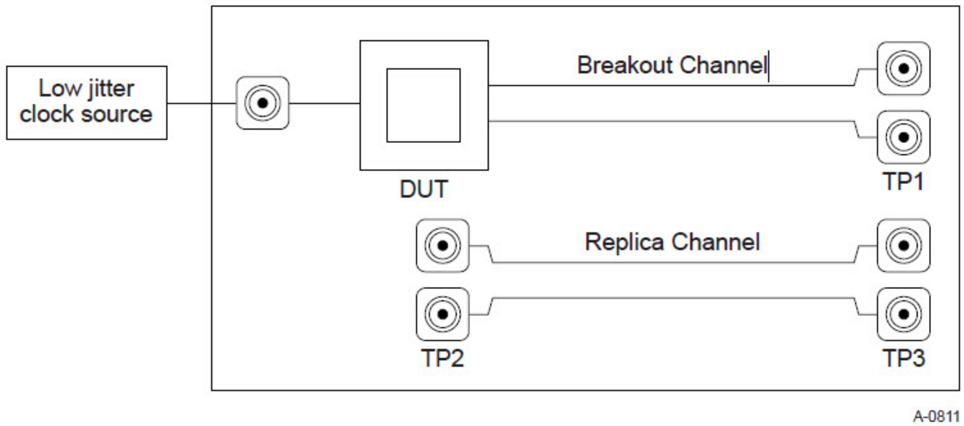


Figure 1 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. In the **Select Tests** tab, navigate to **All PCI Express Tests > 64.0 GT/s Tests > Transmitter (Tx) Tests**.

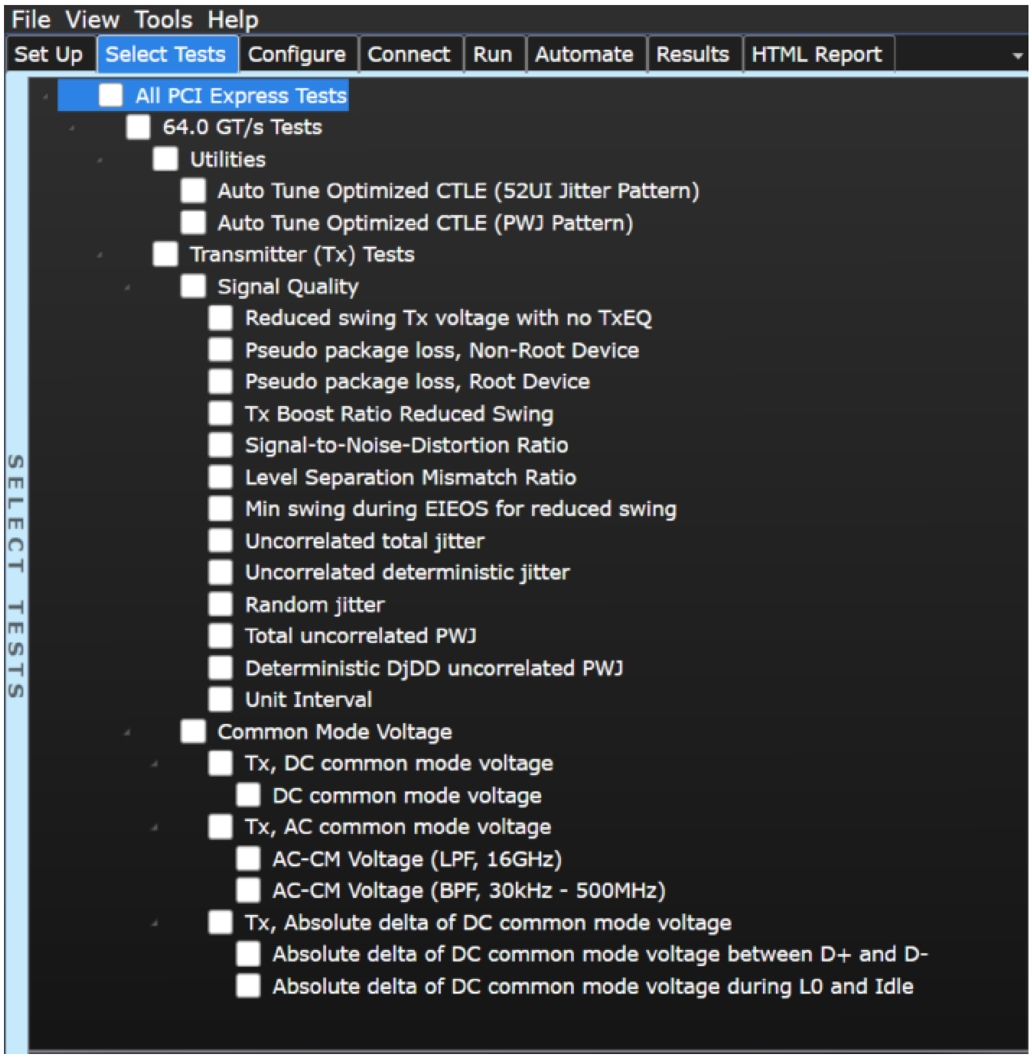


Figure 2 Selecting Transmitter (Tx) Tests

Auto Tune Optimized CTLE (52 UI Jitter Pattern) (Information Only)

This test finds optimized CTLE equalization value for 52 UI jitter pattern by referring to the lowest T_{TX-RJ} value calculated in range of CTLE equalization values (-5 dB to -15 dB).

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.5.2.

Understanding the Test Flow

1. Iterates through the range of CTLE Equalization from -5 dB to -15 dB and identifies the optimized CTLE Equalization value that returns the lowest T_{TX-RJ} value using 12-Edge Jitter measurement.
2. The identified value will be automatically set in **Device definition > CTLE Equalization > 52UI Jitter Pattern** section and ready to be applied in subsequent run.

NOTE This test will be visible if and only if Auto Tune check box is checked in **Device definition > CTLE Equalization > 52UI Jitter Pattern** section.

Viewing Test Results

For each test trial, its result is displayed in the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, please refer to **Viewing Results** in the online help.

Auto Tune Optimized CTLE (PWJ Pattern) (Information Only)

This test finds optimized CTLE Equalization value for PWJ pattern by referring to the lowest $T_{TX\text{-}UPW\text{-}TJ}$ value calculated in range of CTLE equalization values (-5 dB to -15 dB).

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.5.2.

Understanding the Test Flow

1 Iterates through the range of CTLE Equalization from -5 dB to -15 dB and identifies the optimized CTLE Equalization value that returns the lowest $T_{TX\text{-}UPW\text{-}TJ}$ value using jitter measurement.

2 The identified value will be automatically set in **Device definition > CTLE Equalization > PWJ Pattern** section and ready to be applied in subsequent run.

Viewing Test Results

For each test trial, its result is displayed in the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, please refer to Viewing **Results** in the online help.

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 3. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP}$ is used as reference to check the compliance of the DUT.

Table 1 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP}$	Full swing Tx voltage with no TxEQ	800 mV	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2 \times |V_{TXD+} - V_{TXD-}|$
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

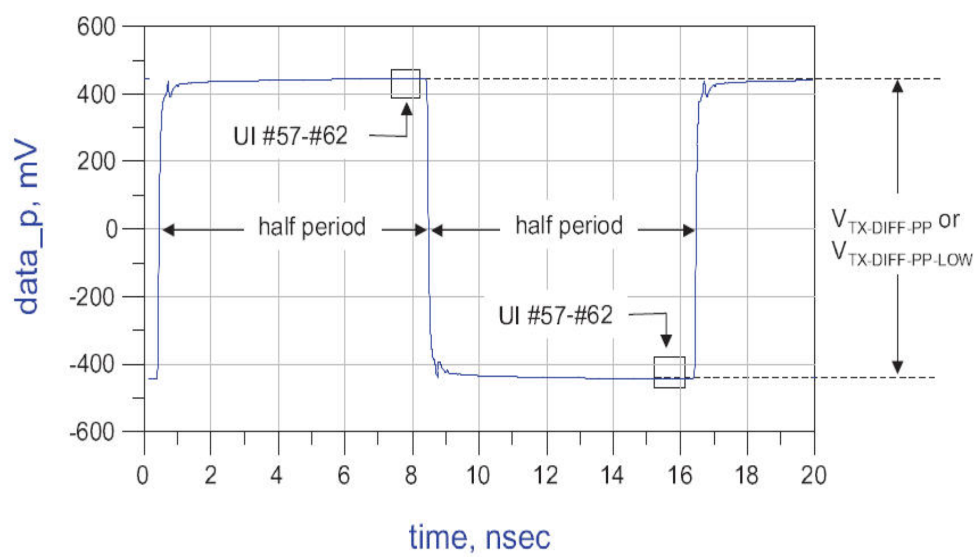


Figure 3 $V_{TX-DIFF-PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 20.0 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Compares the peak to peak voltage value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in PCIE Base Specification. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 4. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 2 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP-LOW}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1000 mVPP

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as 2 × | V_{TXD+}-V_{TXD-}|
- See Section 8.3.3.6 and Section 8.3.3.7 for measurement details.

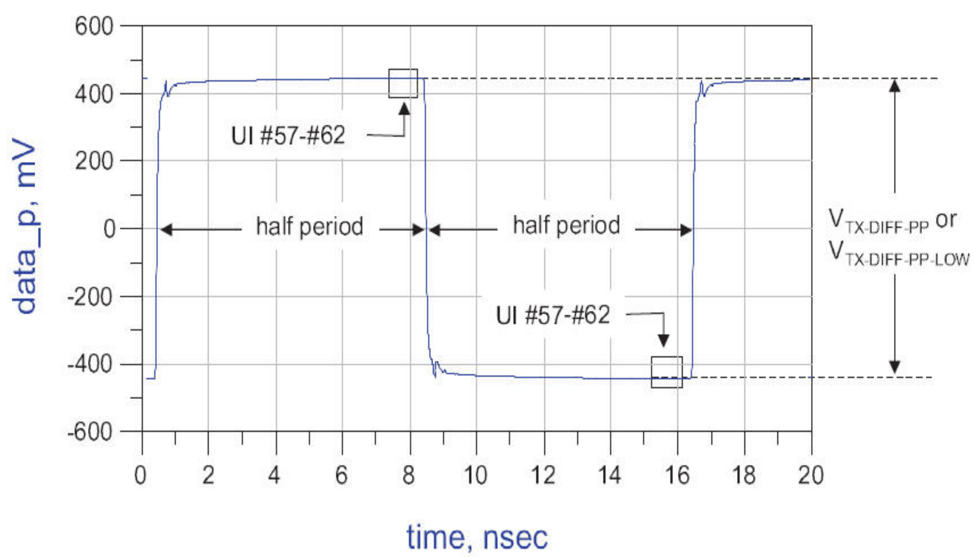


Figure 4 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Compares the peak to peak voltage value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test (Non-Root Device)

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

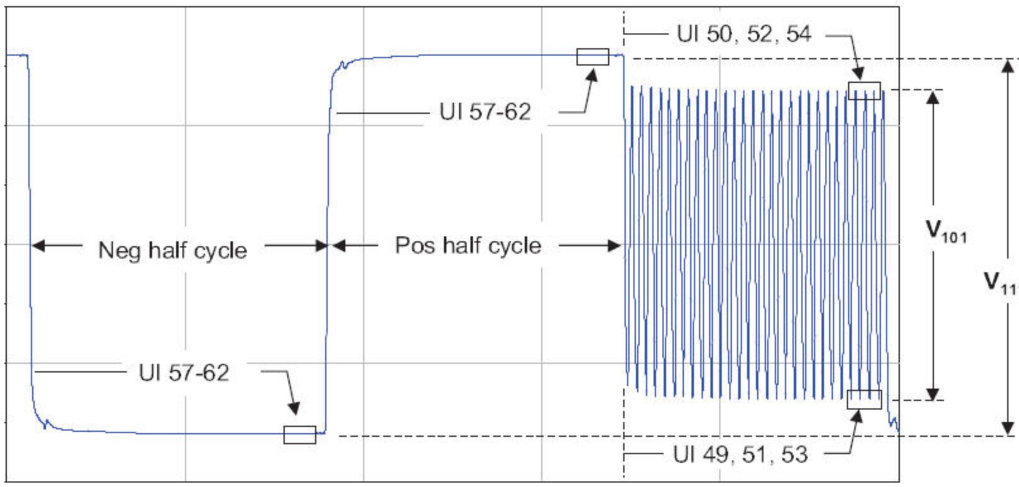
PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 3 Pseudo Package Loss Test Details

Symbol	Parameter	Min
$ps21_{TX-ROOT-DEVICE}$	Pseudo package loss for a device containing root ports	-7.5 dB
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss for all devices not containing root ports	-3.7 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 5 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 MATLAB will analyze the saved waveform by comparing the 64-zeros/64-ones voltage swing (v111) against a 1010 pattern (V101).
4 Reports the package loss ratio value.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test (Root Device)

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

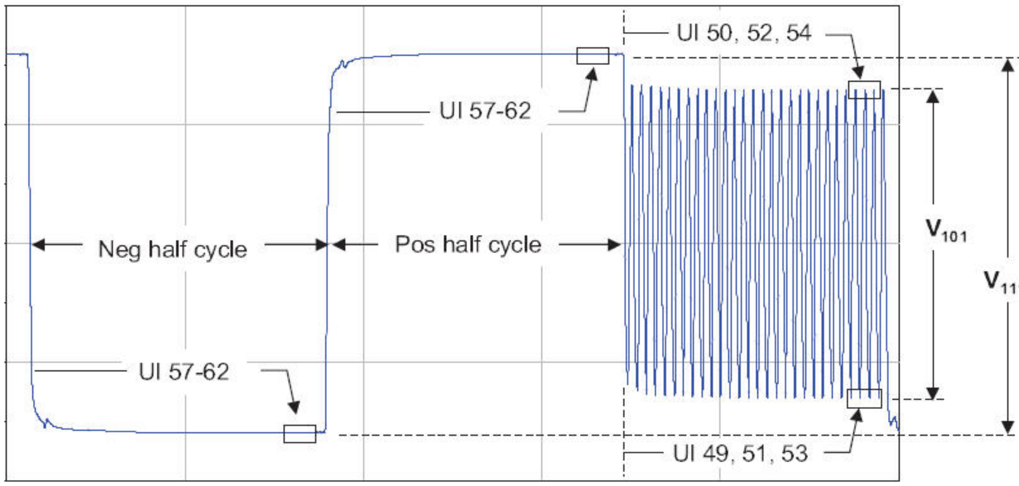
PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 4 Pseudo Package Loss Test Details

Symbol	Parameter	Min
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	-7.5 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	-3.7 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 6 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 MATLAB will analyze the saved waveform by comparing the 64-zeros/64-ones voltage swing (v111) against a 1010 pattern (V101).
4 Reports the package loss ratio value.
5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Full Swing Test

This test verifies that the maximum nominal Tx boost ratio for full swing, $V_{TX-BOOST-FS}$ is within the allowed range. This test requires Preset Q00 and Preset Q10.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 5 **Tx Boost Ratio Full Swing Test Details**

Symbol	Parameter	Min	Max
$V_{TX-BOOST-FS}$	Maximum nominal Tx boost ratio for full swing	6.5 dB	9.5 dB

Test Definition Notes from the Specification

- Nominal boost beyond 8.0 dB is limited to guarantee that ps21 TX limits are satisfied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the Horizontal Domain Scale to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q10.
8 Configures memory depth as per the data rate. Sampling rate is set through the Configure tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the Horizontal Domain Scale to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q10 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q10 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in specification's Figure 8-6.
14 Compares Boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Tx Boost Ratio Reduced Swing Test

This test verifies that the maximum nominal Tx boost ratio for reduced swing, $V_{TX-BOOST-RS}$ is within the allowed range. This test required Preset Q00 and Preset Q04.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 6 Tx Boost Ratio Reduced Swing Test Details

Symbol	Parameter	Min	Max
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	1.5 dB	3.5 dB

Test Definition Notes from the Specification

- Assumes ±1.0 dB tolerance from diagonal elements in Figure 8-9 (Base Spec, Rev 6.0).

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern as defined in the specification.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate at preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the Configure tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the Horizontal Domain Scale to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q4.
8 Configures memory depth as per the data rate. Sampling rate is set through the Configure tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the Horizontal Domain Scale to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q4 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q4 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in specification's Figure 8-6.
14 Compares Boost value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Signal to Noise Distortion Ratio Test

This test verifies that the Signal-to-Noise-Distortion Ratio is within the allowed range. This test required Preset 00.

Signal-to-noise and distortion ratio (SNDR) is measured at the transmitter output using the Compliance Pattern (see Section 4.2.14) with preset Q_0 (no Tx equalization), and the lanes not under test also transmitting the Compliance Pattern with preset Q_0. The recorded waveform must have a minimum of 250 repetitions of the compliance pattern. Measurements should be made with a 4^{th} order Bessel-Thomson filter with a roll-off from DC value by 3.0 dB at 33 GHz to minimize the impact of scope high-frequency noise. The minimum scope bandwidth is 50 GHz.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 7 Signal to Noise Distortion Ratio Test Details

Symbol	Parameter	Min
$SNDR_{TX}$	Signal-to-Noise-Distortion Ratio	34.0 dB

Test Definition Notes from the Specification

- See Section 8.3.3.12 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting preset Q0 compliance pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Loads the saved waveform into oscilloscope and sets required signal type, measurement threshold and clock recovery method.
8 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
9 Sets Pulse Length (Np), Pulse Delay (Dp), and Samples per PAM4 Symbol (M) according to specification.
10 Computes SNDR according to PCIe6 standard as mentioned in specification (section 8.3.3.12).
11 Compares the SNDR value with the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Level Separation Mismatch Ratio Test

This test verifies that the Level Separation Mismatch Ratio is within the allowed range. This test required Preset 00.

Transmitter linearity is defined as a function of the mean signal levels (V_0, V_1, V_2, and V_3) transmitted for PAM4 2-bit symbols. The ratio of level mismatch, R_{LM}, is defined as shown below:

V_{mid} = $(V_0 + V_3) / 2$

ES_1 = $(V_1 - V_{mid}) / (V0 - V_{mid})$

ES_2 = $(V_2 - V_{mid}) / (V3 - V_{mid})$

R_{LM} = $\min((3 \times ES_1), (3 \times ES_2), (2 - 3 \times ES_1), (2 - 3 \times ES_2))$ Equation 8-8

The mean signal levels (V_L where L = 0, 1, 2, and 3) described above are measured by following the same procedure described in section 8.3.3.12 of the PCIe6 base specification, and by using the following equation.

$$V_{L,i} = \frac{\sum_{i=1}^{8} \mu_{L,i}}{8}$$

Figure 7 Equation 8-9 of the PCIe6 Base Specification

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 8 Level Separation Mismatch Ratio Test Details

Symbol	Parameter	Min
$R_{LM\text{-}TX}$	Level Separation Mismatch Ratio	950.0 m

Test Definition Notes from the Specification

See Section 8.3.3.13 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting preset Q0 compliance pattern.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth and sampling rate as per the data rate.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Loads the saved waveform into oscilloscope and sets required signal type, measurement threshold, and clock recovery method.
8. Performs scope random noise removal using the random noise values obtained from scope noise calibration.
9. Computes each of the mean signal levels (V_L) by using Equation 8-9 of the PCIe6 Base Specification.
10. Computes the RLM value (with the computed mean signal levels (V_L)) as shown in the equation 8-8 of the PCIe6 Base Specification.
11. Computes the RLM value according to PCI Express Base Specification.
12. Compares the RLM value with the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ is measured using the EIEOS sequence contained within the compliance pattern. At 64.0 GT/s the EIEOS pattern consists of 32 UI consecutive voltage level 3's followed by 32 UI consecutive voltage level 0's.

A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X\text{-}EIEOS\text{-}FS}$ is measured with a preset number Q10 for 64.0 GT/s. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with preset Q4 for 64.0 GT/s.

A Transmitter is not always permitted to generate the maximum boost level noted above. A Transmitter that cannot drive significantly more than 800mVPP is limited by the need to meet $V_{TX\text{-}EIEOS\text{-}FS}$. The Tx must reject any adjustments to its presets or coefficients that would violate the $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ limits. The EIEOS voltage limits are imposed to guarantee the EIEOS threshold of 175mVPP at the Rx pin. Figure 8 illustrates the de-emphasis peak as observed at the pin of a Tx for $V_{TX\text{-}EIEOS\text{-}FS}$. At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s, UI number 5-14 at 16.0 GT/s, and UI number 9-28 at 32.0 and 64.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform over 500 repetitions of the compliance pattern. $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 9 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

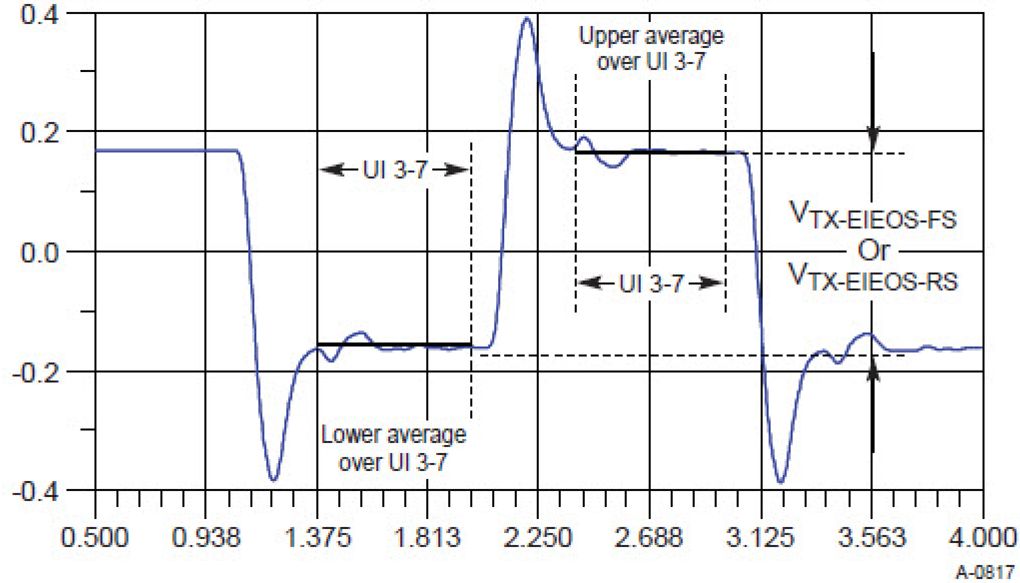


Figure 8 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5 M UI).
3 Gets the average EIEOS high voltage.
4 Gets the average EIEOS low voltage.
5 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ is measured using the EIEOS sequence contained within the compliance pattern. At 64.0 GT/s the EIEOS pattern consists of 32 UI consecutive voltage level 3's followed by 32 UI consecutive voltage level 0's.

A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number Q10 for 64.0 GT/s. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset Q4 for 64.0 GT/s.

A Transmitter is not always permitted to generate the maximum boost level noted above. A Transmitter that cannot drive significantly more than 800mVPP is limited by the need to meet $V_{TX-EIEOS-FS}$. The Tx must reject any adjustments to its presets or coefficients that would violate the $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ limits. The EIEOS voltage limits are imposed to guarantee the EIEOS threshold of 175mVPP at the Rx pin. Figure 8 illustrates the de-emphasis peak as observed at the pin of a Tx for $V_{TX-EIEOS-FS}$. At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s, UI number 5-14 at 16.0 GT/s, and UI number 9-28 at 32.0 and 64.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform over 500 repetitions of the compliance pattern. $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 10 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, 32.0, and 64.0 GT/s that ensures that these parameters are met.

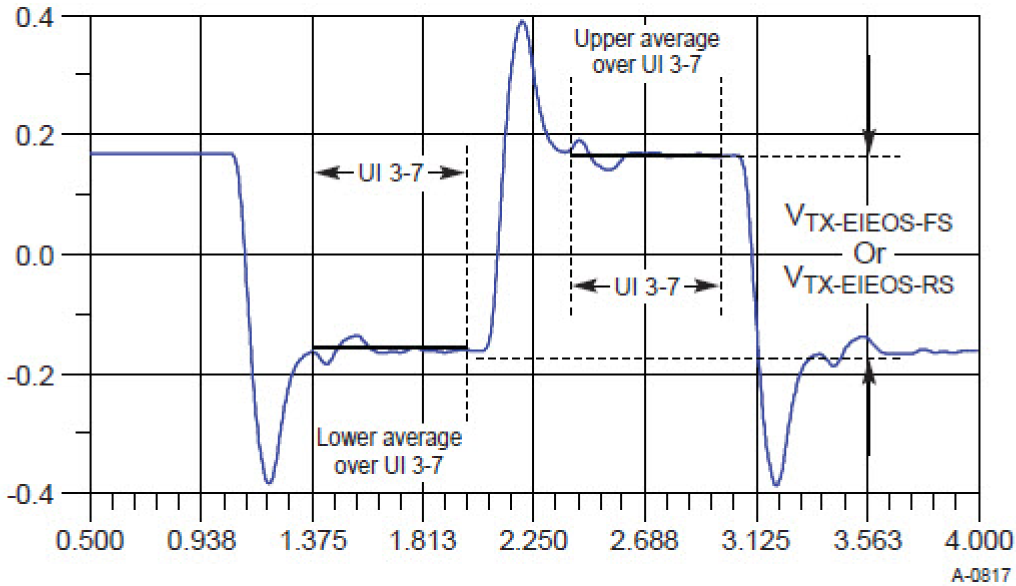


Figure 9 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Gets the average EIEOS high voltage.
4 Gets the average EIEOS low voltage.
5 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 11 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	4.0 ps PP at 10^{-6}

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
4 For 64.0 GT/s, uses the Jitter Measurement Pattern (see Section 4.2.16 of the base spec) with no Tx equalization for measuring the uncorrelated total jitter and the uncorrelated deterministic jitter for all twelve transitions between the four PAM4 voltage levels.
5 As the 64.0 GT/s Jitter Measurement Pattern is 52-UI long and all 12 PAM4 transitions repeat four times within the pattern resulting in 48 edge transitions, it measures jitter on each of the 48 edges individually, and then averages.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 12 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	1.563 ps PP

Test Definition Notes from the Specification

See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
4 For 64.0 GT/s, uses the Jitter Measurement Pattern (see Section 4.2.16 of the base spec) with no Tx equalization for measuring the uncorrelated total jitter and the uncorrelated deterministic jitter for all twelve transitions between the four PAM4 voltage levels.
5 As the 64.0 GT/s Jitter Measurement Pattern is 52-UI long and all 12 PAM4 transitions repeat four times within the pattern resulting in 48 edge transitions, it measures jitter on each of the 48 edges individually, and then averages.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test (Information Only)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 13 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	Info Only

Test Definition Notes from the Specification

- Informative parameter only. Range of Rj possible with zero to maximum allowed $T_{TX-UDJDD}$.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
4 For 64.0 GT/s, uses the Jitter Measurement Pattern (see Section 4.2.16 of the base spec) with no Tx equalization for measuring the uncorrelated total jitter and the uncorrelated deterministic jitter for all twelve transitions between the four PAM4 voltage levels.
5 As the 64.0 GT/s Jitter Measurement Pattern is 52-UI long and all 12 PAM4 transitions repeat four times within the pattern resulting in 48 edge transitions, it measures jitter on each of the 48 edges individually, and then averages.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 14 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	4.0 ps PP at 10^{-6}

Test Definition Notes from the Specification

- See and Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting toggle pattern.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
4 Measures the pulse width jitter by using Infiniium.
5 Reports the uncorrelated total pulse width jitter value.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 15 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	1.250 ps PP

Test Definition Notes from the Specification

- See Section 8.3.5.8 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Acquires scope sample waveform data (re-iterate to capture at least 4.5M UI).
3 Performs scope random noise removal using the random noise values obtained from scope noise calibration.
4 Measures the pulse width jitter by using Infiniium.
5 Reports the peak deterministic DjDD uncorrelated PWJ value.
6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 4.5M consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 4.5M UI clock recovery window.

'p' indicates the p^{th} 4.5M UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 4.5M UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 16 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.246875 ps	31.253125 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting high swing toggle pattern and low swing toggle pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Transmits high swing toggle pattern.
3 Fits and displays all sample data on screen.
4 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
5 Indicates the upper and lower limit of the measured data using markers.
6 Measures the minimum, mean and maximum values of the UI.
7 Repeats step 1 to step 5 by transmitting low swing toggle pattern.

8 Reports mean UI by averaging the values of high swing toggle mean UI and low swing toggle mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

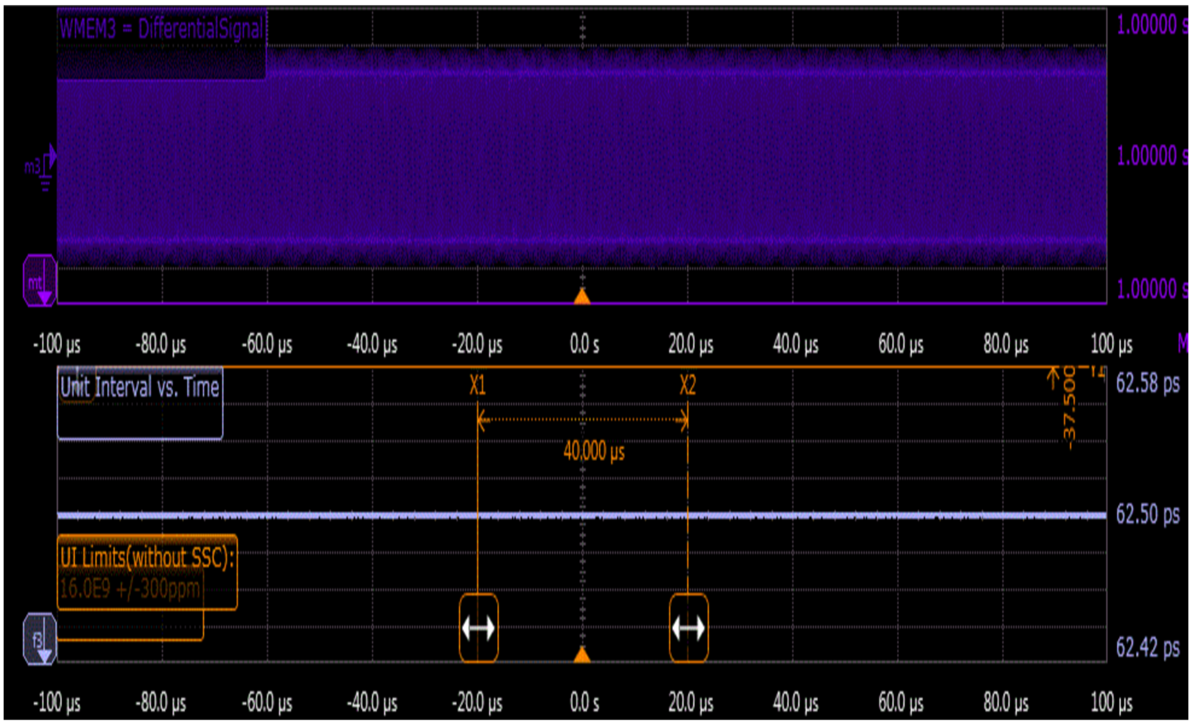


Figure 10 Reference Image for Unit Interval Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 17 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the high swing toggle pattern signal.
2 Verifies that the data rate is 64.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.
9 Repeat step 1 to 8 by using low swing toggle pattern signal.
10 Reports the average of high swing toggle pattern frequency value and low swing toggle pattern frequency value.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 18 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_64G\_SRIS}$	SSC deviation for devices that support 64.0 GT/s and SRIS when operating in SRIS mode at all speeds	0.010%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the high swing toggle pattern signal.
2. Verifies that the data rate is 64.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10. Repeat step 1 to 9 by using low swing toggle pattern signal.
11. Reports the average of high swing toggle pattern SSC deviation Max(%) value and low swing toggle pattern SSC deviation Max(%) value.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 19 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_64G\_SRIS}$	SSC deviation for devices that support 64.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.31%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the high swing toggle pattern signal.
2. Verifies that the data rate is 64.0 GT/s.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures memory depth and sampling rate as per the data rate.
6. Fits and displays all sample data on the screen.
7. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8. Measures Period_max, Period_min and Period_average.
9. Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10. Repeat step 1 to 9 by using low swing toggle pattern signal.
11. Reports the average of high swing toggle pattern SSC deviation Min(%) value and low swing toggle pattern SSC deviation Min(%) value.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 6.0, Section 8.6.3, Table 8-18 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 20 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}FREQ\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µS

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures memory depth and sampling rate as per the data rate..
3. Fits and displays all sample data on screen.
4. Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:
   - *a* Generates a differential plot (x_n - x_{n-1}).
   - *b* The maximum slew rate corresponds to the peak of the differential plot.
7. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

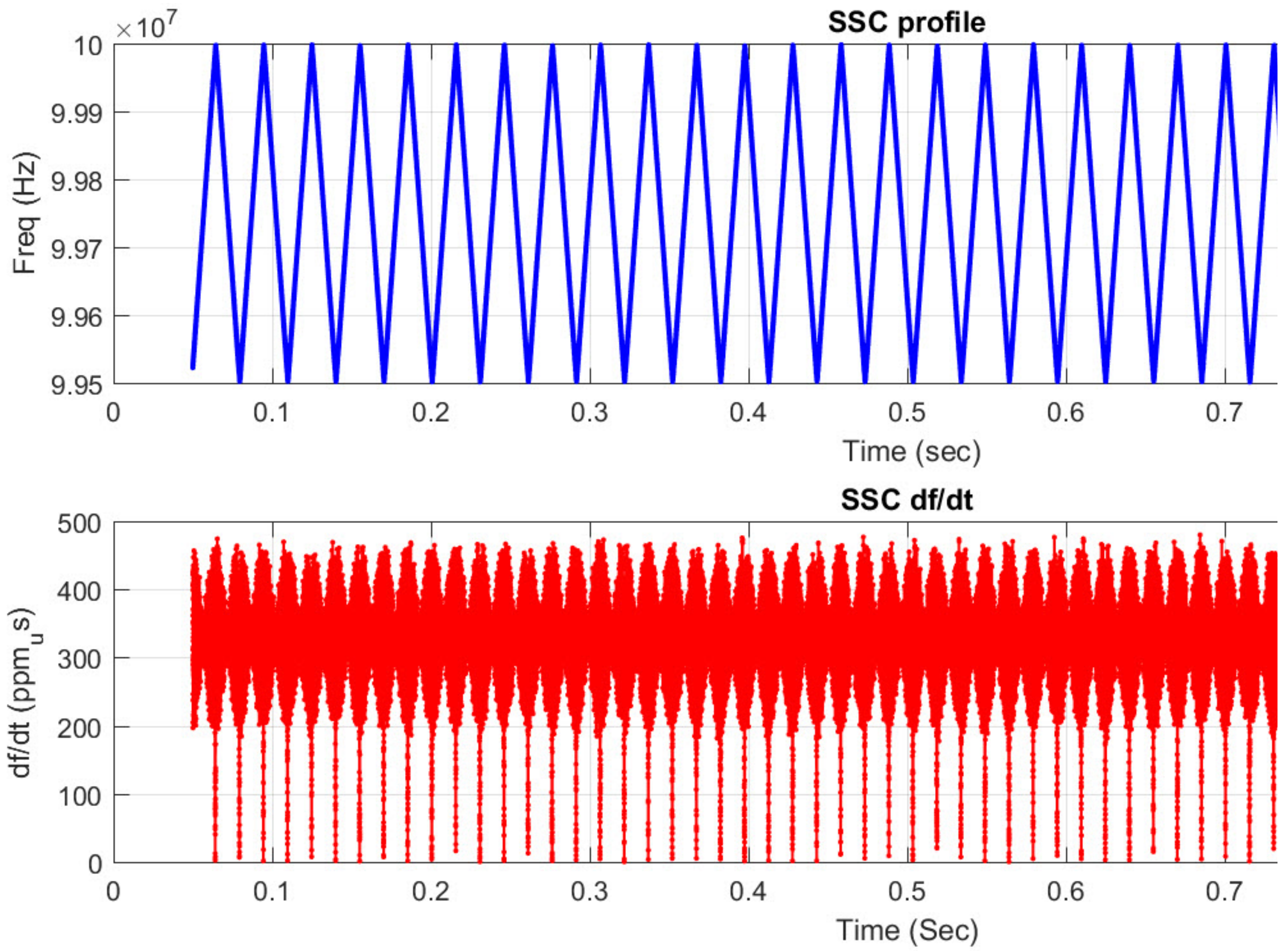


Figure 11 Maximum SSC Slew Rate

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX-DC-CM} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-DC-}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 21 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX-DC-CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage as follows:
   - *a* Enables and displays common mode measurements.
   - *b* Loads common mode signal to waveform memory.
   - *c* Loads and enhance dynamic range D+ signal and D- signal.
   - *d* Enables the average common mode measurement.
   - *e* Uses markers to indicate compliance test limit boundaries (0 V to 3.6 V).
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification as $V_{TX-DC-CM}$ is 0 to 3.6 V.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 16 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-AC-CM-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 22 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	75 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 23 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	25.00 mVPP

Test Definition Notes from the Specification

- Tx ACCM noise measurement analysis is done without any deembedding.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 16 GHz) test.

1 Gets compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}[during\ L0]}| \leq 25$ mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 24 **Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details**

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Test Definition Notes from the Specification

$| V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D\text{-}\ [during\ L0]} | \leq 25$mV

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $| V_{TX\text{-}D+\ [during\ L0]} |$

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $| V_{TX\text{-}D\text{-}\ [during\ L0]} |$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **This test requires the DC Common Mode Output Voltage test.**

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX-CM-DC\ [during\ L0]} - V_{TX-CM-Idle-DC\ [during\ electrical\ idle]}| \leq 100$ mV

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$

$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.3.10, Table 8-7 is used as reference to check the compliance of the DUT.

Table 25 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Test Definition Notes from the Specification

$|V_{TX-CM-DC\ [during\ L0]} - V_{TX-CM-Idle-DC\ [during\ electrical\ idle]}| \leq 100$ mV

$V_{TX-CM-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$

$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $|V_{TX-D+} + V_{TX-D-}|/2$ [electrical idle]

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE **This test requires the Average DC Common Mode Output Voltage test.**

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

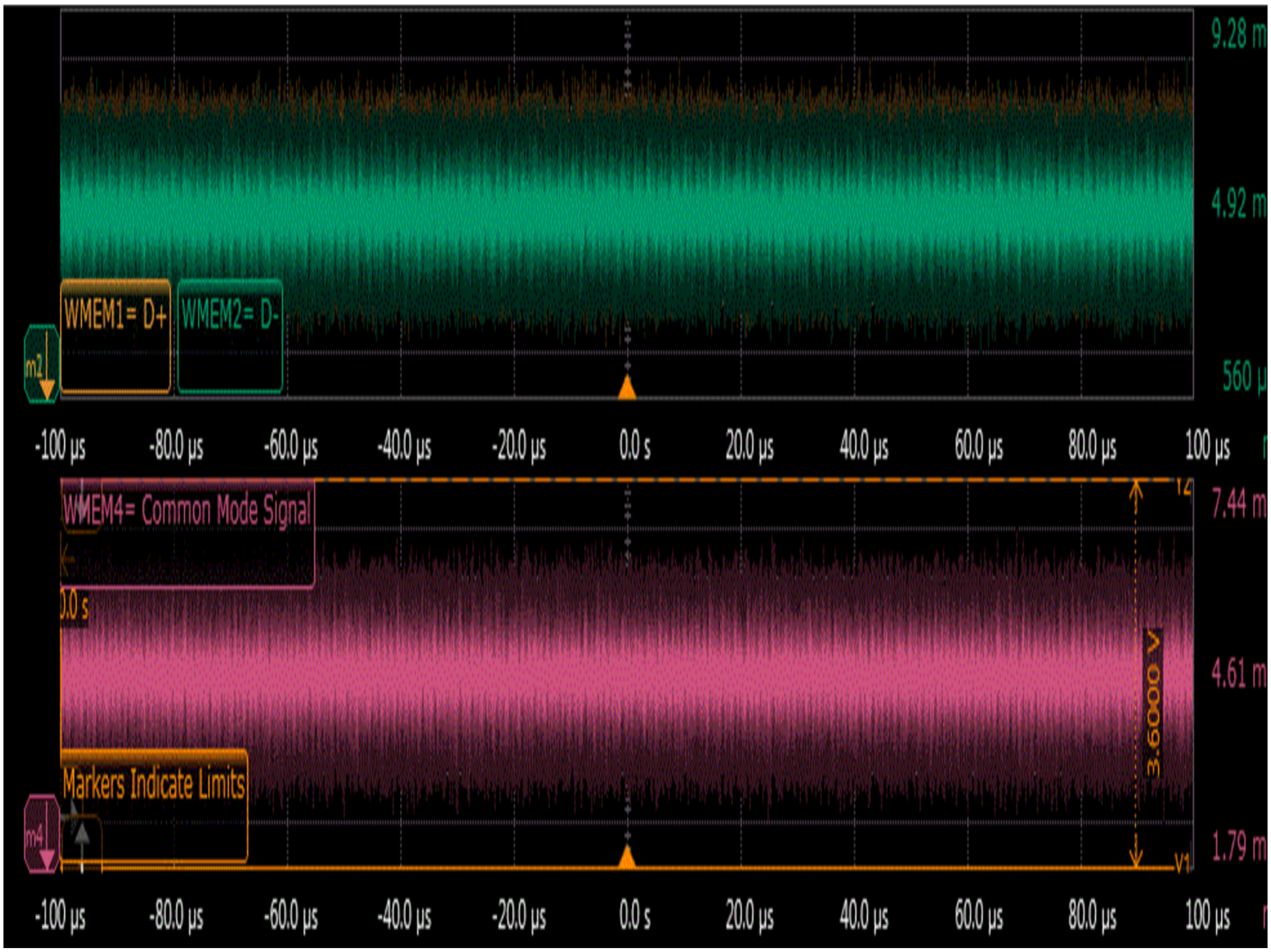


Figure 12 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to "Equalization Presets Tests".

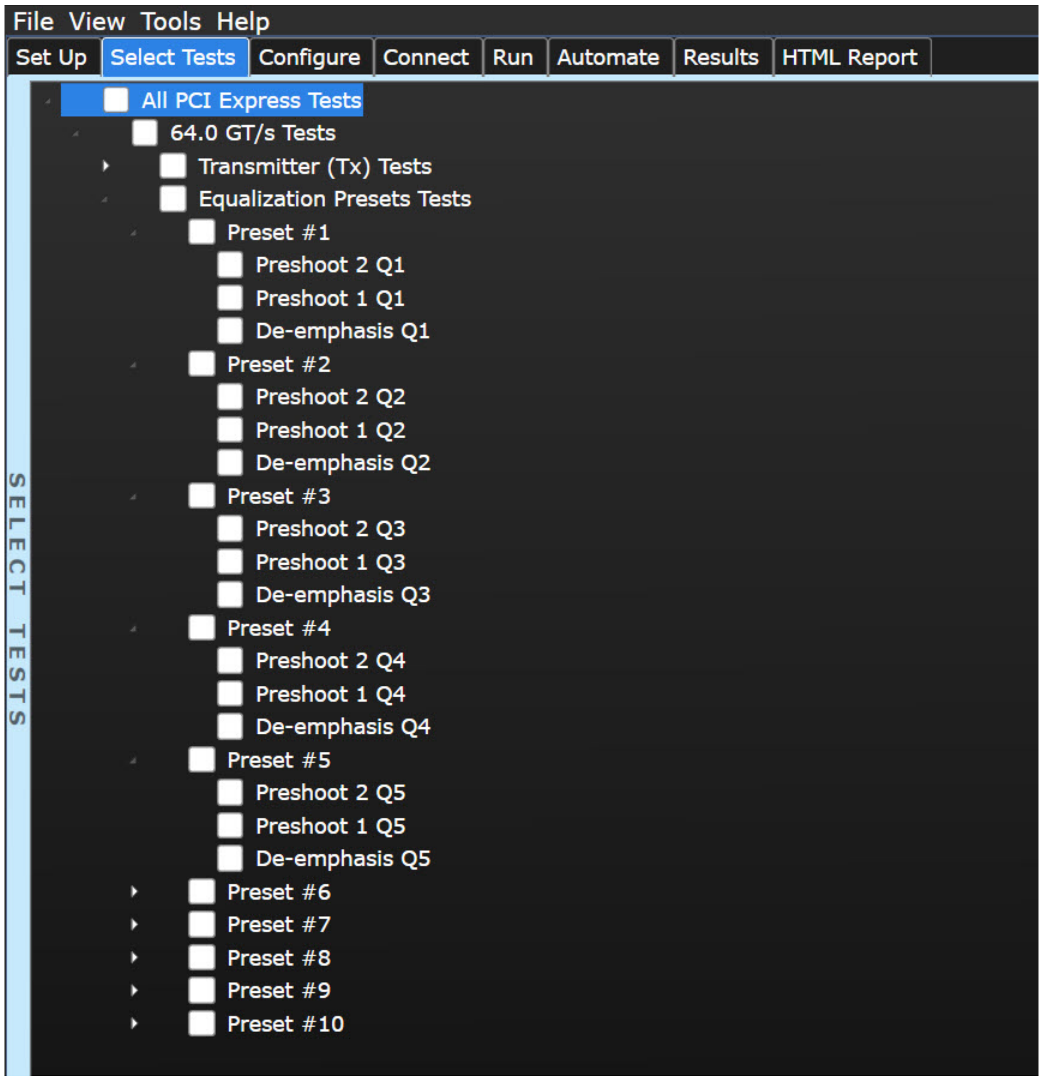


Figure 13 Selecting Equalization Presets Tests

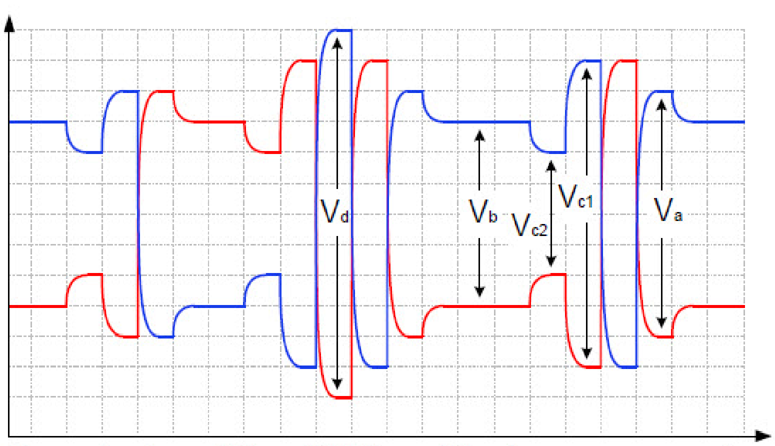
Preset #1 Measurement (Q1), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2 (dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 14.

Table 26 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q1	0.0 ±0.5 dB	1.6 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.083	0.000	0.834	0.834	1.000	0.834



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$
$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$
$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$
$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$
$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 14 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q1.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q1 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q1 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 8-6.
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #1 Measurement (Q1), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 15.

Table 27 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q1	0.0 ±0.5 dB	1.6 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.083	0.000	0.834	0.834	1.000	0.834

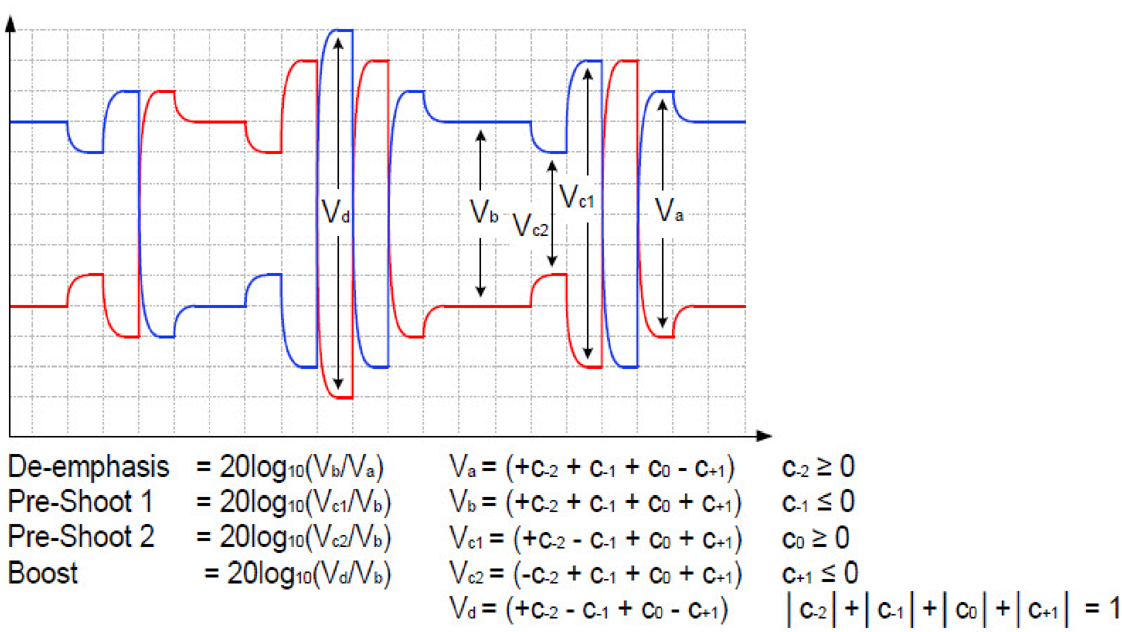


Figure 15 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.

2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #Q0.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.

4 Sets the **Horizontal Domain Scale** to 14.1 µs.

5 Fits and displays all sample data on screen.

6 Saves the Q0 signal into *.bin format.

7 Configures the DUT to operate in preset value #Q1.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.

9 Sets the **Horizontal Domain Scale** to 14.1 µs.

10 Fits and displays all sample data on screen.

11 Saves the Q1 signal in *.bin format.

12 Creates Linear Fit Pulse Response on both Q0 and Q1 by using Infiniium.

13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 15 or Figure 8-6 of the spec.

14 Compares the Preshoot 1 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

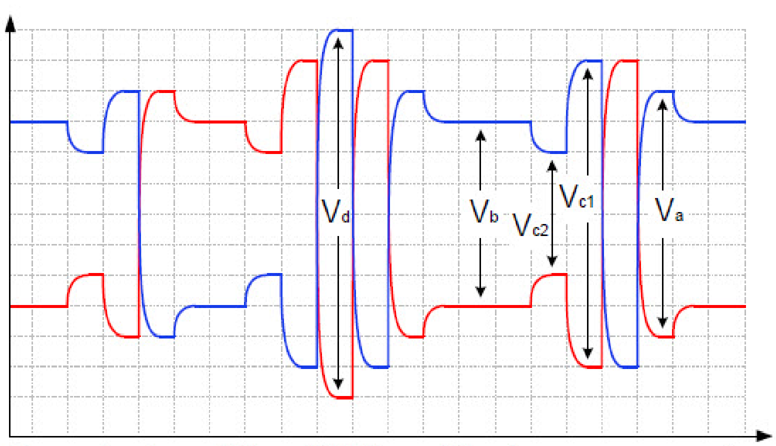
Preset #1 Measurement (Q1), De-emphasis Test

The purpose of this test is to verify that the De-emphasis (dB) of the transmitter Tx at preset number Q1 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 16.

Table 28 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q1	0.0 ±0.5 dB	1.6 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.083	0.000	0.834	0.834	1.000	0.834



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 16 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q1.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q1 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q1 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 16 or Figure 8-6.
14 Compares the De-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (Q2), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 17.

Table 29 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q2	0.0 ±0.5 dB	3.5 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666

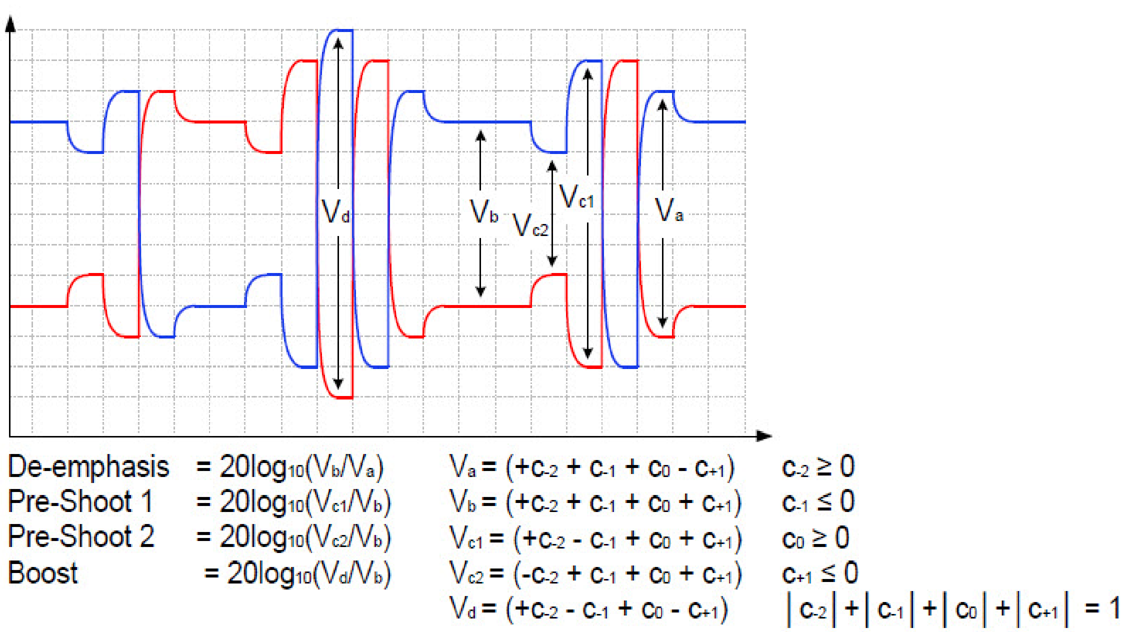


Figure 17 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q2.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q2 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q2 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 17 (Figure 8-6 of the spec).
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

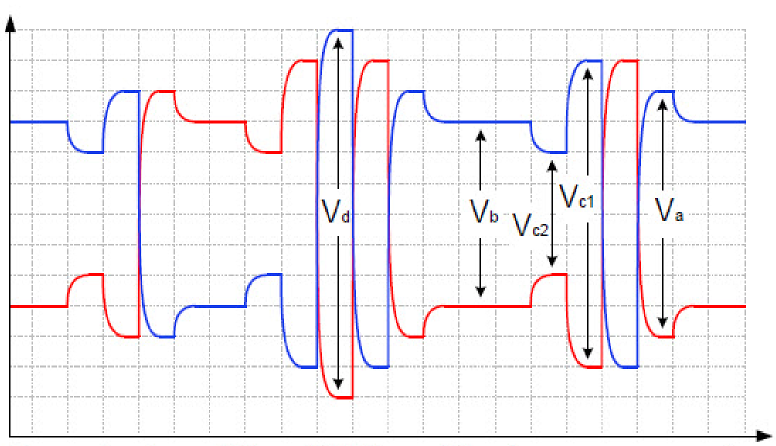
Preset #2 Measurement (Q2), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 18.

Table 30 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q2	0.0 ±0.5 dB	3.5 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 18 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q2.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q2 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q2 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 18 (Figure 8-6 of the spec).
14. Compares the Preshoot 1 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

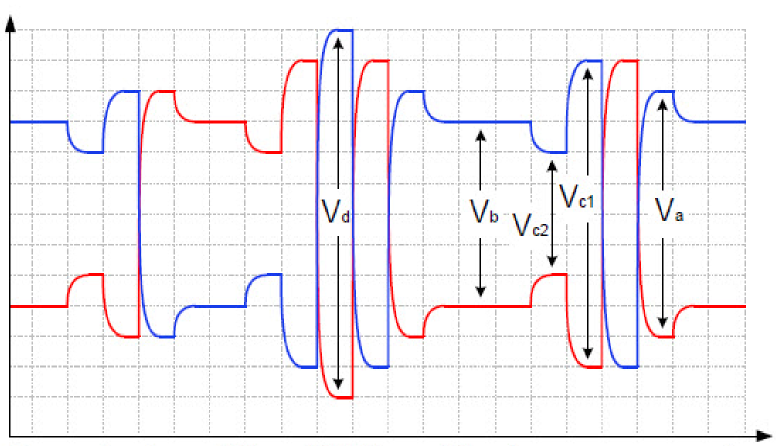
Preset #2 Measurement (Q2), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q2 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 19.

Table 31 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q2	0.0 ±0.5 dB	3.5 ±0.5 dB	0.0 ±0.5 dB	0.000	-0.167	0.000	0.666	0.666	1.000	0.666



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 19 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.

2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #Q0.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.

4 Sets the **Horizontal Domain Scale** to 14.1 µs.

5 Fits and displays all sample data on screen.

6 Saves the Q0 signal into *.bin format.

7 Configures the DUT to operate in preset value #Q2.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.

9 Sets the **Horizontal Domain Scale** to 14.1 µs.

10 Fits and displays all sample data on screen.

11 Saves the Q2 signal in *.bin format.

12 Creates Linear Fit Pulse Response on both Q0 and Q2 by using Infiniium.

13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 19 (Figure 8-6 of the spec).

14 Compares the De-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (Q3), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 20.

Table 32 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q3	0.0 ±0.5 dB	0.0 ±0.5 dB	-1.6 ±0.5 dB	0.000	0.000	0.083	1.000	0.834	0.834	0.834

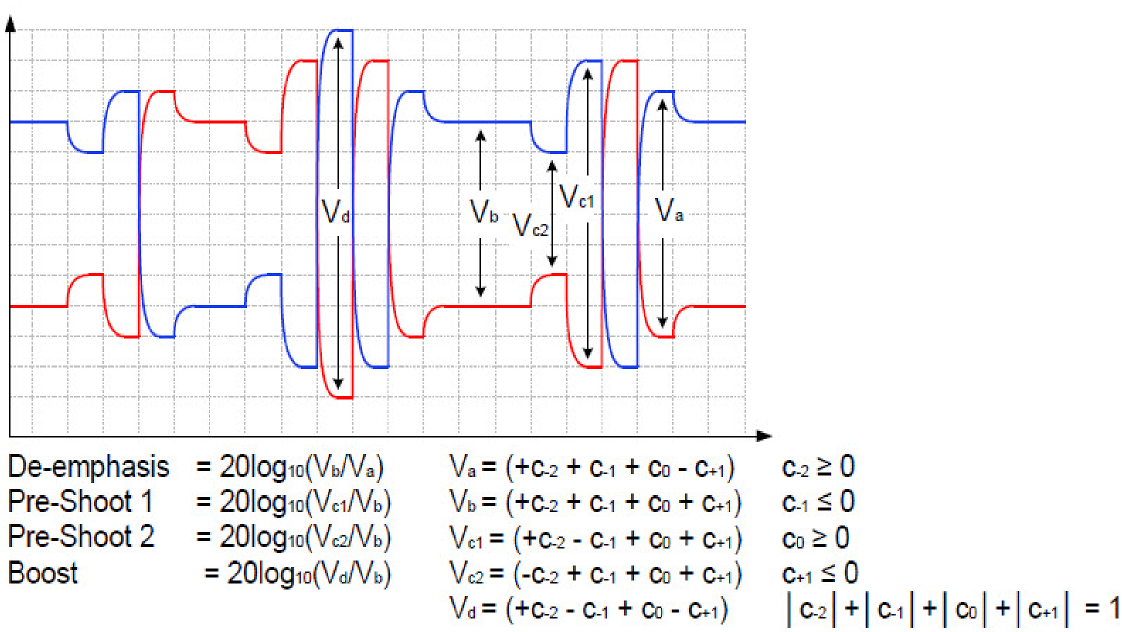


Figure 20 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q3.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q3 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q3 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 20 (Figure 8-6 of the spec).
14. Compares the Preshoot 2 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

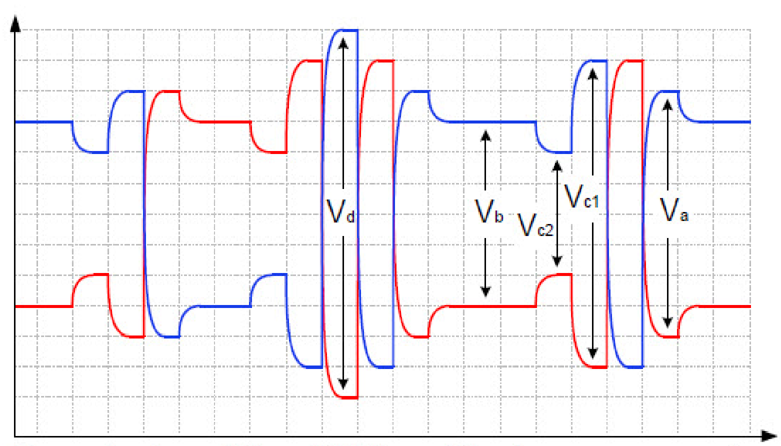
Preset #3 Measurement (Q3), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 21.

Table 33 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q3	0.0 ±0.5 dB	0.0 ±0.5 dB	-1.6 ±0.5 dB	0.000	0.000	0.083	1.000	0.834	0.834	0.834



De-emphasis $= 20\log_{10}(V_b/V_a)$
Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$
Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$
Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$
$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$
$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$
$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$
$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$
$c_{-1} \leq 0$
$c_0 \geq 0$
$c_{+1} \leq 0$
$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 21 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q3 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q3 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 21 (Figure 8-6 of the spec).
14 Compares the Preshoot 1value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

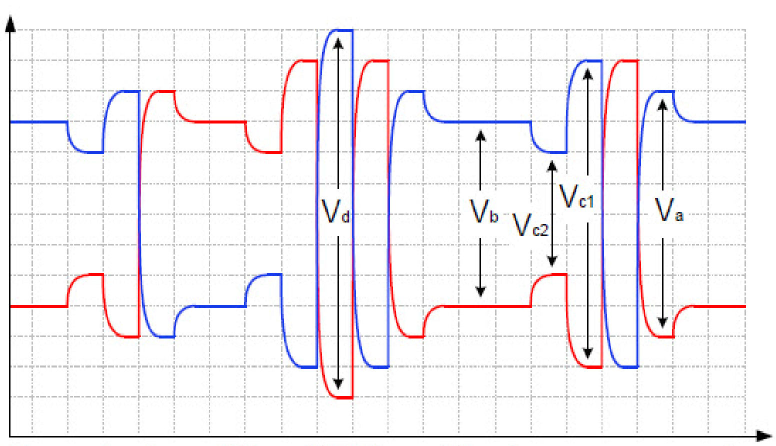
Preset #3 Measurement (Q3), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q3 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 22.

Table 34 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q3	0.0 ±0.5 dB	0.0 ±0.5 dB	-1.6 ±0.5 dB	0.000	0.000	0.083	1.000	0.834	0.834	0.834



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 22 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q3 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q3 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 22 (Figure 8-6 of the spec).
14 Compares the De-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

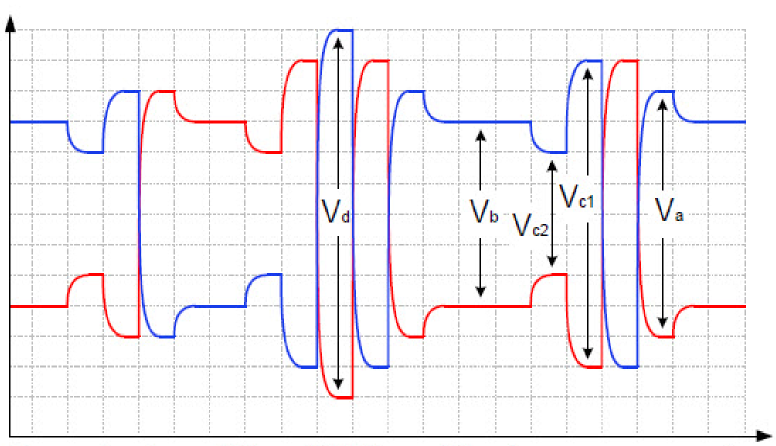
Preset #4 Measurement (Q4), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 23.

Table 35 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q4	0.0 ±0.5 dB	0.0 ±0.5 dB	-3.5 ±0.5 dB	0.000	0.000	-0.167	1.000	0.666	0.666	0.666



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 23 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q4.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q4 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q4 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 23 (Figure 8-6 of the spec).
14 Compares the Pre-shoot 2 value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

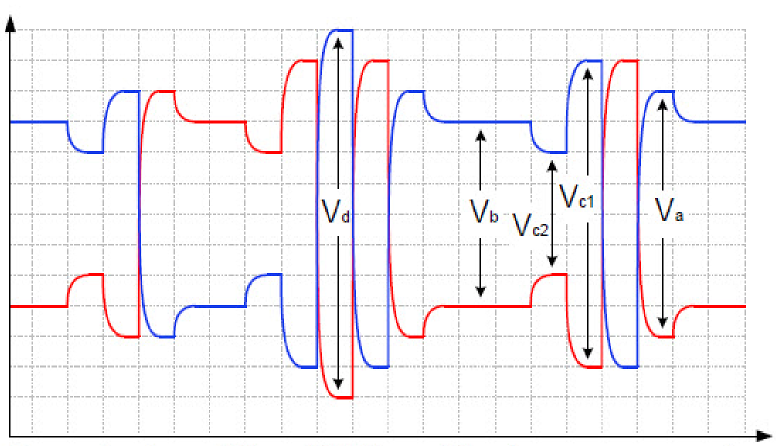
Preset #4 Measurement (Q4), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 24.

Table 36 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q4	0.0 ±0.5 dB	0.0 ±0.5 dB	-3.5 ±0.5 dB	0.000	0.000	-0.167	1.000	0.666	0.666	0.666



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 24 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q4.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q4 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q4 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 24 (Figure 8-6 of the spec).
14 Compares the Pre-shoot 1 value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #4 Measurement (Q4), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q4 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 25.

Table 37 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q4	0.0 ±0.5 dB	0.0 ±0.5 dB	-3.5 ±0.5 dB	0.000	0.000	-0.167	1.000	0.666	0.666	0.666

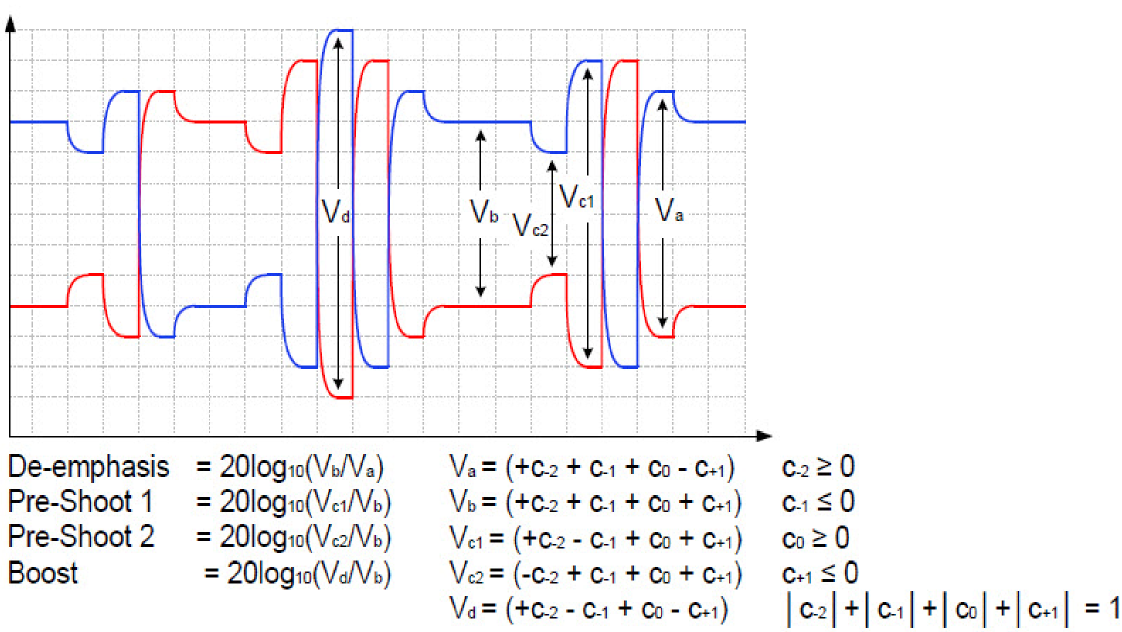


Figure 25 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q4.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q4 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q4 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 25 (Figure 8-6 of the spec).
14. Compares the De-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (Q5), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 26.

Table 38 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q5	-1.3 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.042	-0.208	0.000	0.584	0.584	1.000	0.500

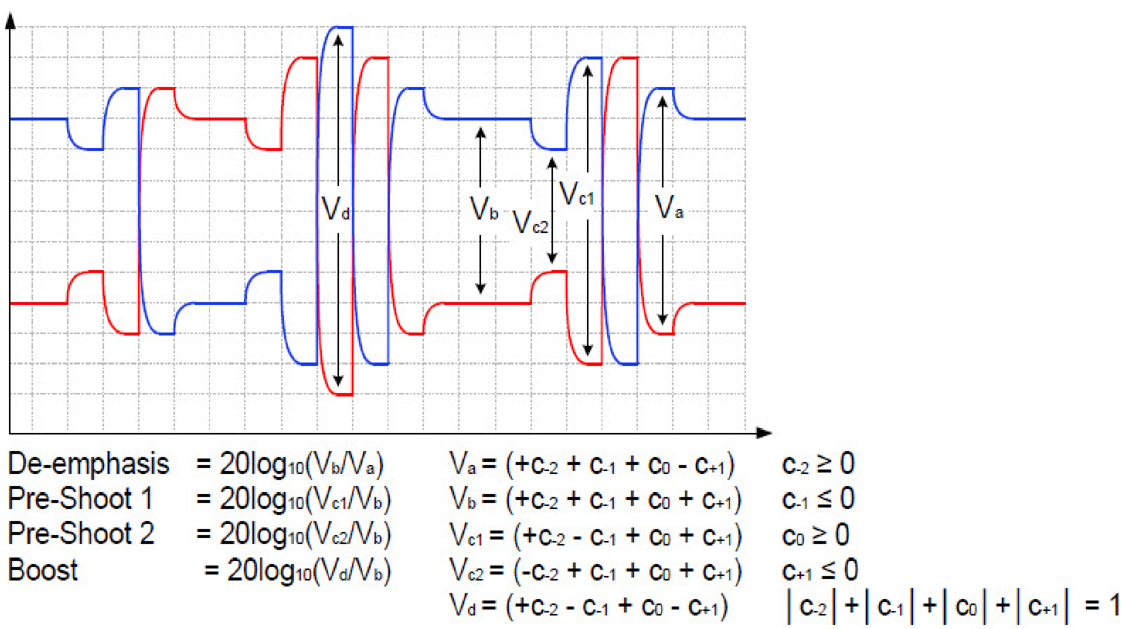


Figure 26 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q5.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q5 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q5 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 26 (Figure 8-6 of the spec).
14. Compares the Preshoot 2 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (Q5), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 27.

Table 39 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q5	-1.3 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.042	-0.208	0.000	0.584	0.584	1.000	0.500

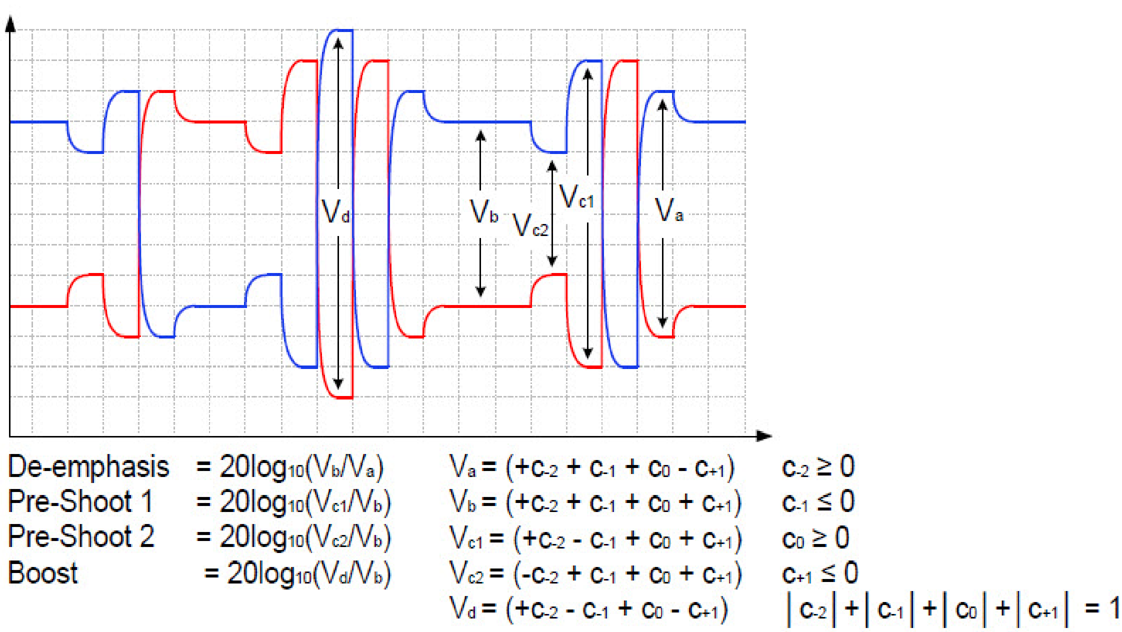


Figure 27 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q5.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q5 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q5 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 27 (Figure 8-6 of the spec).
14 Compares the Preshoot 1 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (Q5), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q5 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 28.

Table 40 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q5	-1.3 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.042	-0.208	0.000	0.584	0.584	1.000	0.500

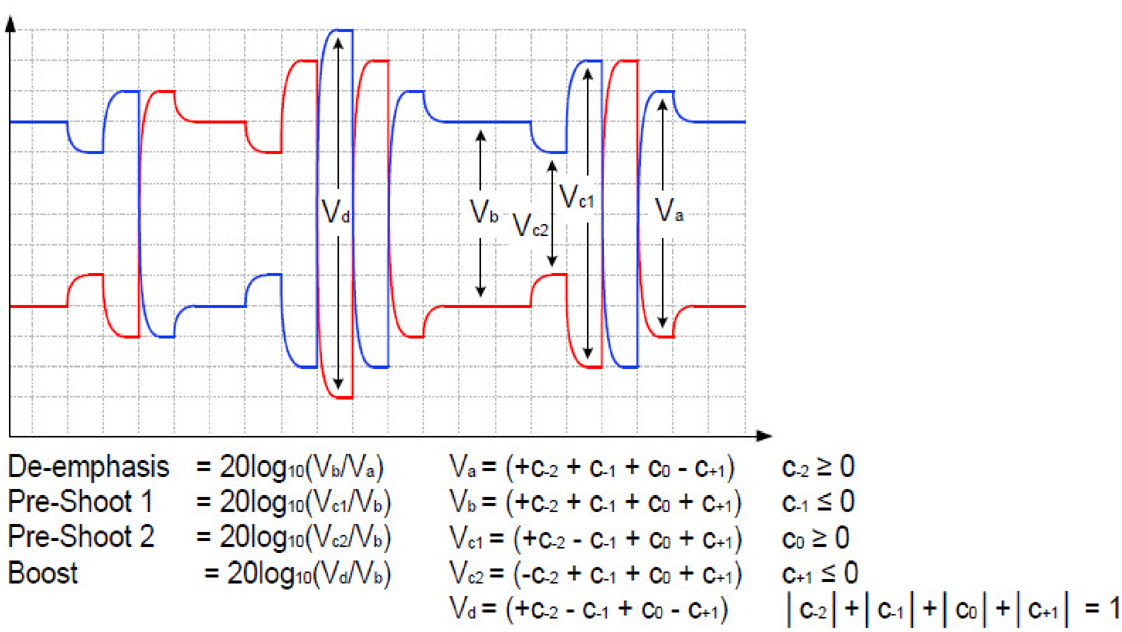


Figure 28 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q5.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q5 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q5 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 28 (Figure 8-6 of the spec).
14 Compares the De-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

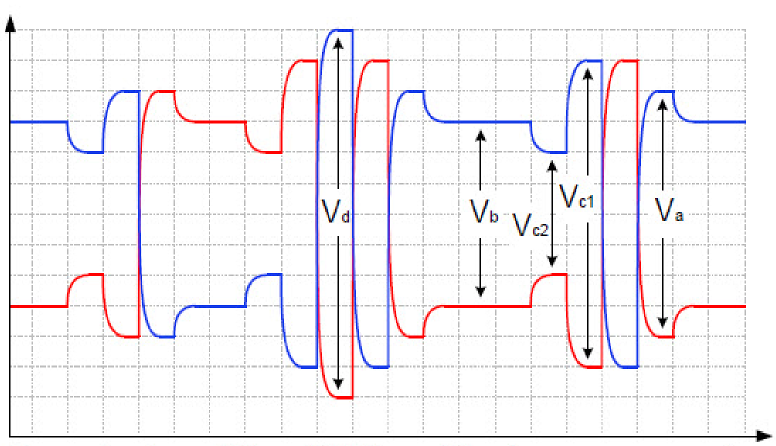
Preset #6 Measurement (Q6), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 29.

Table 41 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q6	-1.6 ±0.5 dB	3.5 ±0.5 dB	-3.5 ±0.5 dB	0.042	-0.125	-0.125	0.750	0.500	0.750	0.416



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 29 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q6.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q6 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q6 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 29 (Figure 8-6 of the spec).
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (Q6), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 30.

Table 42 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q6	-1.6 ±0.5 dB	3.5 ±0.5 dB	-3.5 ±0.5 dB	0.042	-0.125	-0.125	0.750	0.500	0.750	0.416

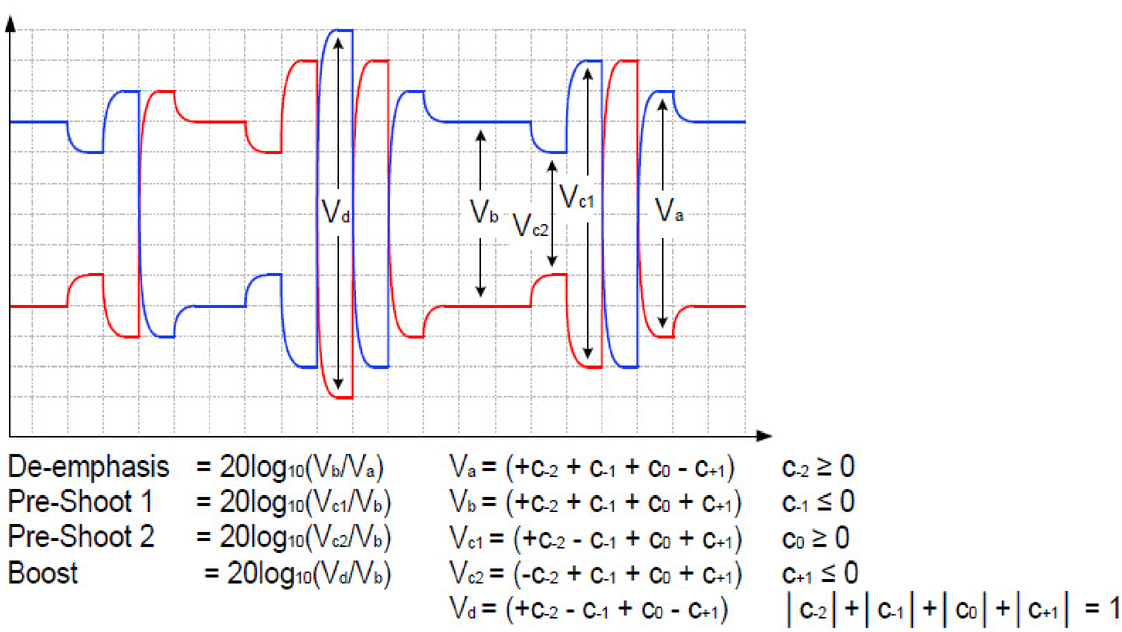


Figure 30 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q6.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q6 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q6 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 30 (Figure 8-6 of the spec).
14 Compares the Preshoot 1 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

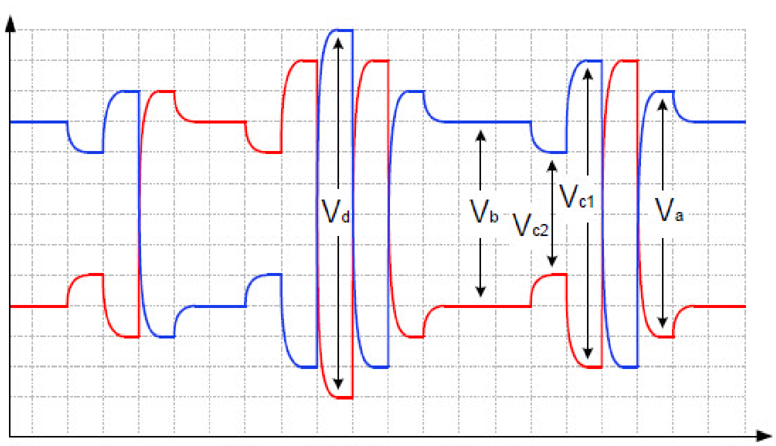
Preset #6 Measurement (Q6), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q6 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 31.

Table 43 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q6	-1.6 ±0.5 dB	3.5 ±0.5 dB	-3.5 ±0.5 dB	0.042	-0.125	-0.125	0.750	0.500	0.750	0.416



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 31 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q6.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q6 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q6 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 31 (Figure 8-6 of the spec).
14 Compares the De-emphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

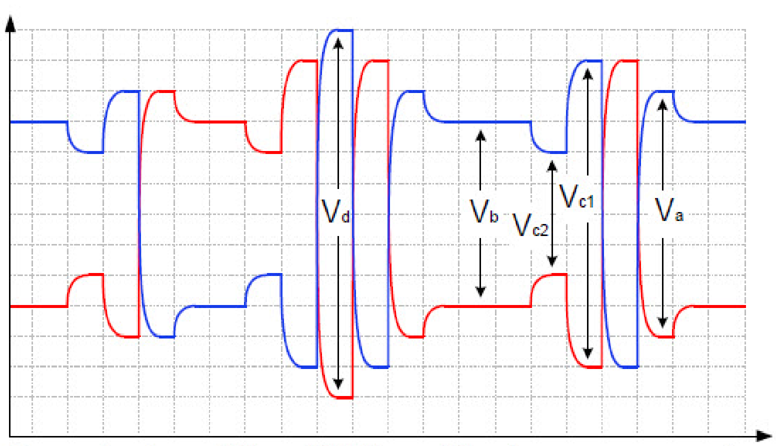
Preset #7 Measurement (Q7), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 32.

Table 44 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q7	-2.9 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.208	0.000	0.584	0.584	1.000	0.418



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 32 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q7 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q7 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 32 (Figure 8-6 of the spec).
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

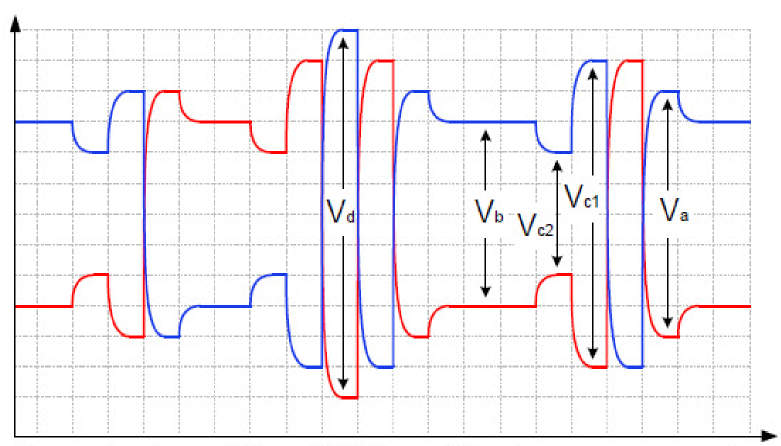
Preset #7 Measurement (Q7), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 33.

Table 45 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q7	-2.9 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.208	0.000	0.584	0.584	1.000	0.418



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a)$$
$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b)$$
$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b)$$
$$\text{Boost} = 20\log_{10}(V_d/V_b)$$

$$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$$
$$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$$
$$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$$
$$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$$
$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$$

$$c_{-2} \geq 0$$
$$c_{-1} \leq 0$$
$$c_0 \geq 0$$
$$c_{+1} \leq 0$$
$$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 33 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q7 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q7 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 33 (Figure 8-6 of the spec).
14 Compares the Preshoot 1 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

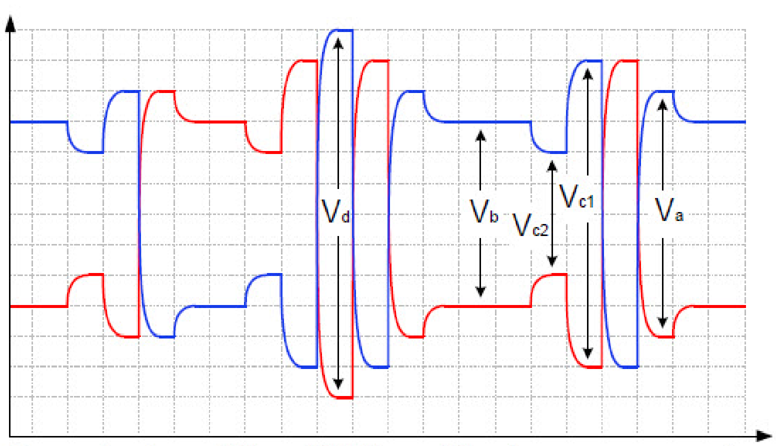
Preset #7 Measurement (Q7), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q7 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 34.

Table 46 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q7	-2.9 ±0.5 dB	4.7 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.208	0.000	0.584	0.584	1.000	0.418



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a) \qquad V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1}) \qquad c_{-2} \geq 0$$

$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b) \qquad V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{-1} \leq 0$$

$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b) \qquad V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1}) \qquad c_0 \geq 0$$

$$\text{Boost} = 20\log_{10}(V_d/V_b) \qquad V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1}) \qquad c_{+1} \leq 0$$

$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1}) \qquad |c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 34 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q7 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q7 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 34 (Figure 8-6 of the spec).
14 Compares the Deemphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (Q8), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 35.

Table 47 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q8	-3.5 ±0.5 dB	6.0 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.250	0.000	0.500	0.500	1.000	0.334

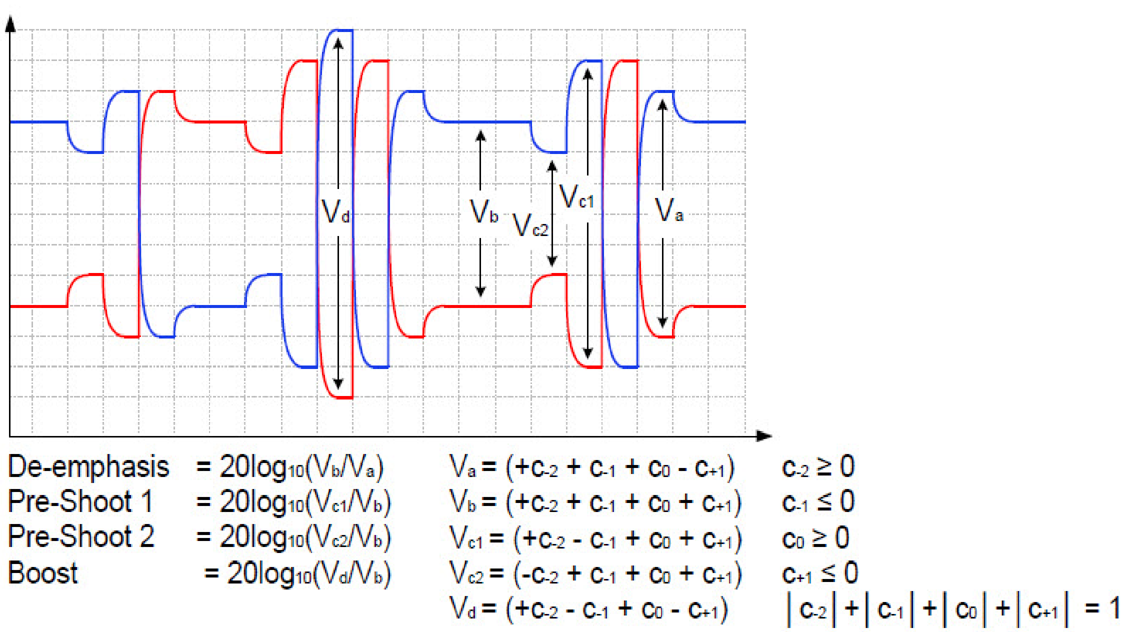


Figure 35 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q8.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q8 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q8 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 35 (Figure 8-6 of the spec).
14. Compares the Preshoot 2 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

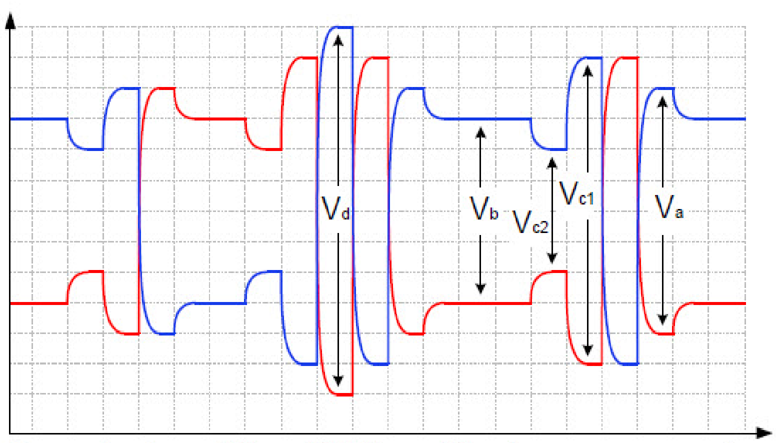
Preset #8 Measurement (Q8), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 36.

Table 48 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q8	-3.5 ±0.5 dB	6.0 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.250	0.000	0.500	0.500	1.000	0.334



$$\text{De-emphasis} = 20\log_{10}(V_b/V_a)$$
$$\text{Pre-Shoot 1} = 20\log_{10}(V_{c1}/V_b)$$
$$\text{Pre-Shoot 2} = 20\log_{10}(V_{c2}/V_b)$$
$$\text{Boost} = 20\log_{10}(V_d/V_b)$$

$$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$$
$$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$$
$$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$$
$$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$$
$$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$$

$$c_{-2} \geq 0$$
$$c_{-1} \leq 0$$
$$c_0 \geq 0$$
$$c_{+1} \leq 0$$
$$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$$

Figure 36 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q8 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q8 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 36 (Figure 8-6 of the spec).
14 Compares the Preshoot 1 value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

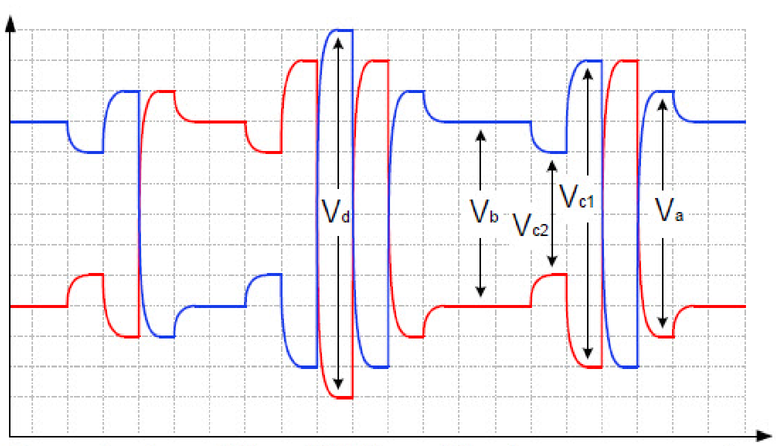
Preset #8 Measurement (Q8), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q8 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 37.

Table 49 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q8	-3.5 ±0.5 dB	6.0 ±1.0 dB	0.0 ±0.5 dB	0.083	-0.250	0.000	0.500	0.500	1.000	0.334



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 37 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q8 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q8 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 37 (Figure 8-6 of the spec).
14 Compares the Deemphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

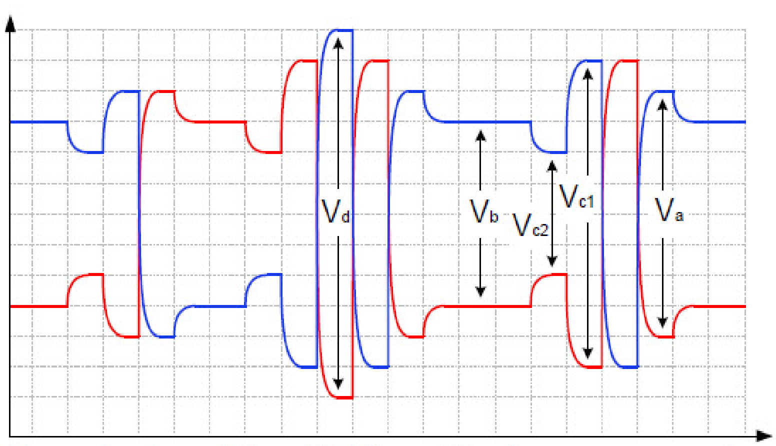
Preset #9 Measurement (Q9), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 38.

Table 50 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q9	-4.4 ±1.0 dB	6.9 ±1.0 dB	-1.6 ±0.5 dB	0.083	-0.250	-0.042	0.500	0.416	0.916	0.250



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 38 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q9.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q9 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q9 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 38 (Figure 8-6 of the spec).
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

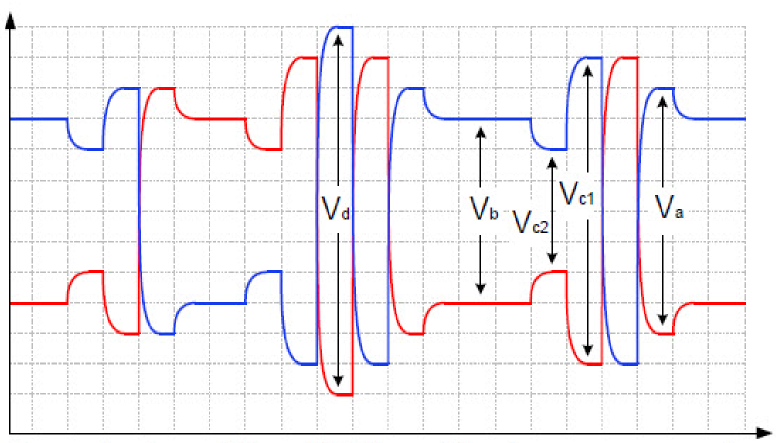
Preset #9 Measurement (Q9), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 39.

Table 51 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q9	-4.4 ±1.0 dB	6.9 ±1.0 dB	-1.6 ±0.5 dB	0.083	-0.250	-0.042	0.500	0.416	0.916	0.250



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 39 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q9.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q9 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q9 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 39 (Figure 8-6 of the spec).
14. Compares the Preshoot 1 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (Q9), De-emphasis Test

The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q9 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 40.

Table 52 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q9	-4.4 ±1.0 dB	6.9 ±1.0 dB	-1.6 ±0.5 dB	0.083	-0.250	-0.042	0.500	0.416	0.916	0.250

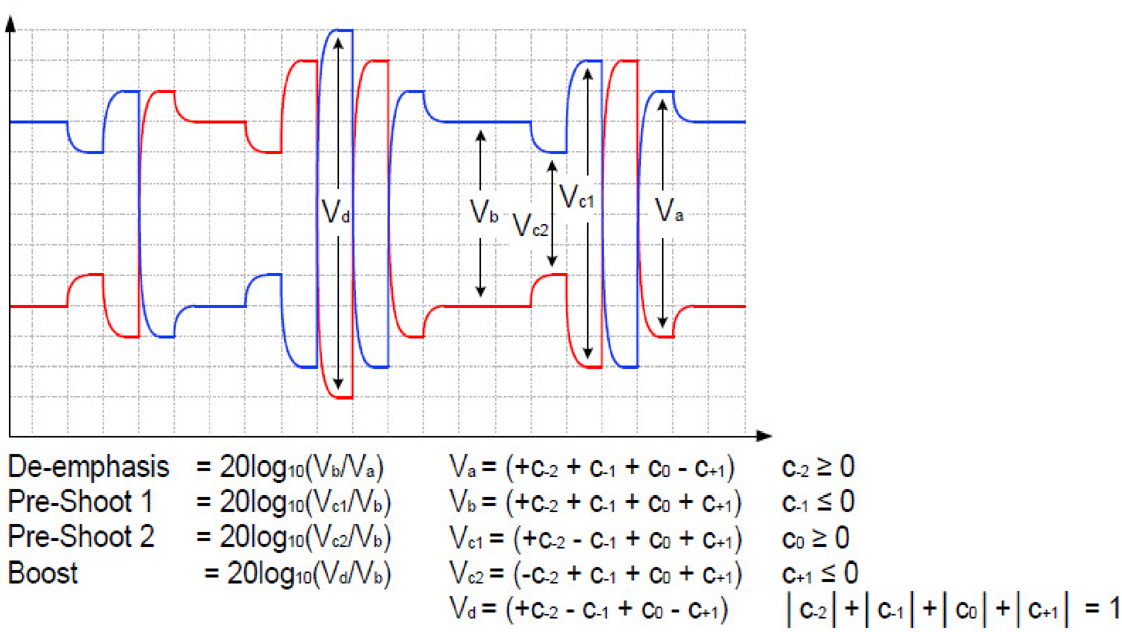


Figure 40 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1. Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2. Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures the DUT to operate in preset value #Q0.
3. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4. Sets the **Horizontal Domain Scale** to 14.1 µs.
5. Fits and displays all sample data on screen.
6. Saves the Q0 signal into *.bin format.
7. Configures the DUT to operate in preset value #Q9.
8. Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9. Sets the **Horizontal Domain Scale** to 14.1 µs.
10. Fits and displays all sample data on screen.
11. Saves the Q9 signal in *.bin format.
12. Creates Linear Fit Pulse Response on both Q0 and Q9 by using Infiniium.
13. Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 40 (Figure 8-6 of the spec).
14. Compares the Demphasis value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (Q10), Preshoot 2 Test

The purpose of this test is to verify that the Preshoot 2(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 41.

Table 53 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q10	0.0 ±0.5 dB	0.0 ±0.5 dB	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2

Note2: Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

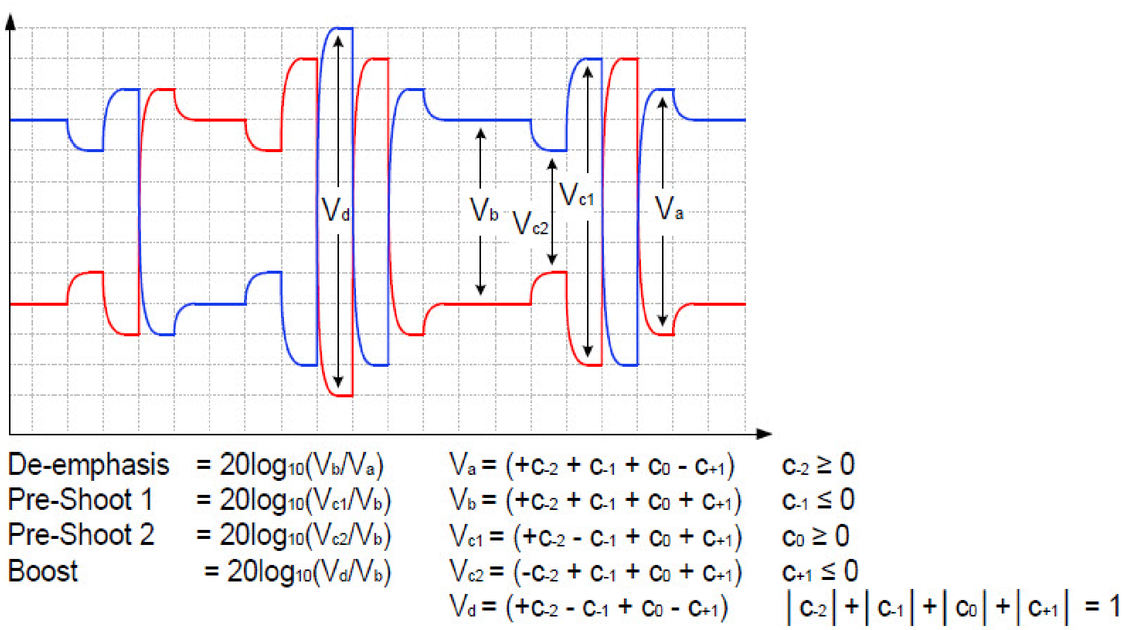


Figure 41 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q10 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q10 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 41 (Figure 8-6 of the spec).
14 Compares the Preshoot 2 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

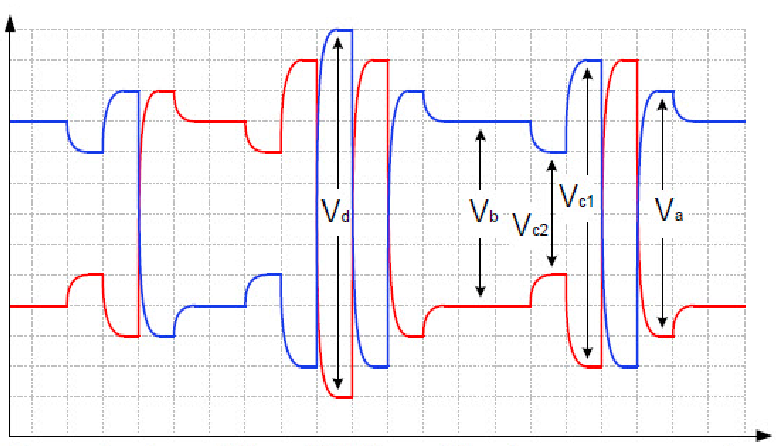
Preset #10 Measurement (Q10), Preshoot 1 Test

The purpose of this test is to verify that the Preshoot 1(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 42.

Table 54 Tx Preset Ratios and Corresponding Coefficient Values

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q10	0.0 ±0.5 dB	0.0 ±0.5 dB	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2
Note2: Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.										



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 42 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE **Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q10 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q10 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 42 (Figure 8-6 of the spec).
14 Compares the Preshoot 1 value to the compliance test limits.

NOTE **Base - Transmitter Tests:**
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (Q10), De-emphasis Test

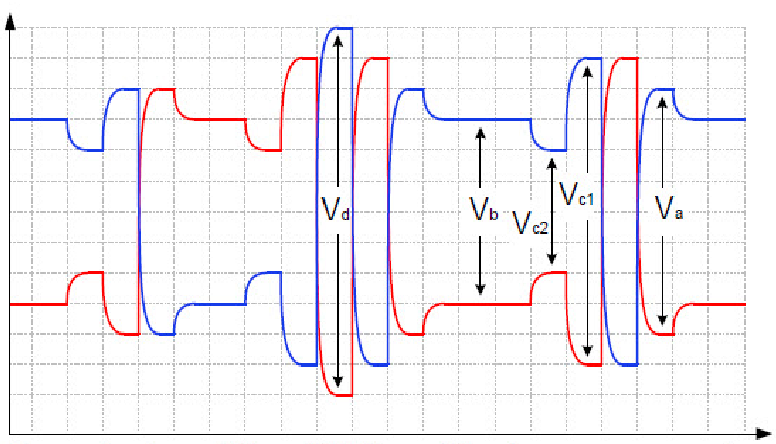
The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number Q10 is within the conformance limits specified in the PCI Express Base Specification.

64.0 GT/s PCIe signaling must support the full range of presets given in Table 8-2 (PCIE Base Specification Revision 6.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 6.0) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 43.

Table 55 **Tx Preset Ratios and Corresponding Coefficient Values**

Preset	Preshoot 2 (dB)	Preshoot 1(dB)	De-emphasis (dB)	c_{-2}	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc1/Vd	Vc2/Vd
Q10	0.0 ±0.5 dB	0.0 ±0.5 dB	Note 2	0.000	0.000	Note 2	1.000	Note 2	Note 2	Note 2

Note2: Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.



De-emphasis $= 20\log_{10}(V_b/V_a)$

Pre-Shoot 1 $= 20\log_{10}(V_{c1}/V_b)$

Pre-Shoot 2 $= 20\log_{10}(V_{c2}/V_b)$

Boost $= 20\log_{10}(V_d/V_b)$

$V_a = (+c_{-2} + c_{-1} + c_0 - c_{+1})$

$V_b = (+c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_{c1} = (+c_{-2} - c_{-1} + c_0 + c_{+1})$

$V_{c2} = (-c_{-2} + c_{-1} + c_0 + c_{+1})$

$V_d = (+c_{-2} - c_{-1} + c_0 - c_{+1})$

$c_{-2} \geq 0$

$c_{-1} \leq 0$

$c_0 \geq 0$

$c_{+1} \leq 0$

$|c_{-2}| + |c_{-1}| + |c_0| + |c_{+1}| = 1$

Figure 43 Waveform measurement points for preshoot and de-emphasis

Test Reference

PCIE Base Specification Revision 6.0, Section 8.3.3.3, Table 8-2 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

1 Reduced swing signaling must implement presets Q0, Q1, Q2, Q3, and Q4. Full swing signaling must implement all the above presets.
2 Q10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. Q10 is used for testing the boost limit of Transmitter at full swing. Q4 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.11 of the PCI Express Base Specification, Rev 6.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #Q0.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
4 Sets the **Horizontal Domain Scale** to 14.1 µs.
5 Fits and displays all sample data on screen.
6 Saves the Q0 signal into *.bin format.
7 Configures the DUT to operate in preset value #Q10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used.
9 Sets the **Horizontal Domain Scale** to 14.1 µs.
10 Fits and displays all sample data on screen.
11 Saves the Q10 signal in *.bin format.
12 Creates Linear Fit Pulse Response on both Q0 and Q10 by using Infiniium.
13 Computes their equalization voltages by using Matlab, and then calculates equalization ratios by using the formulae stated in Figure 43 (Figure 8-6 of the spec).
14 Compares the De-emphasis value to the compliance test limits.

NOTE

Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

36 Reference Clock Tests, 64.0 GT/s, PCI-E 6.0

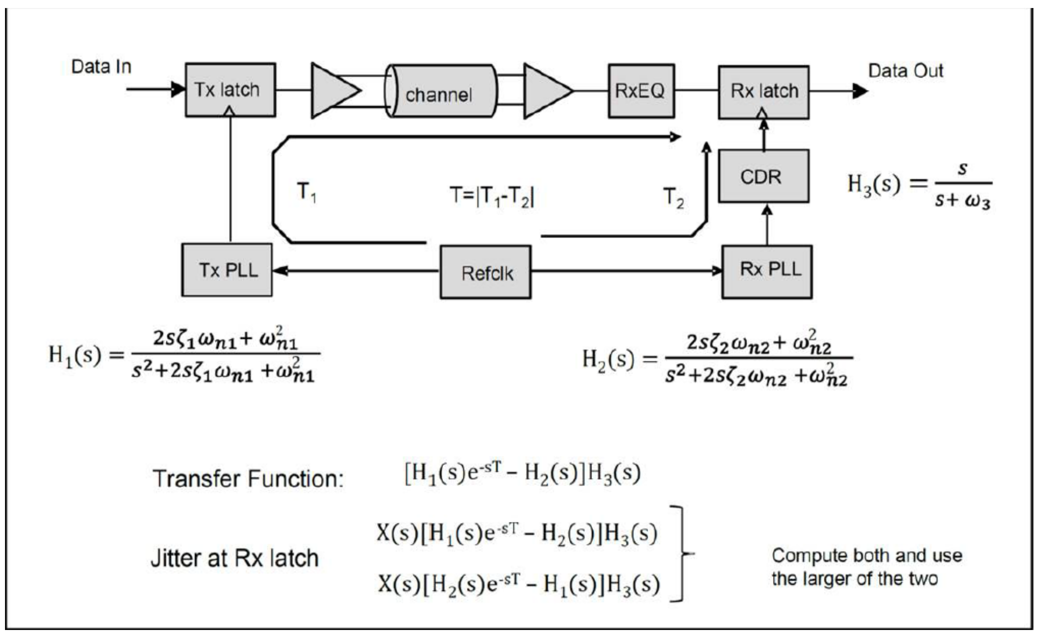
This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 64.0 GT/s using Keysight Z-Series or UXR Series Infiniium oscilloscope and the PCI Express Compliance Test Application.

Reference Clock Architectures

For 64.0 GT/s, PCI-E 6.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

Common Clock Architecture

This architecture utilizes a single Refclk source that is distributed to both the Tx and Rx. Most of the SSC jitter sourced by the Refclk is propagated equally through Tx and Rx PLLs, and so intrinsically tracks LF jitter. This is particularly true for SSC which tends to be low frequency. Figure 8-89 of the base spec illustrates the Common Refclk Rx architecture, showing key jitter, delay, and PLL and CDR transfer function sources for all data rates except 32.0 and 64.0 GT/s. At 32.0 and 64.0 GT/s the only difference in the figure is Behavioral CDR transfer function as defined in Section 8.3.5.5 of the base spec. The amount of jitter appearing at the CDR is then defined by the difference function between the Tx and Rx PLLs multiplied by the CDR high-pass characteristic.



Based on the above clock architecture, it is possible to define a difference function that corresponds to the worst case mismatch between Tx and Rx PLLs. Second order PLL transfer functions are assumed, (even though most PLL transfer functions are 3^{rd} order or higher), since a 2^{nd} order function tends to yield a slightly conservative difference function vis-a-vis most actual PLL implementations. In the Common Refclk Rx architecture it is also necessary to comprehend a maximum Transmitter to Receiver transport delay difference. This delay delta is illustrated in Figure 8-89 of the base spec and represents the delay difference between the Transmitter data and recovered Receiver clock as seen at the inputs to the receiver's data latch.

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
$BW_{PLL}(min)$ = 0.5 MHz	ω_{n1} = 0.112 Mrad/s ζ_1 = 14	ω_{n1} = 1.50 Mrad/s ζ_1 = 0.73
$BW_{PLL}(max)$ = 1.0 MHz	ω_{n1} = 0.224 Mrad/s ζ_1 = 14	ω_{n1} = 3.00 Mrad/s ζ_1 = 0.73

64.0 GT/s CC **CDR**

16 combinations

64.0 GT/s

Figure 8-94 Common Refclk PLL and CDR Characteristics for 64.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 6.0, Section 8.6.1, Figure 8-80.

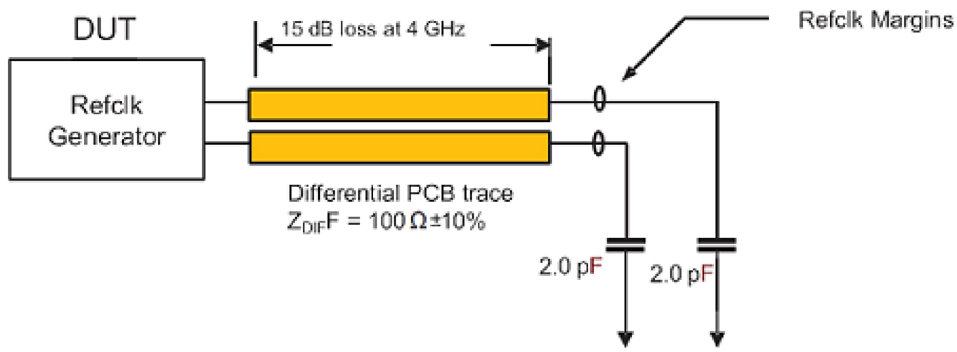


Figure 44 Driver Compliance Test Load

The test setup for the Refclk assumes that only the Refclk generator itself is present. Provision is made in the test setup to account for signal degradation that occurs between the pins of the Refclk generator and the Transmitter or Receiver in an actual system. The above described setup emulates the worst case signal degradation that is likely to occur at the pins of a PCI Express device. Note that the Refclk signal is tested into a load that represents the series (open) termination appearing at the Refclk input pins of a PCIe device for all requirements except 32.0 and 64.0 GT/s reference clock jitter. For 32.0 and 64.0 GT/s, the reference clock jitter is measured with an oscilloscope, and is tested with the reference clock terminated by 50 Ohm terminations without a channel.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Compliance Test Application" on page 39. Then, when selecting tests, navigate to **All PCI Express Tests > 64.0 GT/s Tests > Reference Clock Tests**.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

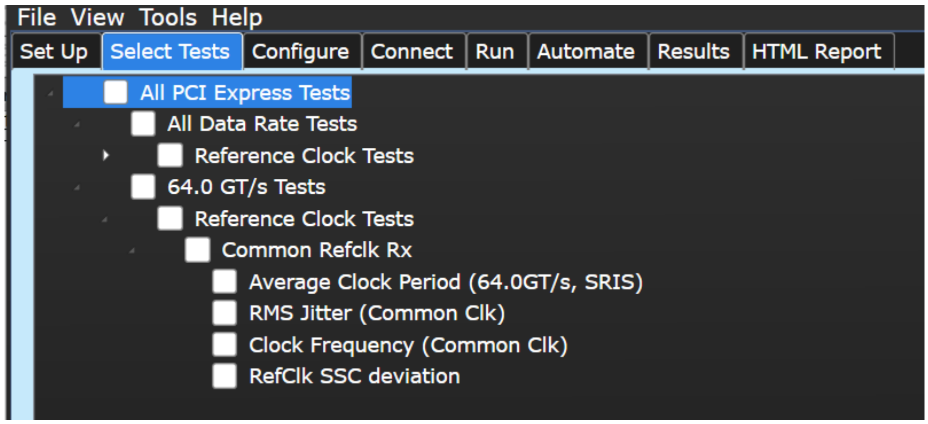


Figure 45 Selecting Reference Clock Tests when SSC is Selected with SRIS mode enabled.

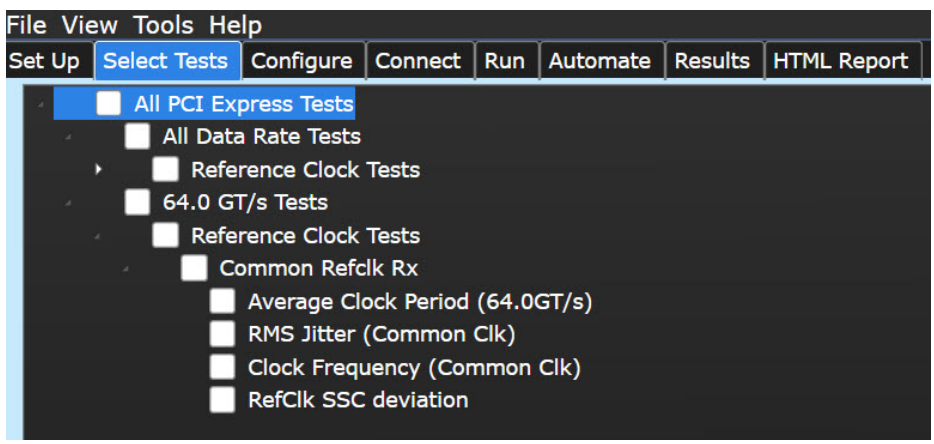


Figure 46 Selecting Reference Clock Tests when SSC is Selected without SRIS mode.

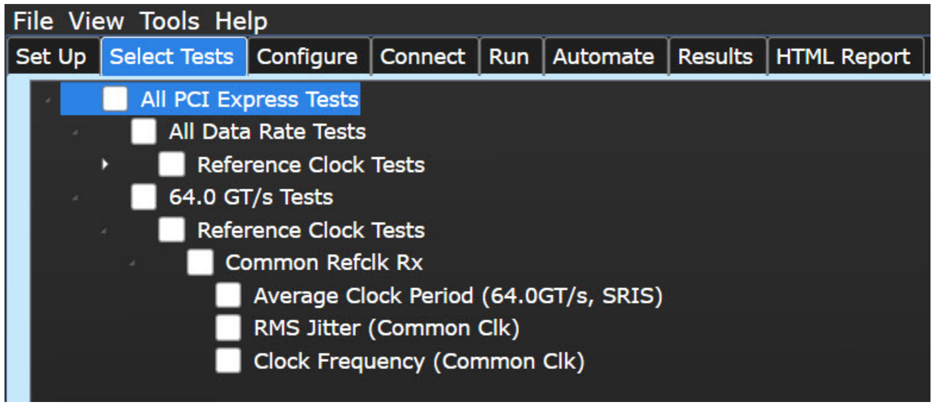


Figure 47 Selecting Reference Clock Tests when Clean Clock is Selected with SRIS mode enabled.

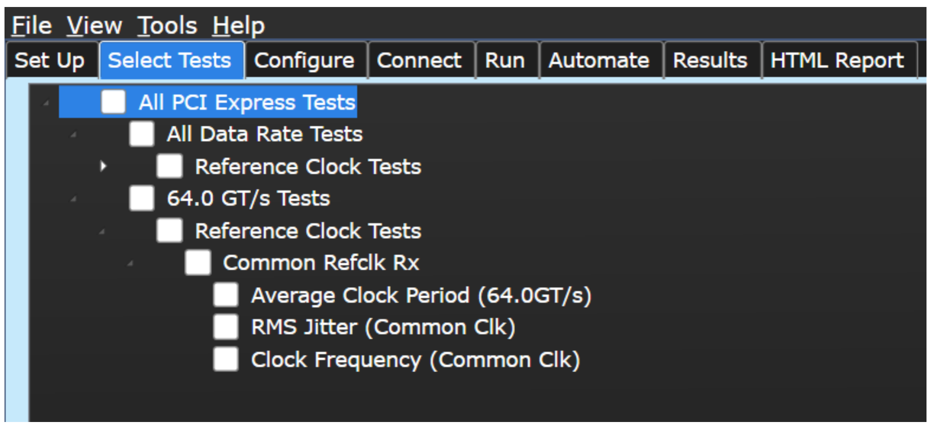


Figure 48 Selecting Reference Clock Tests when Clean Clock is Selected without SRIS mode.

Average Clock Period Test (64.0 GT/s)

This test verifies that the Refclk Average Clock Period (64 GT/s) is within the conformance limits as specified in PCIE Express Base Specification.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC, there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 64.0GT/s speed.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.2, Table 8-17 (REFCLK DC Specifications and AC Timing Requirements) is used as reference to check the compliance of the DUT.

Table 56 Average Clock Period Test Details

		100 MHz Input	
Symbol	**Parameter**	**Min**	**Max**
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	+2800 ppm
$T_{PERIOD\ AVG\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices that support 32.0 GT/s or 64 GT/s in CC Mode at any speed	-100 ppm	+2600 ppm
$T_{PERIOD\ AVG\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices that support 32.0 GT/s or 64 GT/s in SRIS Mode at any speed	-100 ppm	+1600 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform..
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3 Configures memory depth and sampling rate as per the data rate.
4 Fits and displays all sample data on screen.
5 Measures the average voltage using **V average** measurement.
6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
7 Measures the average frequency using **Frequency** measurement of **Clock**.
8 Measures the average period using **Period** measurement of **Clock**.
9 Computes the difference between ideal and actual frequency in terms of parts per million of 100 MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification.

For SSC Mode,

-300 ppm ≤ Average Clock Period Accuracy ≤ +2800 ppm

For Clean Clock,

-100 ppm ≤ Average Clock Period Accuracy ≤ +2600 ppm

For SRIS Mode,

-100 ppm ≤ Average Clock Period Accuracy ≤ +1600 ppm

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

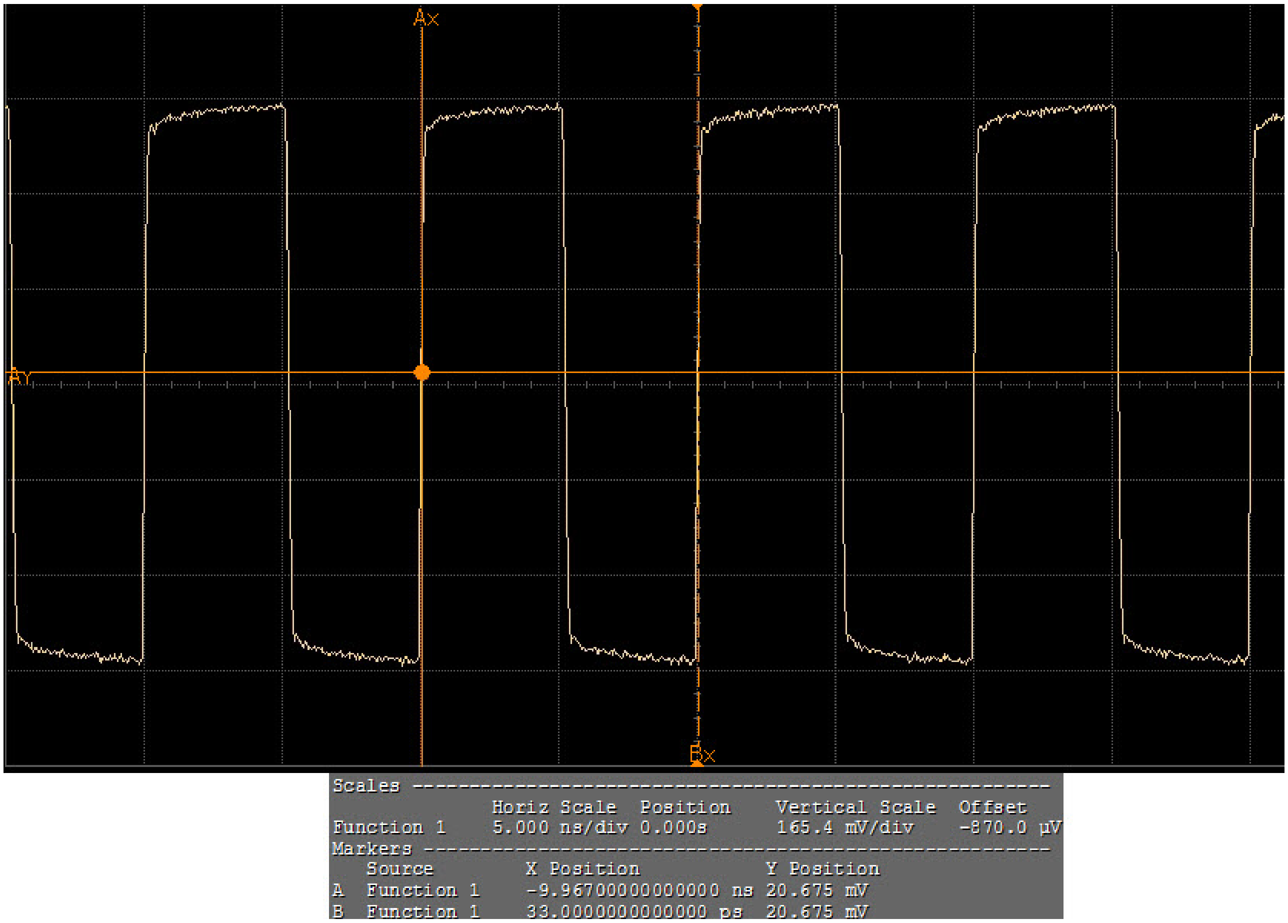


Figure 49 Reference Image for Average Clock Period

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.7, Table 8-19 is used as reference to check the compliance of the DUT.

Table 57 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.1 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-89.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.
- For the 16.0, 32.0, and 64.0 GT/s CC measurements SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
- Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting toggle pattern.

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE

Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

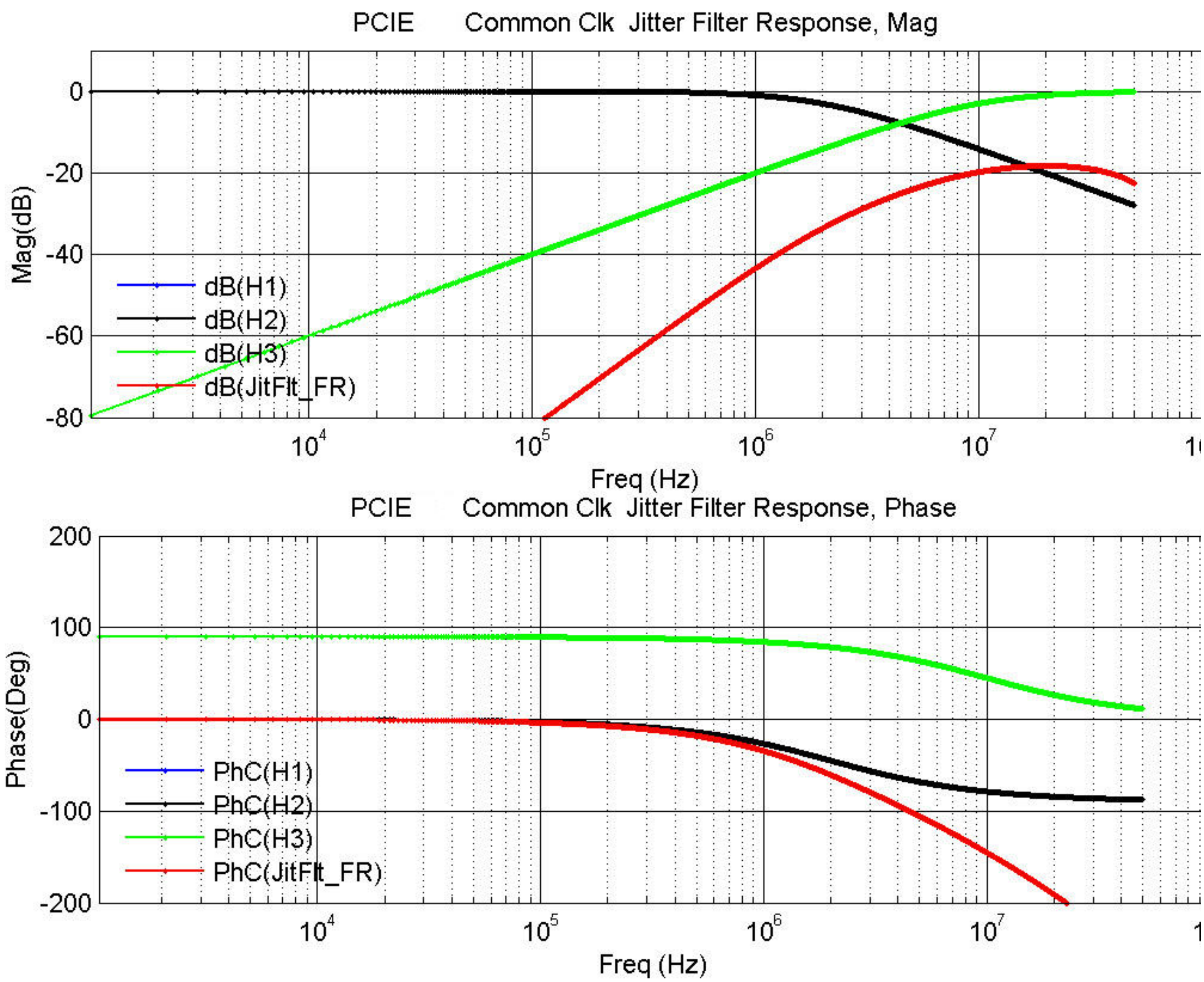


Figure 50 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

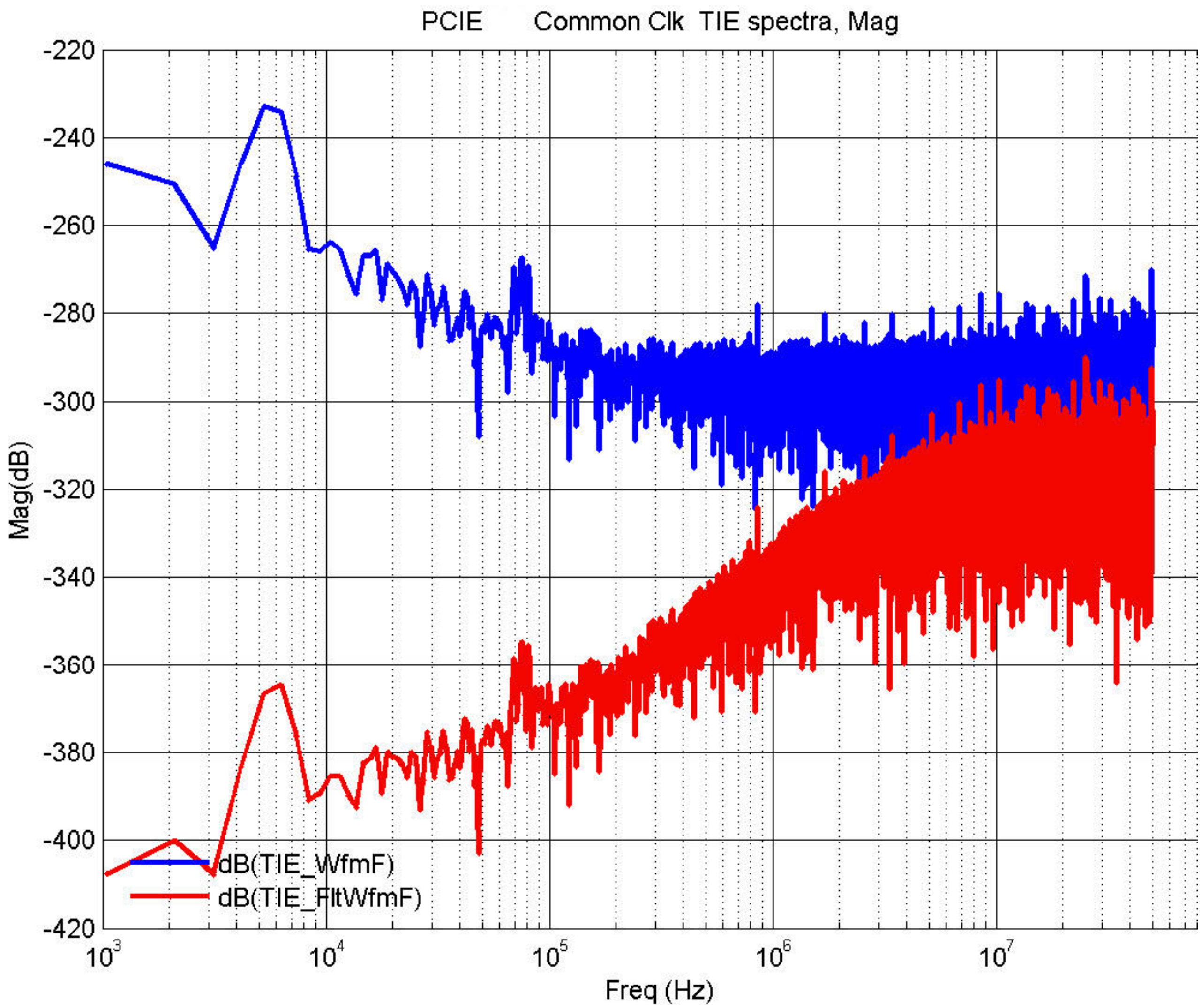


Figure 51 Reference Image for Common Clock TIE Spectra RMS Jitter Test

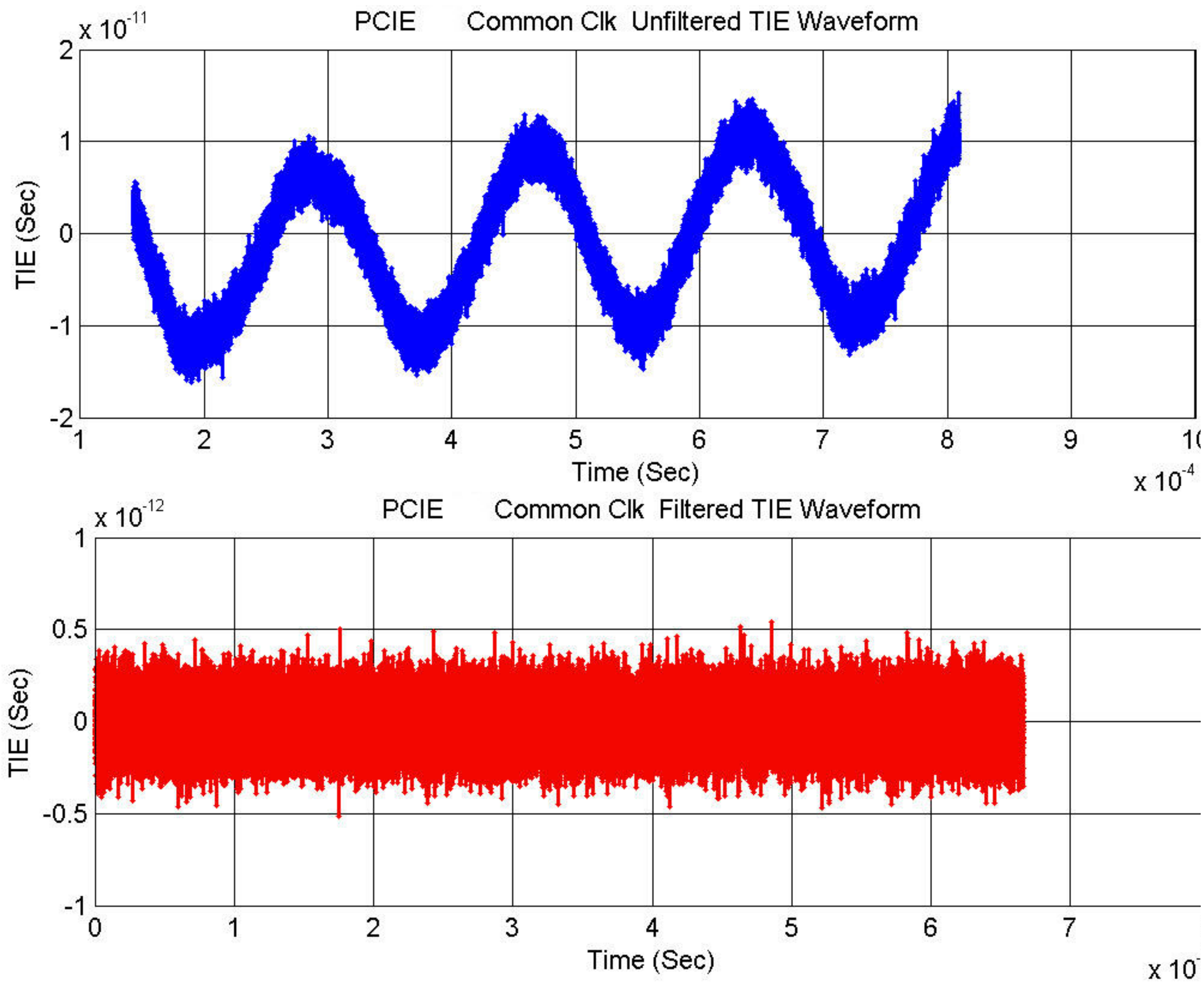


Figure 52 Reference Image for TIE Waveform RMS Jitter Test

Clock Frequency (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in the PCIE Base Specification.

Test Reference

PCI Express Base Specification, Rev 6.0, Section 8.6.3, Table 8-18 is used as reference to check the compliance of the DUT.

Table 58 RMS Jitter Test Details

Symbol	Description	Min	Max
$T_{REFCLK\_32G\_64G}$	Ref Clock Frequency (Common Clk)	99.99 MHz	100.01 MHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 1193 and select **Clock Frequency (Common Clk) (Data Clk).**

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Sets the time scale to 5 ns.
5 Fits and displays all sample data on the screen.
6 Enables jitter analysis so that measurements are made on all edges.
7 Measures the clock frequency.
8 Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part XV
Appendices

A Calibrating the Digital Storage Oscilloscope

This appendix describes the Keysight digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the oscilloscope in preparation for running the PCI Express automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2, (provided with the Keysight Infiniium oscilloscope).
- Calibration cable.
- BNC shorting cap.

Figure 1 below shows a drawing of the above connector items.

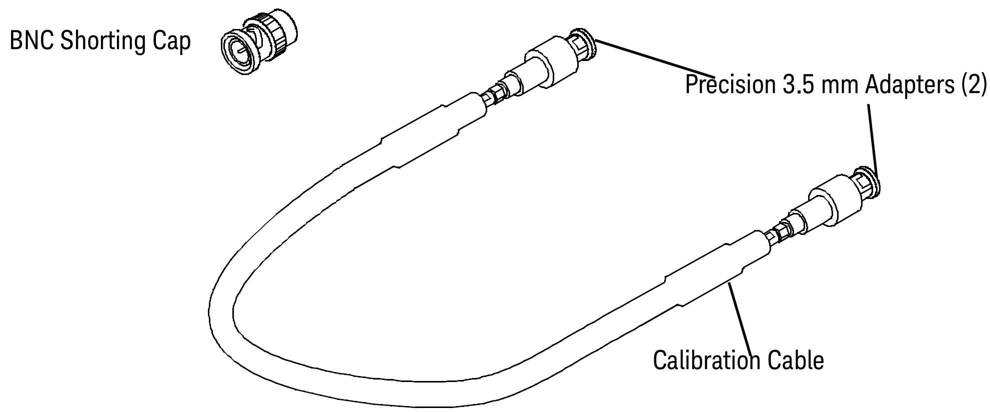


Figure 1 Accessories Provided with the Keysight Oscilloscope

- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG316/U or similar, qty = 2, matched length.
- SMA T-adapter.
- BNC to SMA male adapter, qty = 1.

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

- *a* Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
- *b* If SigTest is being used on the oscilloscope, then connect a second monitor to the VGA connector located near the LAN port, on the rear of the oscilloscope.
- *c* Plug in the power cord.
- *d* Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
- *e* Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

- *a* Locate the BNC shorting cap.
- *b* Locate the calibration cable.
- *c* Locate the two Keysight precision SMA/BNC adapters.
- *d* Attach one SMA adapter to one end of the calibration cable - hand tighten snugly.
- *e* Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 2 below, perform the following steps:

- *a* Click on the Utilities>Calibration menu to open the Calibration window.

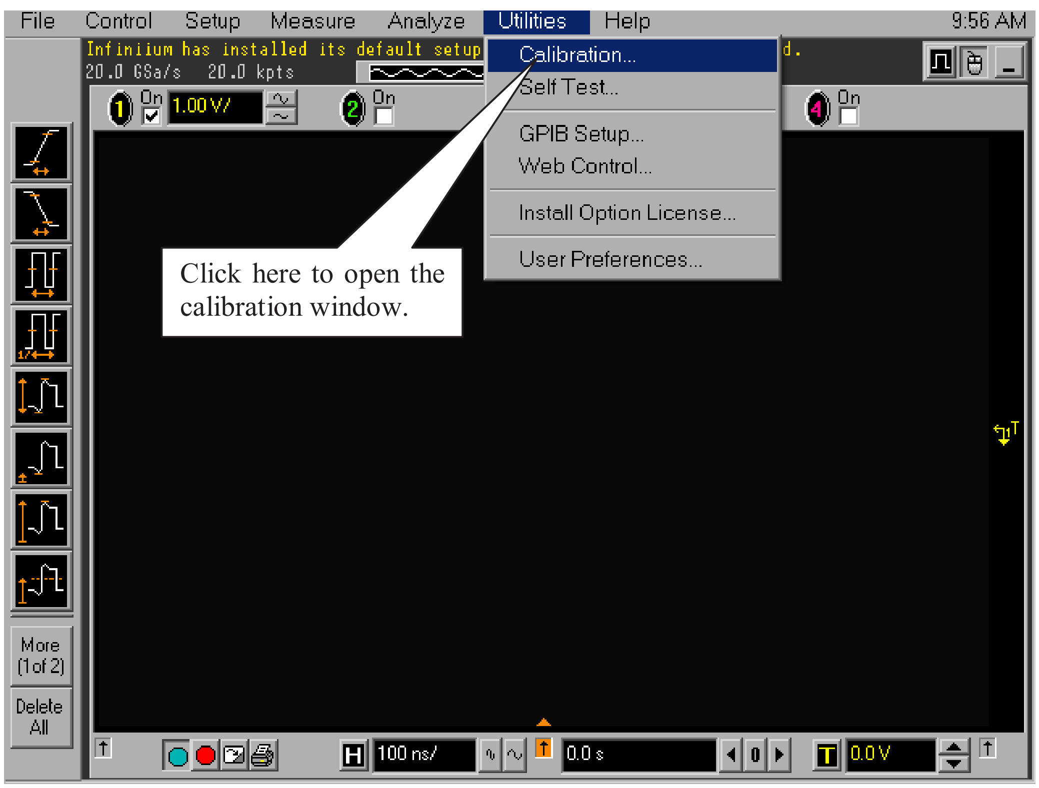


Figure 2 Accessing the Calibration Menu.

4 Referring to Figure 3 below, perform the following steps to start the calibration:

   a Uncheck the Cal Memory Protect checkbox.

   b Click the Start button to begin the calibration.

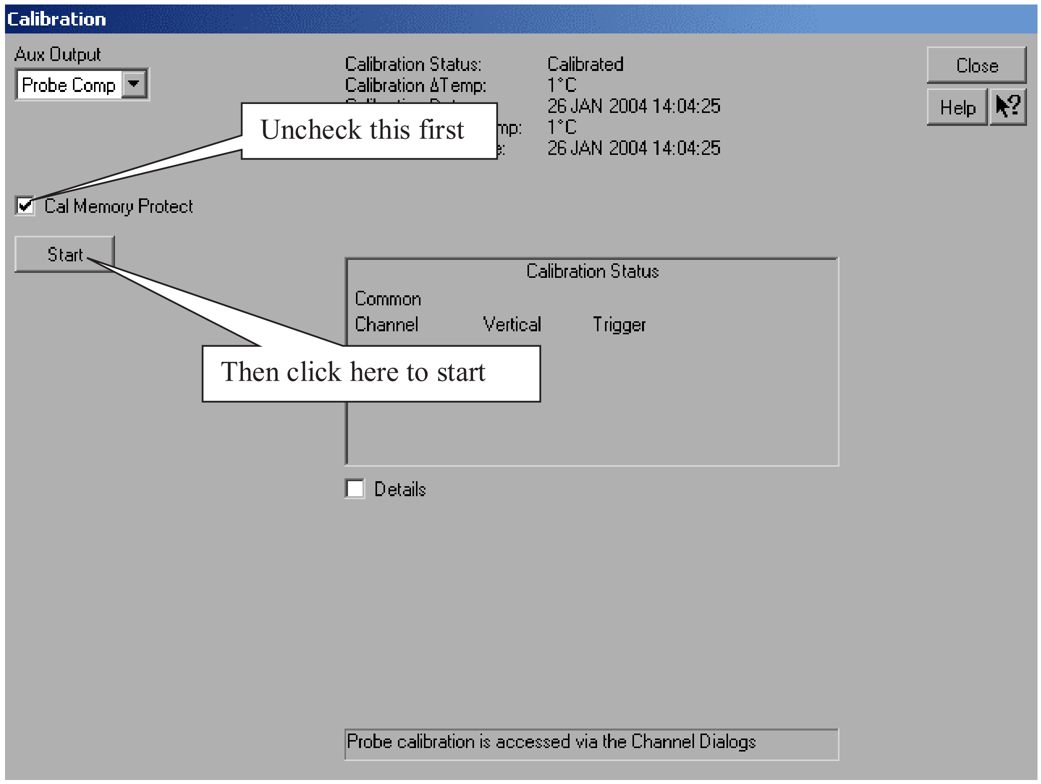


Figure 3 Oscilloscope Calibration Menu.

5 Follow the on-screen instructions:

   a You will be prompted to disconnect everything from all the inputs, click the OK button.

   b Then, you will be prompted to connect BNC shorting cap to a specified input. Install the BNC shorting cap by pressing it on the specified input BNC, and turning right. Click the OK button after moving the BNC cap to each specified channel.

c Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input, as shown in the example in Figure 4 below. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

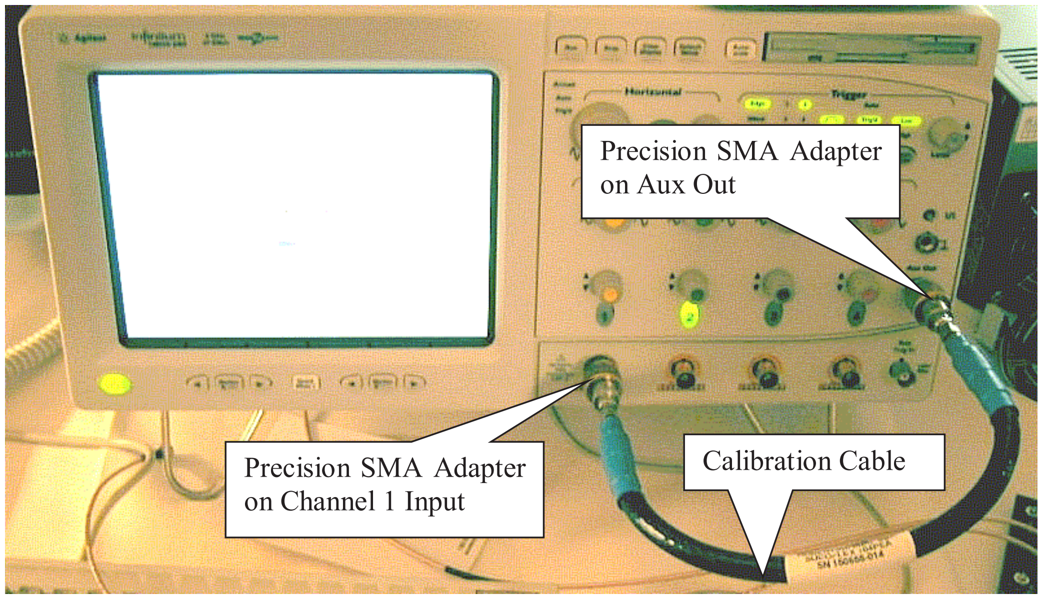


Figure 4 Calibration Cable Connection Example.

d Early during the calibration of channel 1, you will be prompted to perform a Time Scale Calibration, as shown in Figure 5 below.

e Click on the Default button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

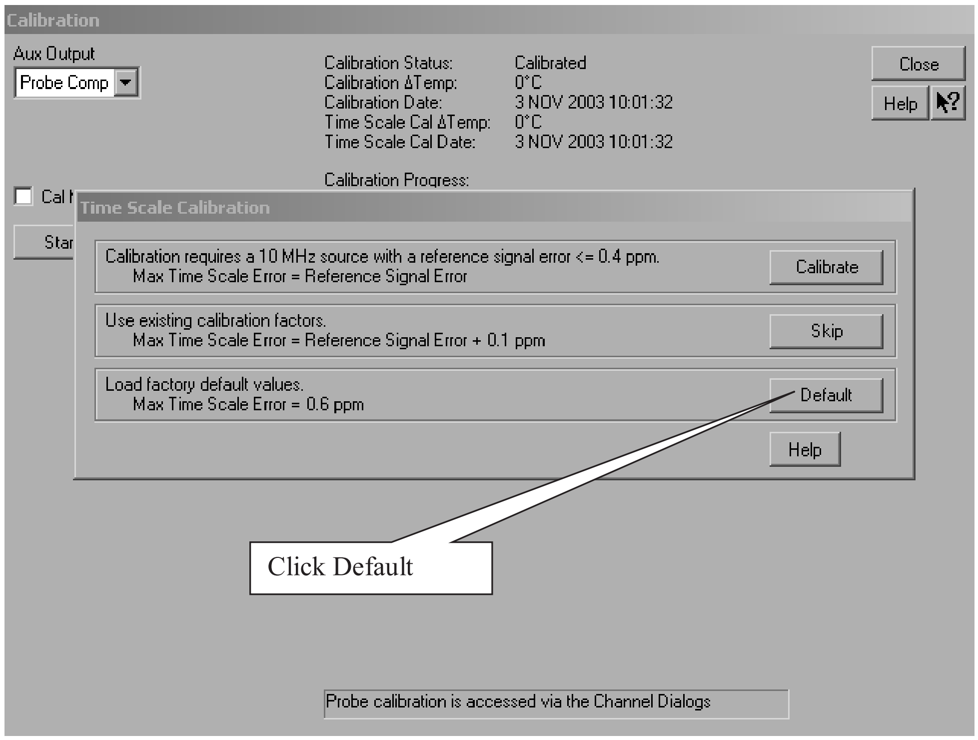


Figure 5 Time Scale Calibration Menu.

6 Referring to Figure 6 below, perform the following steps:

a Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

b Click the Close button to close the calibration window.

c The internal calibration is completed.

d Read NOTE below.

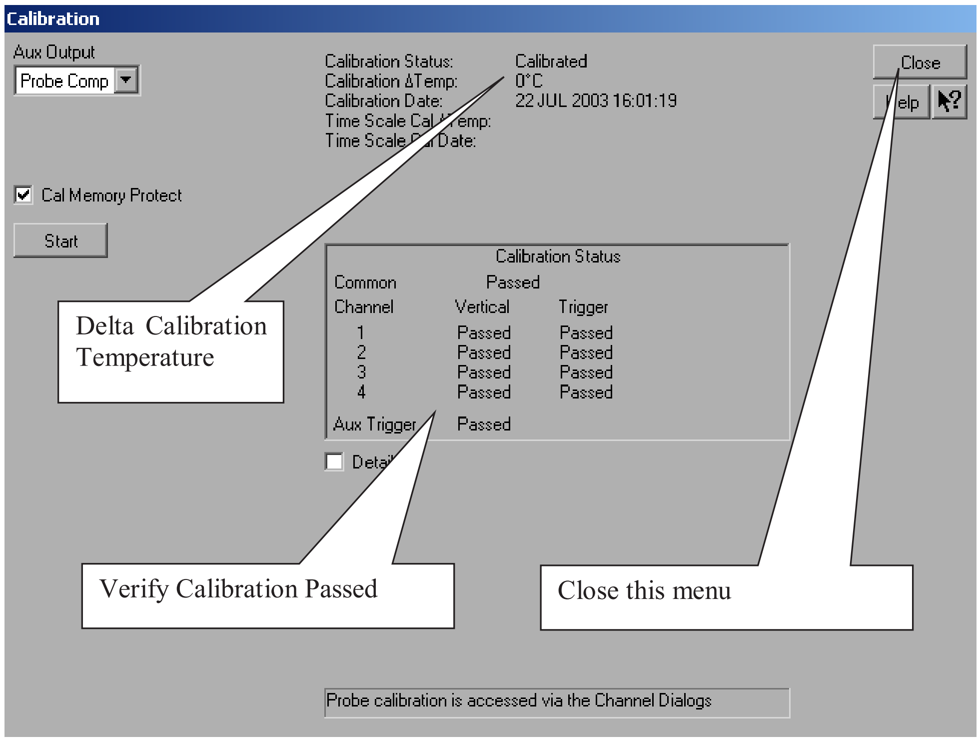


Figure 6 Calibration Status Screen.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Cable and Probe Calibration

Perform a 50-ohm direct-coupled input calibration for the SMA interface of channel 1 and channel 3. This calibration compensates for gain, offset, and skew errors in cables and probes. Perform the following steps.

1 Referring to the Figure 7 below, perform the following steps:

  a Locate and connect one of the Keysight precision SMA adapters to the Channel 1 oscilloscope input.

  b Locate and connect the other Keysight precision SMA adapter to the Channel 3 oscilloscope input.

  c Locate and connect one end of one of the RG-316 cables to the SMA adapter on Channel 1.

  d Locate and connect one end of the other RG-316 cable to the SMA adapter on Channel 3.

  e Locate and connect the non-Keysight SMA/BNC adapter to the Aux Out BNC on the oscilloscope.

  f Connect the other end of the cable attached to Channel 1 to the SMA adapter on the Aux Out.

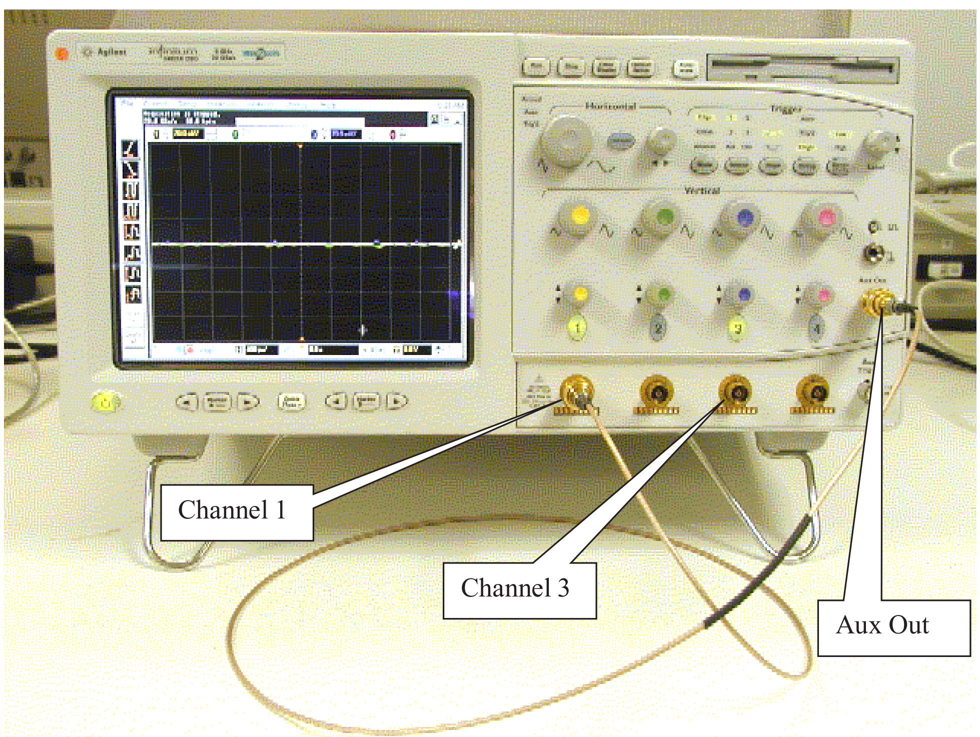


Figure 7 Vertical Input Calibration Connections (Cable on Channel 3 not shown).

2 Referring to Figure 8 below, perform the following steps:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Click the Probes button in the Channel Setup window, to open the Probe Setup window.

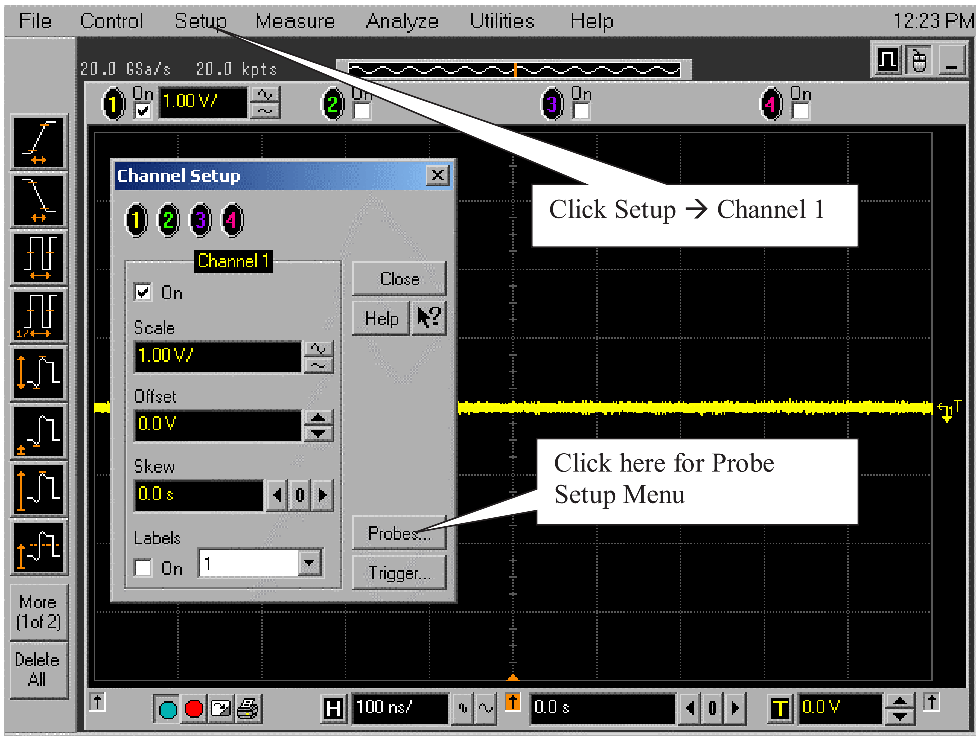


Figure 8 Channel Setup Window.

3 Referring to Figure 9 below, perform the following steps:

a Click the Configure Probing System button, and then click on User Defined Probes.

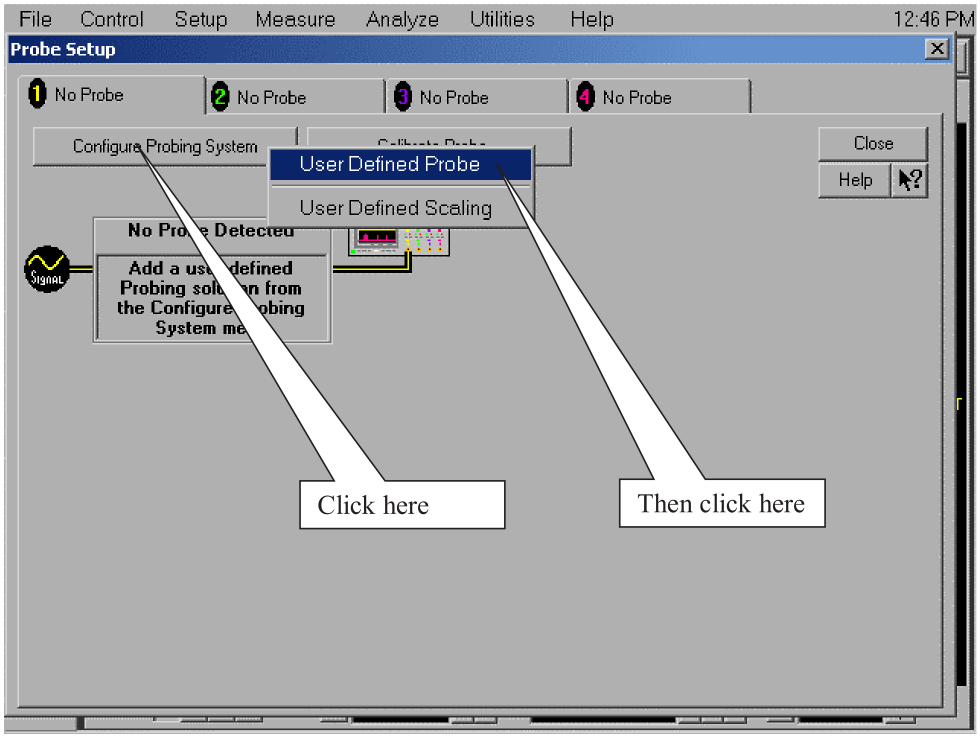


Figure 9 Probe Setup Window.

4 Referring to Figure 10 below, perform the following steps:

   a Click on the Calibrate Probe button to open the Probe Calibration window.

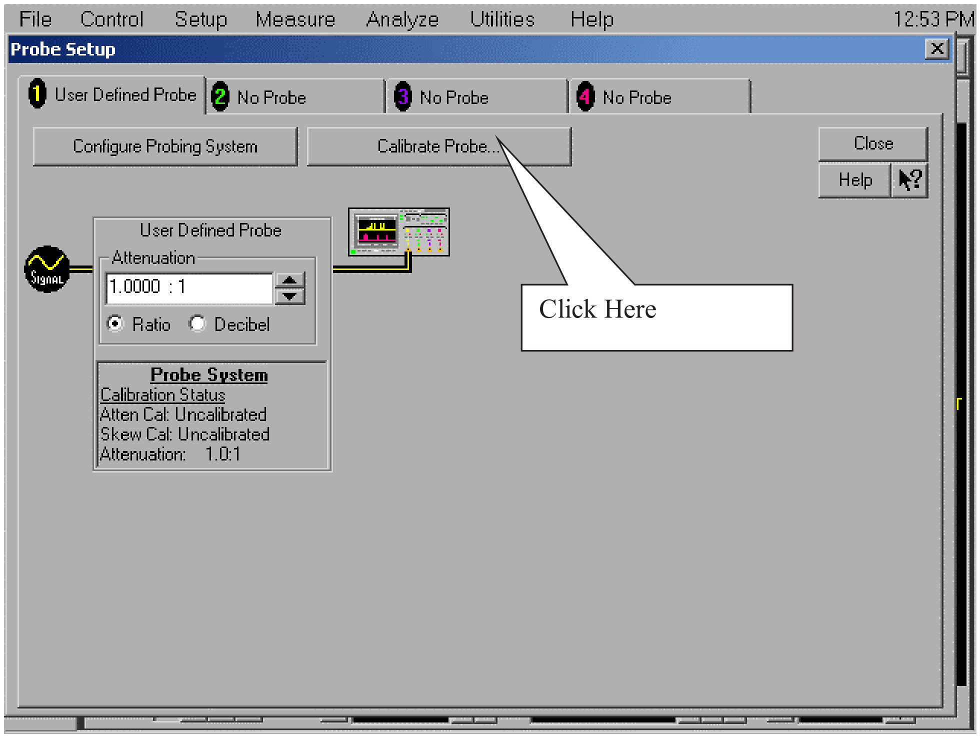


Figure 10 User Defined Probe Window.

5 Referring to Figure 11 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

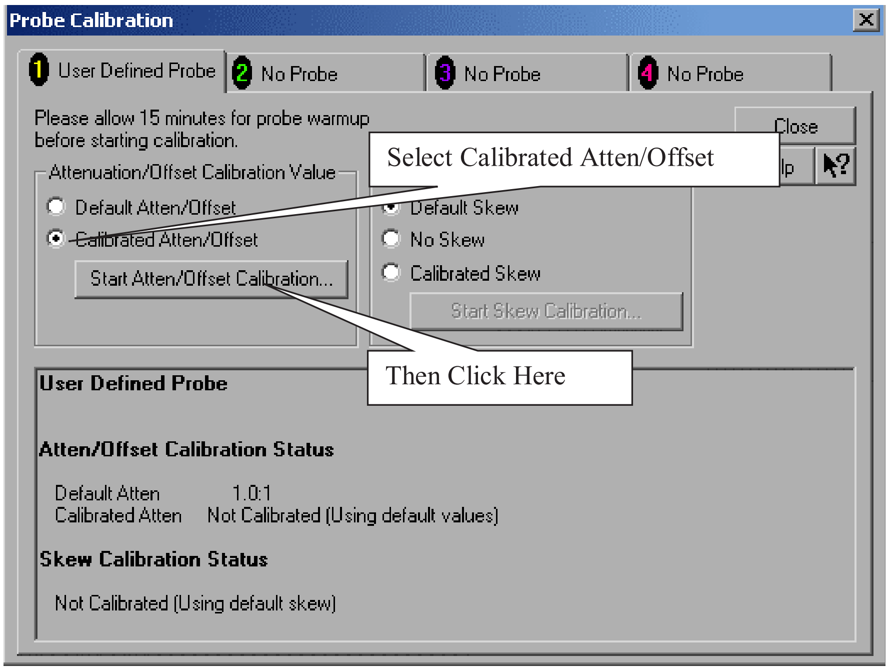


Figure 11 Probe Calibration Window.

6 Referring to Figure 12 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

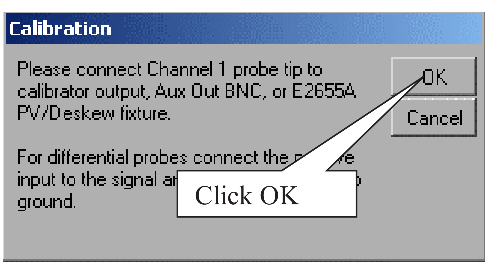


Figure 12 Calibration Window.

7 Referring to Figure 13 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

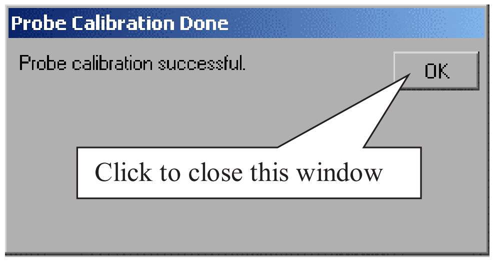


Figure 13 Probe Calibration Done Window.

8 Referring to Figure 14 below, perform the following steps:

a Select the Calibrated Skew Radio button in the Probe Calibration window

b Click the Start Skew Calibration button

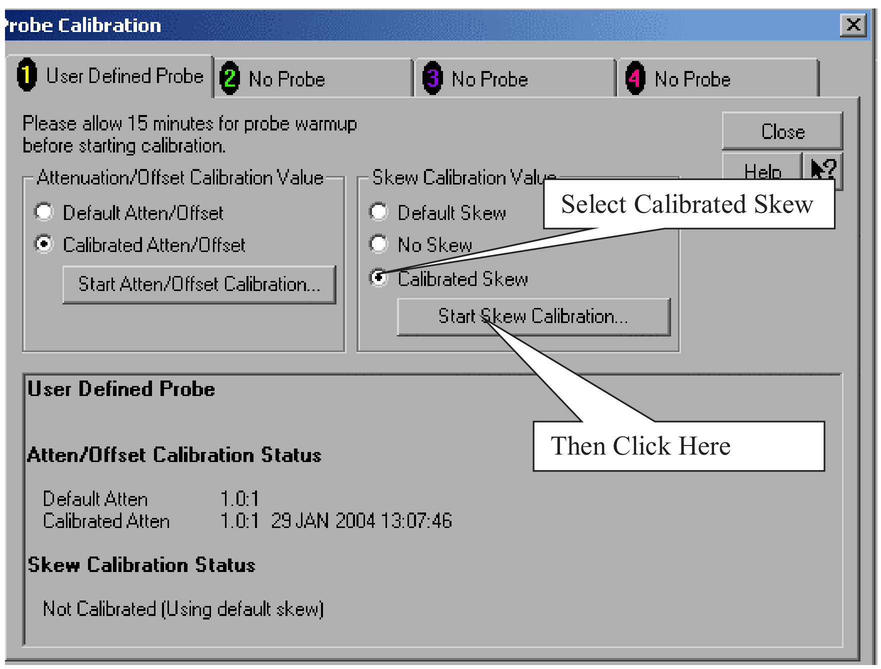


Figure 14 Probe Calibration Window.

9 Referring to Figure 15 shown below, perform the following steps:
  a Ignore the instructions shown in the dialog box.
  b Click the OK button on the Calibration window.
  c The calibration should complete in about 10 seconds.

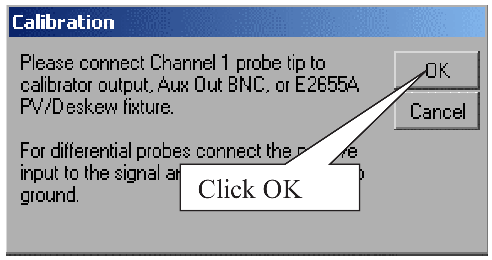


Figure 15 Calibration Window.

10 Referring to Figure 16 below, perform the following steps:
  a Click OK to close the Probe Calibration Done window.

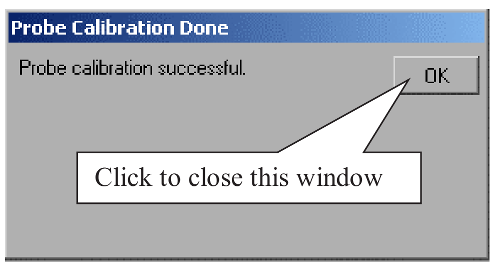


Figure 16 Calibration Window.

11 Referring to Figure 17 below, perform the following steps:

   a Click the Close button to close this window.

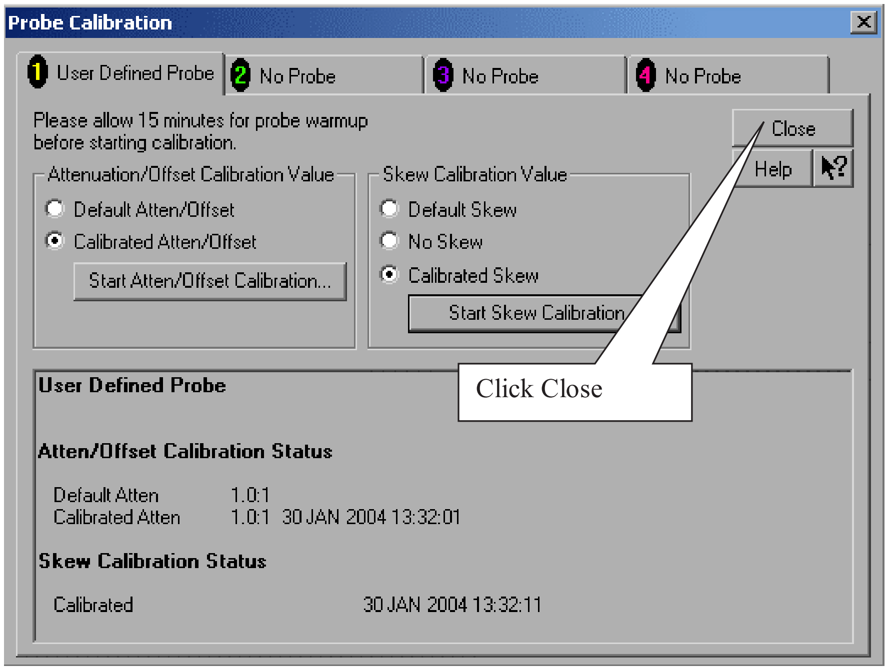


Figure 17 Calibration Window.

12 Referring to Figure 18 below, perform the following steps:

a Click on the Channel 3 tab.

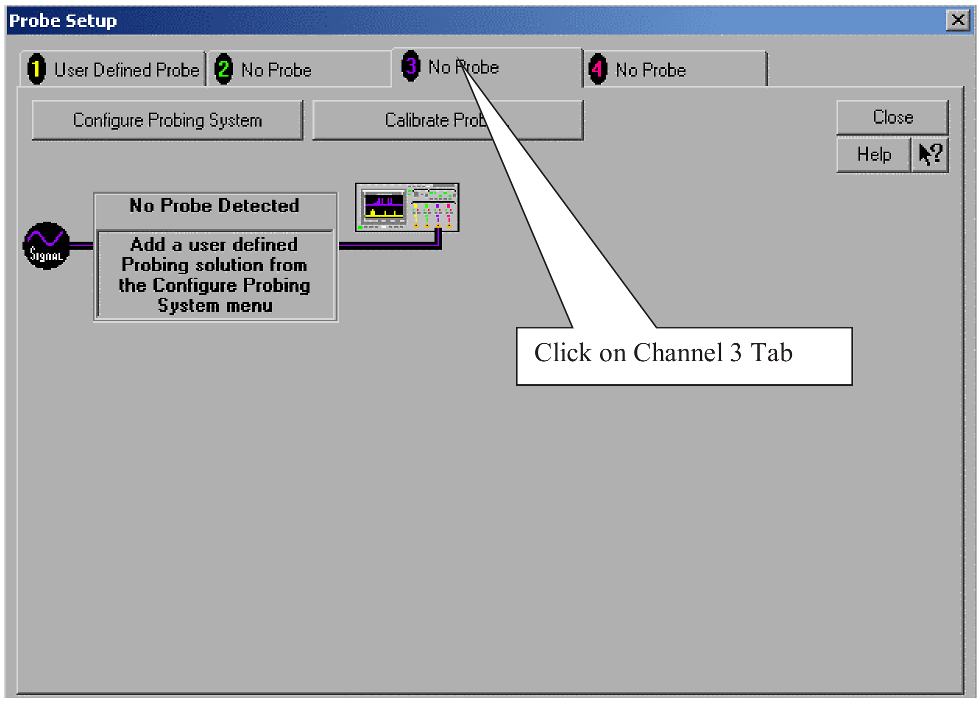


Figure 18 Calibration Window.

13 Referring to Figure 7 on page 1214, perform the following steps:

a Disconnect the RG-316 cable connected to the SMA adapter on the Aux Out.

b Connect the other end of the RG-316 cable connected to the SMA adapter on Channel 3, to the SMA adapter on the Aux Out.

14 Repeat steps 3 through 11 of this section to calibrate the cable on Channel 3.

15 Click the Close button on the Probe Setup window (Figure 18) to close this window.

16 Click the Close button on the Channel Setup window (Figure 8 on page 1215) to close this window.

17 The Cable and Probe calibration is complete.

18 Read the NOTE below.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

Channel-to-Channel De-skew

This procedure ensures that the timing skew errors between channel 1 and channel 3 are minimized. Perform the following steps:

1 Referring to Figure 19 below, perform the following steps:

   a Do not disconnect the RG-316 cables from either the Channel 1 or Channel 3 SMA adapters.

   b If not already installed, install the non-Keysight SMA adapter on the oscilloscope Aux Out.

   c Disconnect any cable connected to the SMA adapter on the Aux Out.

   d Locate and connect the middle branch of the SMA Tee to the SMA adapter on the Aux Out BNC.

   e Connect the far end of the cable from the Channel 1 SMA adapter, to one branch of the SMA Tee on the Aux Out.

   f Connect the far end of the cable from the Channel 3 SMA adapter, to the other branch of the SMA Tee on the Aux Out.

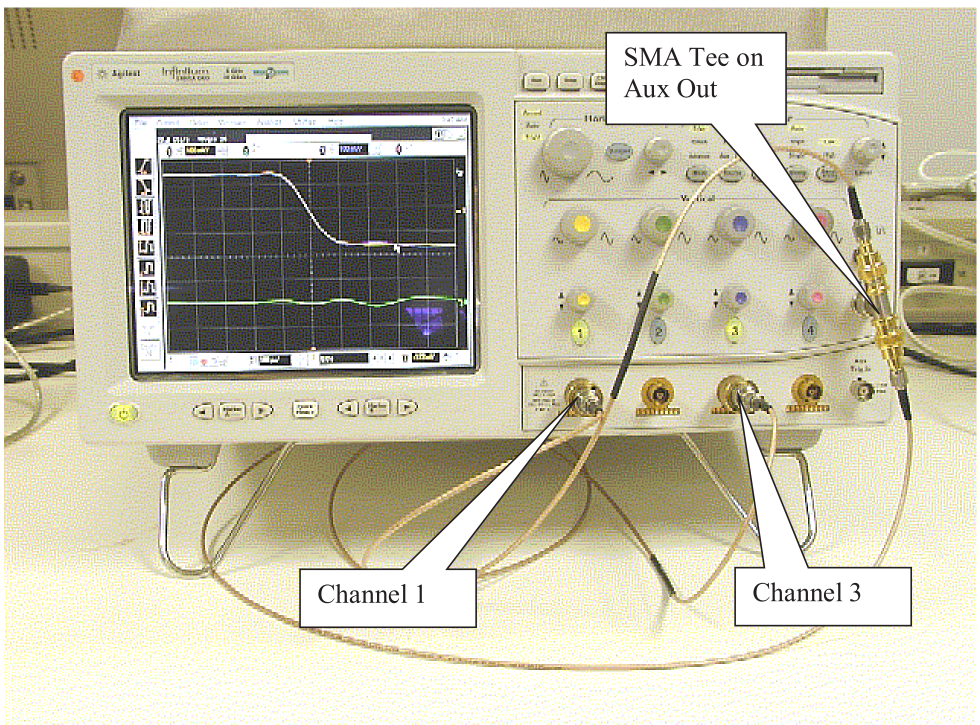


Figure 19 De-skew Connection.

2 Referring to Figure 20 below, perform the following steps:

   a Select the File>Load>Setup menu to open the Load Setup window.

   b Navigate to the directory location that contains the INF_SMA_Deskew.set setup file. If the setup file is not available, it can be created by following the instructions in Appendix B, “INF_SMA_Deskew.set Setup File Details.

   c Select the INF_SMA_Deskew.set setup file by clicking on it.

   d Click the Load button to configure the oscilloscope from this setup file.

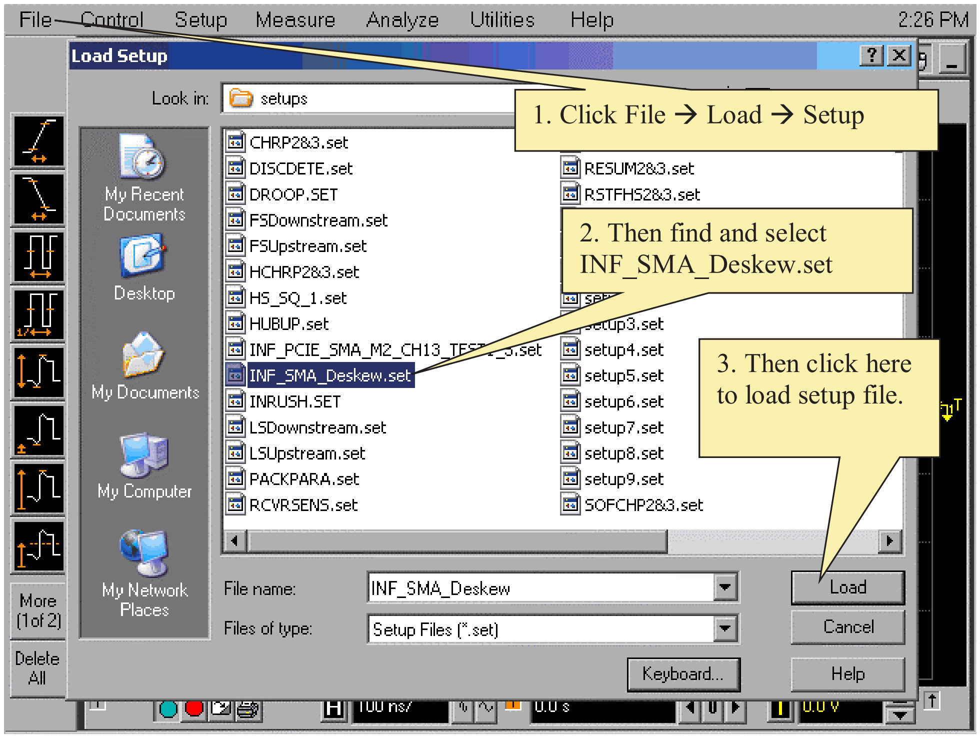


Figure 20 Load De-skew Setup.

The oscilloscope display should look similar to Figure 21 below. A falling edge of the square wave is shown in a 200 ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure 21 is an example of exaggerated skew between channel 1 and channel 3, measured to be about 50 ps with the cursor.

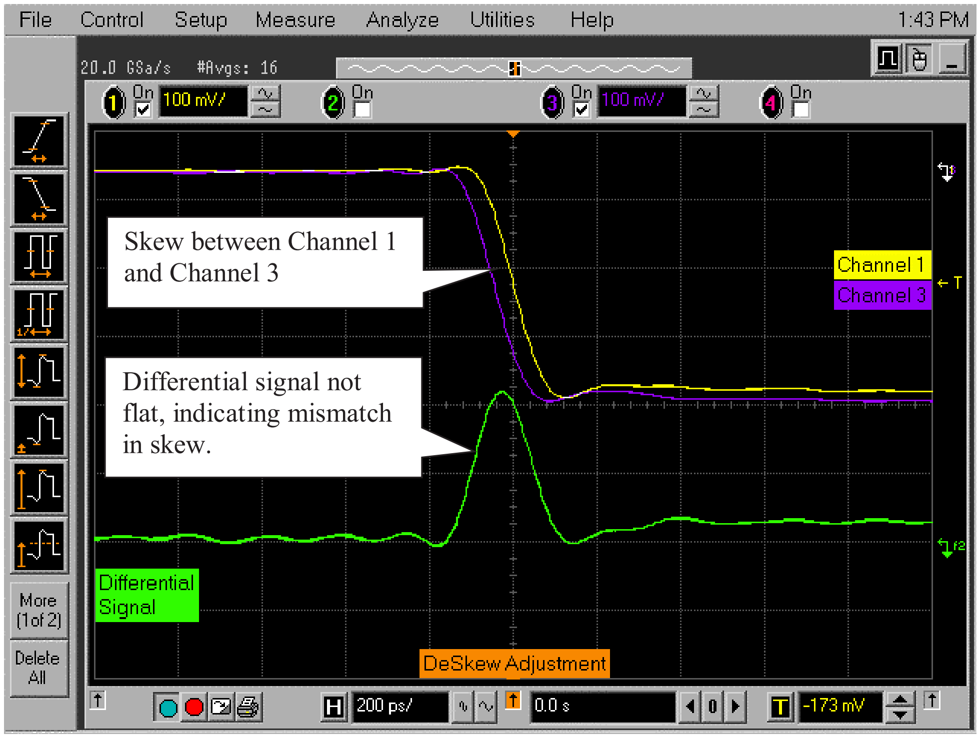


Figure 21 Channel Skew.

Figure 22 below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace), channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

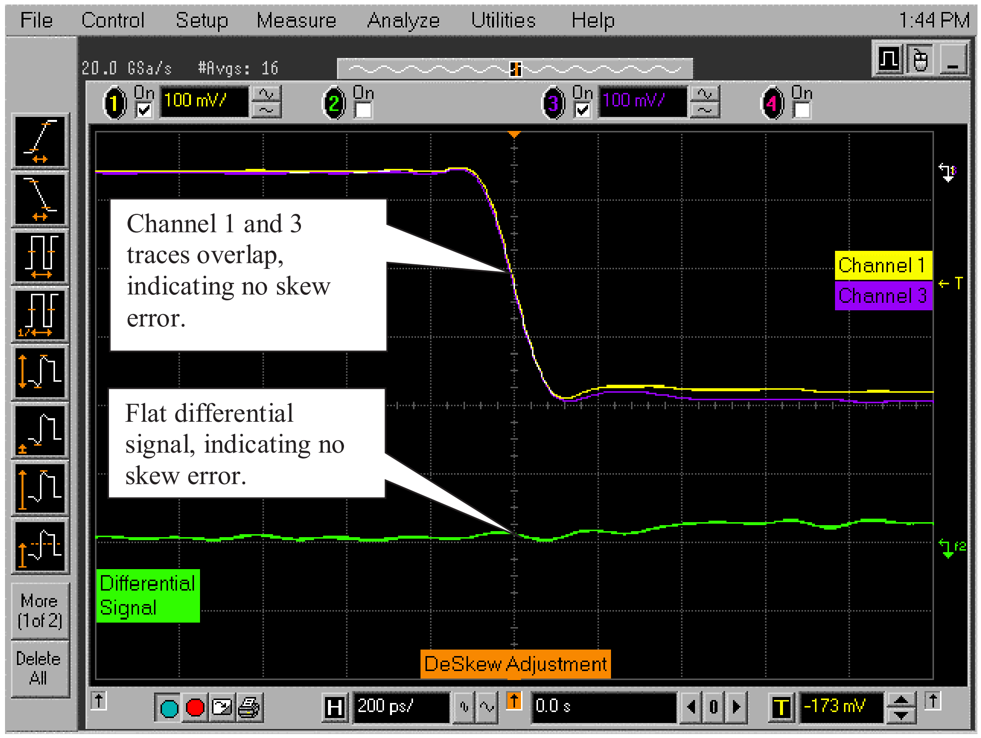


Figure 22 Skew Minimized.

3 Referring to Figure 23, perform the following steps to de-skew the channels:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Move the Channel Setup window to the left so you can see the traces.

c Adjust the Skew by clicking on the < or > arrows, to achieve the flattest response on the differential signal (green trace).

d Click the Close button on the Channel Setup window to close it.

e The de-skew operation is complete.

f Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

g Read the NOTE below.

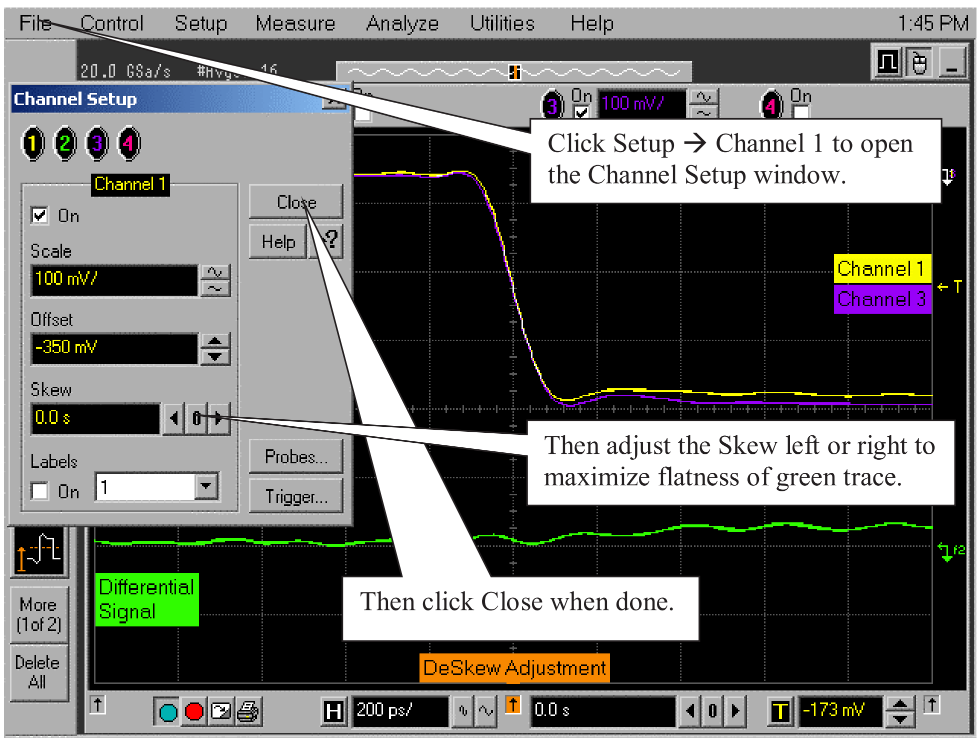


Figure 23 De-skewing Procedure.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

B INF_SMA_Deskew.set Setup File Details

If the INF_SMA_Deskew.set file is not available, you can create it by following these instructions.

1 Start from a default setup by pressing the Default Setup key on the front panel. Then configure the following settings:

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

C InfiniiMax Probing Options

Figure 24 1134A/B InfiniiMax Probe Amplifier

Figure 25 1134A/B Probe Amplifier and E2675A/B Differential Browser Probe Head

Keysight recommends 1169A/B or 1134A/B probe amplifiers. PCI Express 2.0 requires minimum of 1169A/B probe amplifiers. Keysight also recommends either the E2677A/B differential solder-in probe head or the E2675A/B differential browser probe head.

The differential solder-in probe head (E2677A/B) is recommended for highest signal fidelity while the differential browser probe head (E2675A/B) may be used for probing convenience.

Figure 26 Recommended Probe Heads for the PCI Express Testing

Table 1 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential browser	E2675A/B	6 GHz, 0.32 pF, 50 kOhm	6 GHz, 0.57 pF, 25 kOhm
Differential solder-in	E2677A/B	7 GHz / 12 GHz, 0.27 pF, 50 kOhm	7 GHz / 12GHz, 0.44 pF, 25 kOhm
Differential socket	E2678A/B	7 GHz / 12 GHz, 0.34 pF, 50 kOhm	7 GHz / 12 GHz, 0.56 pF, 25 kOhm

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